DDR2 SDRAM Mini-RDIMM

MT9HTF6472PKZ – 512MB

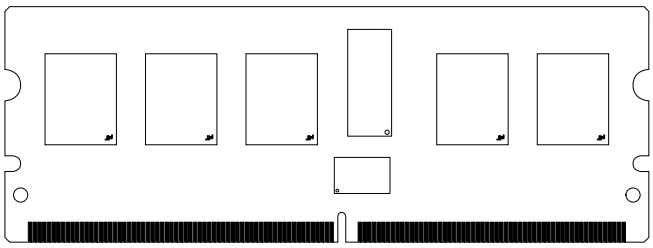
MT9HTF12872PKZ – 1GB

Features

- 244-pin, mini registered dual in-line memory module
- Fast data transfer rates: PC2-6400, PC2-5300, PC2-4200, or PC2-3200
- 512MB (64 Meg x 72), 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = 1.8V$
- $V_{DDSPD} = 1.7–3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Single rank
- Halogen-free

Figure 1: 244-Pin Mini-RDIMM (MO-244, R/C A)

Module Height: 30mm (1.181 in.)



Options	Marking
• Parity	P
• Operating temperature	
– Commercial (0°C ≤ T_A ≤ 70°C)	None
– Industrial (–40°C ≤ T_A ≤ 85°C)[1]	I
• Package	
– 244-pin DIMM (halogen-free)	Z
• Frequency/CL[2]	
– 2.5ns @ CL = 5 (DDR2-800)	-80E
– 2.5ns @ CL = 6 (DDR2-800)	-800
– 3.0ns @ CL = 5 (DDR2-667)	-667

Notes:
1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	800	533	400	12.5	12.5	55
-800	PC2-6400	800	667	533	400	15	15	55
-667	PC2-5300	–	667	553	400	15	15	55
-53E	PC2-4200	–	–	553	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 2: Addressing

	512MB	1GB
Refresh count	8K	8K
Row address	16K A[13:0]	16K A[13:0]
Device bank address	4 BA[1:0]	8 BA[2:0]
Device configuration	512Mb (64 Meg x8)	1Gb (128 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	1 S0#	1 S0#

Table 3: Part Numbers and Timing Parameters – 512MB

Base device: MT47H64M8,[1] 512Mb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL - ^{t}RCD - ^{t}RP)
MT9HTF6472PK(I)Z-80E__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF6472PK(I)Z-800__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF6472PK(I)Z-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5

Table 4: Part Numbers and Timing Parameters – 1GB

Base device: MT47H128M8,[1] 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9HTF12872PK(I)Z-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF12872PK(I)Z-800__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF12872PK(I)Z-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9HTF12872PKZ-80EH1.

Pin Assignments

Table 5: Pin Assignments

244-Pin VLP Mini-RDIMM Front								244-Pin VLP Mini-RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REF}	32	V_{SS}	63	V_{DDQ}	94	DQS5#	123	V_{SS}	154	DQ28	185	A3	216	NC
2	V_{SS}	33	DQ24	64	A2	95	DQS5	124	DQ4	155	DQ29	186	A1	217	V_{SS}
3	DQ0	34	DQ25	65	V_{DD}	96	V_{SS}	125	DQ5	156	V_{SS}	187	V_{DD}	218	DQ46
4	DQ1	35	V_{SS}	66	V_{SS}	97	DQ42	126	V_{SS}	157	DM3	188	CK0	219	DQ47
5	V_{SS}	36	DQS3#	67	V_{SS}	98	DQ43	127	DM0	158	NC	189	CK0#	220	V_{SS}
6	DQS0#	37	DQS3	68	Par_In	99	V_{SS}	128	NC	159	V_{SS}	190	V_{DD}	221	DQ52
7	DQS0	38	V_{SS}	69	V_{DD}	100	DQ48	129	V_{SS}	160	DQ30	191	A0	222	DQ53
8	V_{SS}	39	DQ26	70	A10	101	DQ49	130	DQ6	161	DQ31	192	BA1	223	V_{SS}
9	DQ2	40	DQ27	71	BA0	102	V_{SS}	131	DQ7	162	V_{SS}	193	V_{DD}	224	NC
10	DQ3	41	V_{SS}	72	V_{DD}	103	SA2	132	V_{SS}	163	CB4	194	RAS#	225	NC
11	V_{SS}	42	CB0	73	WE#	104	NC	133	DQ12	164	CB5	195	V_{DDQ}	226	V_{SS}
12	DQ8	43	CB1	74	V_{DDQ}	105	V_{SS}	134	DQ13	165	V_{SS}	196	S0#	227	DM6
13	DQ9	44	V_{SS}	75	CAS#	106	DQS6#	135	V_{SS}	166	DM8	197	V_{DDQ}	228	NC
14	V_{SS}	45	DQS8#	76	V_{DDQ}	107	DQS6	136	DM1	167	NC	198	ODT0	229	V_{SS}
15	DQS1#	46	DQS8	77	NC	108	V_{SS}	137	NC	168	V_{SS}	199	A13	230	DQ54
16	DQS1	47	V_{SS}	78	NC	109	DQ50	138	V_{SS}	169	CB6	200	V_{DD}	231	DQ55
17	V_{SS}	48	CB2	79	V_{DDQ}	110	DQ51	139	NC	170	CB7	201	NC	232	V_{SS}
18	RESET#	49	CB3	80	NC	111	V_{SS}	140	NC	171	V_{SS}	202	V_{SS}	233	DQ60
19	NC	50	V_{SS}	81	V_{SS}	112	DQ56	141	V_{SS}	172	NC	203	DQ36	234	DQ61
20	V_{SS}	51	NC	82	DQ32	113	DQ57	142	DQ14	173	V_{DDQ}	204	DQ37	235	V_{SS}
21	DQ10	52	V_{DDQ}	83	DQ33	114	V_{SS}	143	DQ15	174	NC	205	V_{SS}	236	DM7
22	DQ11	53	CKE0	84	V_{SS}	115	DQS7#	144	V_{SS}	175	V_{DD}	206	DM4	237	NC
23	V_{SS}	54	V_{DD}	85	DQS4#	116	DQS7	145	DQ20	176	A15	207	NC	238	V_{SS}
24	DQ16	55	NC/BA2[1]	86	DQS4	117	V_{SS}	146	DQ21	177	A14	208	V_{SS}	239	DQ62
25	DQ17	56	Err_Out#	87	V_{SS}	118	DQ58	147	V_{SS}	178	V_{DDQ}	209	DQ38	240	DQ63
26	V_{SS}	57	V_{DDQ}	88	DQ34	119	DQ59	148	DM2	179	A12	210	DQ39	241	V_{SS}
27	DQS2#	58	A11	89	DQ35	120	V_{SS}	149	NC	180	A9	211	V_{SS}	242	SDA
28	DQS2	59	A7	90	V_{SS}	121	SA0	150	V_{SS}	181	V_{DD}	212	DQ44	243	SCL
29	V_{SS}	60	V_{DD}	91	DQ40	122	SA1	151	DQ22	182	A8	213	DQ45	244	V_{DDSPD}
30	DQ18	61	A5	92	DQ41			152	DQ23	183	A6	214	V_{SS}		
31	DQ19	62	A4	93	V_{SS}			153	V_{SS}	184	V_{DDQ}	215	DM5		

Note: 1. Pin 55 is NC for 512MB, or BA2 for 1GB.

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR2 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 6: Pin Descriptions

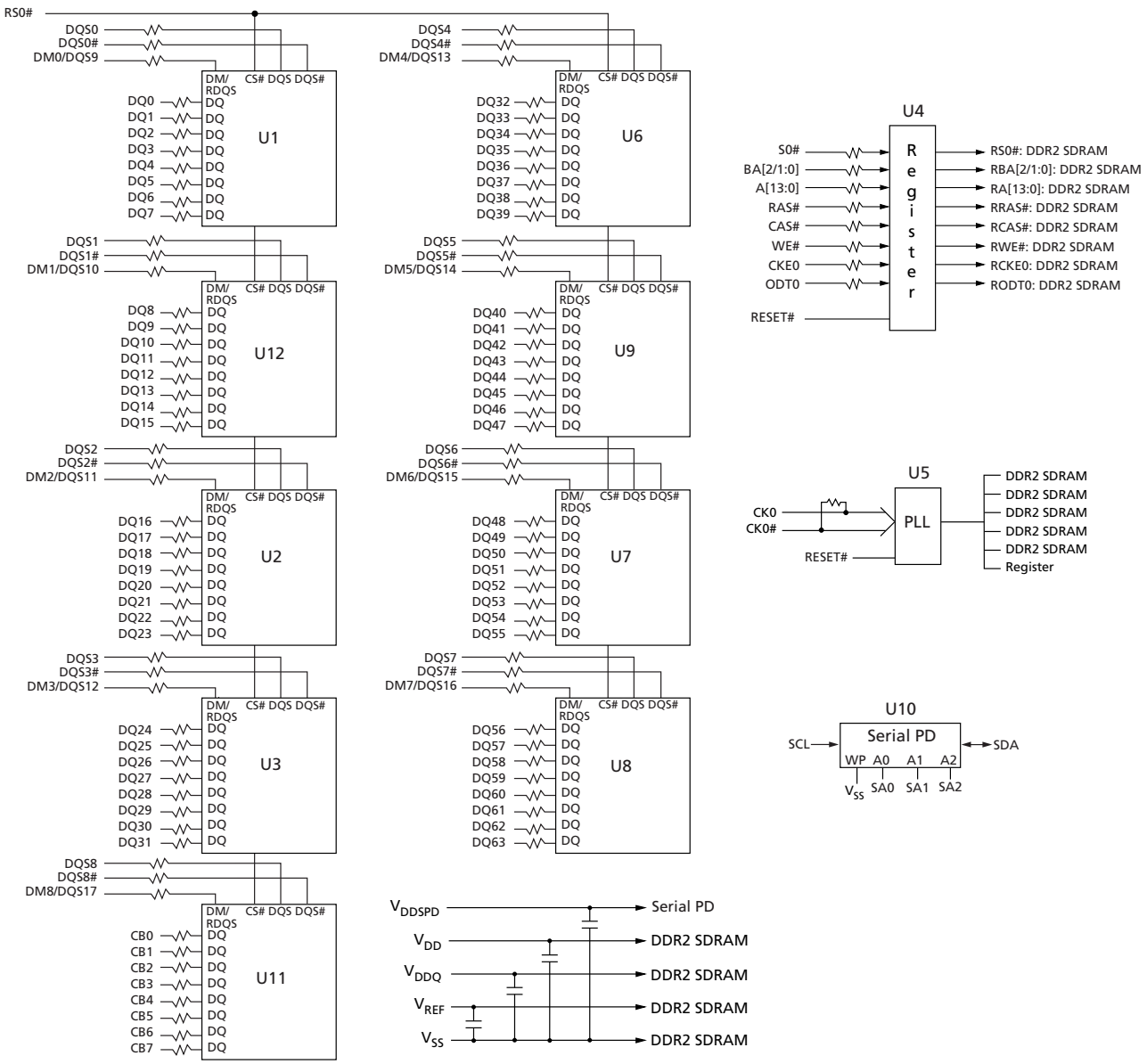
Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CKx, CK#x	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.
DMx,	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S#x	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** Used to synchronize communication to and from the SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits.** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQS#x	I/O	**Data strobe:** Travels with the DQ and is used to capture DQ at the DRAM or the controller. Output with read data; input with write data for source synchronous operation. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.

Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the SPD EEPROM on the I^2C bus.
RDQSx, RDQS#x	Output	**Redundant data strobe (x8 devices only):** RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, RDQS becomes data mask (see DMx). RDQS# is only used when RDQS is enabled and differential data strobe mode is enabled.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
V_{DD}/V_{DDQ}	Supply	**Power supply:** 1.8V ±0.1V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**SPD EEPROM power supply:** 1.7–3.6V.
V_{REF}	Supply	**Reference voltage:** $V_{DD}/2$.
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.
NU	–	**Not used:** These pins are not used in specific module configurations/operations.
RFU	–	Reserved for future use.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

DDR2 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR2 SDRAM devices. DDR2 SDRAM modules use DDR architecture to achieve high-speed operation. DDR2 architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR2 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect EEPROM Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection.

Register and PLL Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Parity Operations

The registering clock driver can accept a parity bit from the system's memory controller, providing even parity for the control, command, and address bus. Parity errors are flagged on the Err_Out# pin. Systems not using parity are expected to function without issue if Par_In and Err_Out# are left as no connects (NC) to the system.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the DRAM devices on the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}/V_{DDQ}	V_{DD}/V_{DDQ} supply voltage relative to V_{SS}		–0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	2.3	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Command/address RAS#, CAS#, WE#, S#, CKE, ODT, BA	–5	5	µA
		CK, CK#	–250	250	
		DM	–5	5	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	–5	5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–18	18	µA
T_A	Module ambient operating temperature	Commercial	0	70	°C
		Industrial	–40	85	°C
T_C[1]	DDR2 SDRAM component case operating temperature[2]	Commercial	0	85	°C
		Industrial	–40	95	°C

Notes:
1. Refresh rate is required to double when 85°C < T_C ≤ 95°C.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

I_{DD} Specifications

Table 8: I_{DD} Specifications and Conditions – 512MB (Die Revision F)

Values shown for MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512MB (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E -800	-667	Units
Operating one bank active-precharge current: $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}	900	810	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN (I_{DD}), $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}	1035	945	mA
Precharge power-down current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}	63	63	mA
Precharge quiet standby current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}	450	405	mA
Precharge standby current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}	495	450	mA
Active power-down current: All device banks open; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3P}	360	315	mA
	Slow PDN exit MR[12] = 1		108	108	mA
Active standby current: All device banks open; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}	630	585	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}	1755	1530	mA
Operating burst read current: All device banks open; Continuous burst reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP$ (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}	1845	1620	mA
Burst refresh current: $^tCK = ^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}	2070	1620	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^tRCD (I_{DD})$ - 1 × $^tCK (I_{DD})$; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRRD = ^tRRD (I_{DD})$, $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		I_{DD7}	2700	2160	mA

Table 9: I_{DD} Specifications and Conditions – 512MB (Die Revision G)

Values shown for MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512MB (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E -800	-667	Units
Operating one bank active-precharge current: $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}	585	540	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN (I_{DD}), $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}	675	630	mA
Precharge power-down current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}	63	63	mA
Precharge quiet standby current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}	216	198	mA
Precharge standby current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}	252	225	mA
Active power-down current: All device banks open; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3P}	162	135	mA
	Slow PDN exit MR[12] = 1		81	81	mA
Active standby current: All device banks open; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}	297	270	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}	1125	1035	mA
Operating burst read current: All device banks open; Continuous burst reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP$ (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}	1080	990	mA
Burst refresh current: $^tCK = ^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}	855	810	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^tRCD (I_{DD})$ - 1 × $^tCK (I_{DD})$; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRRD = ^tRRD (I_{DD})$, $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		I_{DD7}	1350	1260	mA

Table 10: I_{DD} Specifications and Conditions – 1GB (Die Revisons E and G)

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E -800	-667	Units
Operating one bank active-precharge current: $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}	810	765	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN (I_{DD}), $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}	990	900	mA
Precharge power-down current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}	63	63	mA
Precharge quiet standby current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}	450	360	mA
Precharge standby current: All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}	450	360	mA
Active power-down current: All device banks open; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3P}	360	270	mA
	Slow PDN exit MR[12] = 1		90	90	mA
Active standby current: All device banks open; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}	540	495	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}	1440	1215	mA
Operating burst read current: All device banks open; Continuous burst reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP$ (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}	1440	1215	mA
Burst refresh current: $^tCK = ^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}	2115	1935	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^tRCD (I_{DD})$ - 1 × $^tCK (I_{DD})$; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRRD = ^tRRD (I_{DD})$, $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		I_{DD7}	3015	2520	mA

Table 11: I_{DD} Specifications and Conditions – 1GB (Die Revision H)

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E -800	-667	Units
Operating one bank active-precharge current: $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}	585	540	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN (I_{DD}), $^tRCD = {}^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}		I_{DD1}	675	630	mA
Precharge power-down current: All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}	63	63	mA
Precharge quiet standby current: All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}	216	216	mA
Precharge standby current: All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}	252	216	mA
Active power-down current: All device banks open; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3P}	180	135	mA
	Slow PDN exit MR[12] = 1		90	90	mA
Active standby current: All device banks open; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}	297	270	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}	1125	1035	mA
Operating burst read current: All device banks open; Continuous burst reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP$ (I_{DD}); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}	1080	990	mA
Burst refresh current: $^tCK = {}^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}	1305	1260	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^tRCD (I_{DD})$ - 1 × $^tCK (I_{DD})$; $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRRD = {}^tRRD (I_{DD})$, $^tRCD = {}^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		I_{DD7}	1890	1665	mA

Register and PLL Specifications

Table 12: Register Specifications

SSTU32866 devices or equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Control, command, address	SSTL_18	$V_{REF(DC)}$ + 125	V_{DDQ} + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Control, command, address	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Control, command, address	SSTL_18	$V_{REF(DC)}$ + 250	–	mV
AC low-level input voltage	$V_{IL(AC)}$	Control, command, address	SSTL_18	–	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	–	V
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.5	V
Input current	I_I	All pins	$V_I = V_{DD}$ or V_{SS}	–	±0.5	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I_O = 0)	–	100	µA
Static operating	I_{DD}	All pins	RESET# = V_{SS}; $V_I = V_{IH(AC)}$ or $V_{IL(DC)}$ I_O = 0	–	40	mA
Dynamic operating (clock tree)	I_{DDD}	N/A	RESET# = V_{DD}; $V_I = V_{IH(DC)}$ or $V_{IL(AC)}$, I_O = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	N/A	RESET# = V_{DD}; $V_I = V_{IH(AC)}$ or $V_{IL(DC)}$, I_O = 0; CK and CK# switching 50% duty cycle; One data in/out switching at $^tCK/2$, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_{IN}	All inputs except RESET#	$V_I = V_{REF}$ ±250mV; V_{DD} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C_{IN}	RESET#	$V_I = V_{DD}$ or V_{SS}	Varies by manufacturer	Varies by manufacturer	pF

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of the DDR2 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

Table 13: PLL Specifications

CU877 device or equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	V
Input voltage (limits)	V_{IN}	RESET#, CK, CK#	–	0.3	V_{DD} + 0.3	V
DC high-level input voltage	V_{IH}	CK, CK#	Differential input	0.65 × V_{DD}	–	V
DC low-level input voltage	V_{IL}	CK, CK#	Differential input	–	0.35 × V_{DD}	V
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential input	(V_{DDQ}/2) - 0.15	(V_{DD}/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	V_{DD} + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	V_{DD} + 0.4	V
Input current	I_I	RESET#	V_I = V_{DD} or V_{SS}	–10	10	µA
		CK, CK#	V_I = V_{DD} or V_{SS}	–250	250	µA
Output disabled current	I_{ODL}		RESET# = V_{SS}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}		CK = CK# = LOW	–	500	µA
Dynamic supply	I_{DD}	N/A	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = V_{DD} or V_{SS}	2	3	pF

Table 14: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	^{t}L	–	15	µs
Input clock slew rate	slr(i)	1.0	4.0	V/ns
SSC modulation frequency	–	30	33	kHz
SSC clock input frequency deviation	–	0.0	–0.5	%
PLL loop bandwidth (–3dB from unity gain)	–	2.0	–	MHz

Note: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 15: SPD EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 kHz	I_{CCR}	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I_{CCW}	2	3	mA

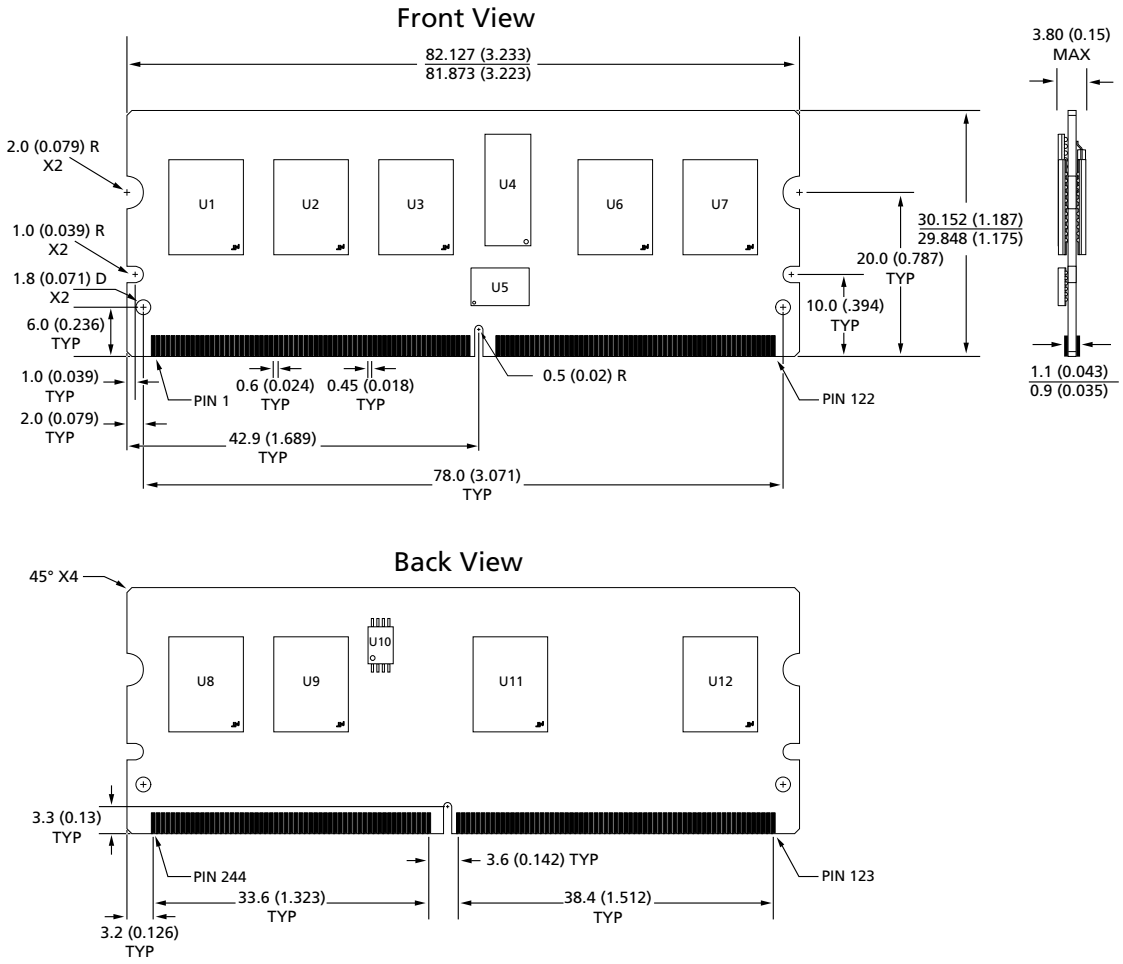
Table 16: SPD EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
SDA and SCL fall time	^{t}F	–	300	ns	2
SDA and SCL rise time	^{t}R	–	300	ns	2
Data-in hold time	$^{t}HD:DAT$	0	–	µs	
Start condition hold time	$^{t}HD:STA$	0.6	–	µs	
Clock HIGH period	$^{t}HIGH$	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SCL clock frequency	^{t}SCL	–	400	kHz	
Data-in setup time	$^{t}SU:DAT$	100	–	ns	
Start condition setup time	$^{t}SU:STA$	0.6	–	µs	3
Stop condition setup time	$^{t}SU:STO$	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Module Dimensions

Figure 3: 244-Pin DDR2 VLP Mini-RDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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