

# NCV4269C

## LDO Linear Regulator - Micropower, DELAY, Adjustable RESET, Sense Output

### 5.0 V, 150 mA

The NCV4269C is a 5.0 V precision micropower voltage regulator with an output current capability of 150 mA.

The output voltage is accurate within  $\pm 2.0\%$  with a maximum dropout voltage of 0.5 V at 100 mA. Low quiescent current is a feature drawing only 125  $\mu\text{A}$  with a 1.0 mA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active reset output RO with delay and a SI/SO monitor which can be used to provide an early warning signal to the microprocessor of a potential impending reset signal. The use of the SI/SO monitor allows the microprocessor to finish any signal processing before the reset shuts the microprocessor down.

The active Reset circuit operates correctly at an output voltage as low as 1.0 V. The Reset function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of an external resistor divider to the  $R_{\text{ADJ}}$  lead. The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

#### Features

- 5.0 V  $\pm 2.0\%$  Output
- Low 125  $\mu\text{A}$  Quiescent Current
- Active Reset Output Low Down to  $V_{\text{Q}} = 1.0$  V
- Adjustable Reset Threshold
- 150 mA Output Current Capability
- Fault Protection
  - ◆ +60 V Peak Transient Voltage
  - ◆ -40 V Reverse Voltage
  - ◆ Short Circuit
  - ◆ Thermal Overload
- Early Warning through SI/SO Leads
- Internally Fused Leads in SO-14 Package
- Integrated Pullup Resistor at Logic Outputs (To Use External Resistors, Select the NCV4279C)
- Very Low Dropout Voltage
- Electrical Parameters Guaranteed Over Entire Temperature Range
- AEC-Q100 Grade 1 Qualified and PPAP Capable
- These are Pb-Free Devices



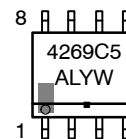
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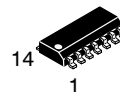
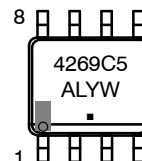
#### MARKING DIAGRAM



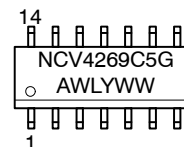
SO-8  
D1 SUFFIX  
CASE 751



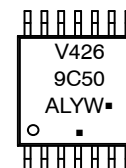
SO-8  
EXPOSED PAD  
PD SUFFIX  
CASE 751AC



SO-14  
D2 SUFFIX  
CASE 751A



TSSOP-14 EP  
PA SUFFIX  
CASE 948AW



A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G, ■ = Pb Free

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

# NCV4269C

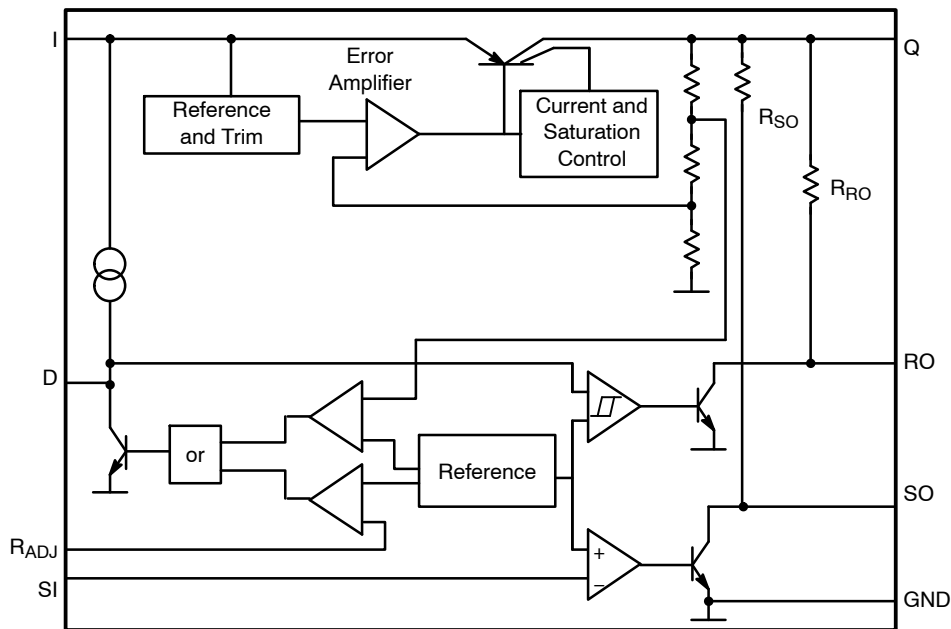
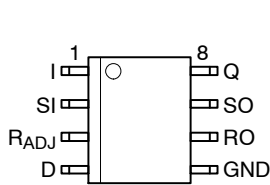
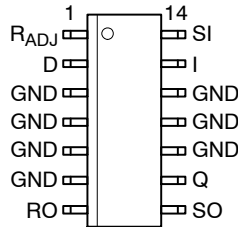


Figure 1. Block Diagram

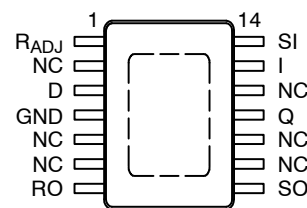
## PIN CONNECTIONS



SO-8



SO-14



TSSOP-14 EP

## PACKAGE PIN DESCRIPTION

Package Pin Number				Pin Symbol	Function
SO-8	SO-8 EP	SO-14	TSSOP14		
3	3	1	1	R <sub>ADJ</sub>	Reset Threshold Adjust; if not used to connect to GND.
4	4	2	3	D	Reset Delay; To Set Time Delay, Connect to GND with Capacitor
5	5	3, 4, 5, 6, 10, 11, 12	4	GND	Ground
-	-	-	2, 5, 6, 9, 10, 12	NC	No connection to these pins from the IC.
6	6	7	7	RO	Reset Output; The Open-Collector Output has a 20 kΩ Pullup Resistor to Q. Leave Open if Not Used.
7	7	8	8	SO	Sense Output; This Open-Collector Output is Internally Pulled Up by 20 kΩ pullup resistor to Q. If not used, keep open.
8	8	9	11	Q	5 V Output; Connect to GND with a 10 μF Capacitor, ESR < 2.5 Ω.
1	1	13	13	I	Input; Connect to GND Directly at the IC with Ceramic Capacitor.
2	2	14	14	SI	Sense Input; If not used, Connect to Q.
-	EPAD	-	EPAD	EPAD	Connect to ground potential or leave unconnected

# NCV4269C

## MAXIMUM RATINGS (T<sub>J</sub> = -40°C to 150°C)

Parameter	Symbol	Min	Max	Unit
Input to Regulator	V <sub>I</sub> I <sub>I</sub>	-40 Internally Limited	45 Internally Limited	V
Input Transient to Regulator (Note 3)	V <sub>I</sub>	-	60	V
Sense Input	V <sub>SI</sub> I <sub>SI</sub>	-40 -1	45 1	V mA
Reset Threshold Adjust	V <sub>RADJ</sub> I <sub>RADJ</sub>	-0.3 -10	7 10	V mA
Reset Delay	V <sub>D</sub> I <sub>D</sub>	-0.3 Internally Limited	7 Internally Limited	V
Ground	I <sub>q</sub>	50	-	mA
Reset Output	V <sub>RO</sub> I <sub>RO</sub>	-0.3 Internally Limited	7 Internally Limited	V
Sense Output	V <sub>SO</sub> I <sub>SO</sub>	-0.3 Internally Limited	7 Internally Limited	V
Regulated Output	V <sub>Q</sub> I <sub>Q</sub>	-0.5 -10	7 -	V mA
Junction Temperature	T <sub>J</sub>	-	150	°C
Storage Temperature	T <sub>STG</sub>	-50	150	°C
Input Voltage Operating Range	V <sub>I</sub>	-	45	V
Junction Temperature Operating Range	T <sub>J</sub>	-40	150	°C

## LEAD TEMPERATURE SOLDERING AND MSL

Parameter	Symbol	Value
MSL, 8-Lead, 14-Lead, LS Temperature 265°C Peak (Note 4)	MSL	1
MSL, 8-Lead EP, LS Temperature 260°C	MSL	2

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and exceeds the following ratings:

Human Body Model (HBM) ≤ 4.0 kV per AEC-Q100-002.

Machine Model (MM) ≤ 200 V per AEC-Q100-003.

2. Latchup tested per AEC-Q100-004.

3. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750-1.

4. +5°C/-0°C, 40 Sec Max-at-Peak, 60 - 150 Sec above 217°C.

## THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Values)	Unit
<b>SO-8 Package (Note 5)</b>		
Junction-to-Pin 6 (Ψ - JL6, Ψ <sub>L6</sub> )	58.3	°C/W
Junction-to-Ambient Thermal Resistance (R <sub>θJA</sub> , θ <sub>JA</sub> )	151.1	°C/W
<b>SO-8 EP Package (Note 5)</b>		
Junction-to-Pin 8 (Ψ - JL8, Ψ <sub>L8</sub> )	47	°C/W
Junction-to-Ambient Thermal Resistance (R <sub>θJA</sub> , θ <sub>JA</sub> )	131.6	°C/W
Junction-to-Pad (Ψ - JPad)	16.3	°C/W
<b>SO-14 Package (Note 5)</b>		
Junction-to-Pin 4 (Ψ - JL4, Ψ <sub>L4</sub> )	19.5	°C/W
Junction-to-Ambient Thermal Resistance (R <sub>θJA</sub> , θ <sub>JA</sub> )	100.9	°C/W
<b>TSSOP-14 EP Package (Note 5)</b>		
Junction-to-Pin 3 (Ψ - JL3, Ψ <sub>L3</sub> )	19.3	°C/W

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## THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Values)	Unit
<b>TSSOP-14 EP Package (Note 5)</b>		
Junction-to-Ambient Thermal Resistance ( $R_{\theta JA}$ , $\theta_{JA}$ )	77.3	°C/W
Junction-to-Pad ( $\Psi$ - JPad)	12.6	°C/W

5. 2 oz copper, 150 mm<sup>2</sup> copper area, 1.5 mm thick FR4

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## ELECTRICAL CHARACTERISTICS ( $T_J = -40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ , $V_I = 13.5\text{ V}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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### REGULATOR

Output Voltage	$V_Q$	$1\text{ mA} \leq I_Q \leq 100\text{ mA}$ $6\text{ V} \leq V_I \leq 16\text{ V}$	4.90	5.00	5.10	V
Current Limit	$I_Q$	-	150	430	500	mA
Current Consumption; $I_q = I_I - I_Q$	$I_q$	$I_Q = 1\text{ mA}$ , RO, SO High	-	125	250	$\mu\text{A}$
Current Consumption; $I_q = I_I - I_Q$	$I_q$	$I_Q = 10\text{ mA}$ , RO, SO High	-	230	450	$\mu\text{A}$
Current Consumption; $I_q = I_I - I_Q$	$I_q$	$I_Q = 50\text{ mA}$ , RO, SO High	-	0.9	3.0	mA
Dropout Voltage	$V_{dr}$	$V_I = 5\text{ V}$ , $I_Q = 100\text{ mA}$	-	0.23	0.5	V
Load Regulation	$\Delta V_Q$	$I_Q = 5\text{ mA}$ to $100\text{ mA}$	-	1	20	mV
Line Regulation	$\Delta V_Q$	$V_I = 6\text{ V}$ to $26\text{ V}$ $I_Q = 1\text{ mA}$	-	1	30	mV

### RESET GENERATOR

Reset Switching Threshold	$V_{RT}$	-	4.50	4.65	4.80	V
Reset Adjust Switching Threshold	$V_{RADJ,TH}$	$V_Q > 3.5\text{ V}$	1.26	1.35	1.44	V
Reset Pullup Resistance	$R_{RO,INT}$	-	10	20	40	k $\Omega$
Reset Output Saturation Voltage	$V_{RO,SAT}$	$V_Q < V_{RT}$ , $R_{RO,INT}$	-	0.03	0.4	V
Upper Delay Switching Threshold	$V_{UD}$	-	1.4	1.8	2.2	V
Lower Delay Switching Threshold	$V_{LD}$	-	0.3	0.45	0.60	V
Saturation Voltage on Delay Capacitor	$V_{D,SAT}$	$V_Q < V_{RT}$	-	-	0.1	V
Charge Current	$I_{D,C}$	$V_D = 1\text{ V}$	3.0	6.5	9.5	$\mu\text{A}$
Delay Time L $\rightarrow$ H	$t_d$	$C_D = 100\text{ nF}$	17	28	73	ms
Delay Time H $\rightarrow$ L	$t_{RR}$	$C_D = 100\text{ nF}$	-	1.5	-	$\mu\text{s}$

### INPUT VOLTAGE SENSE

Sense Threshold High	$V_{SI,High}$	-	1.24	1.31	1.38	V
Sense Threshold Low	$V_{SI,Low}$	-	1.16	1.20	1.28	V
Sense Output Saturation Voltage	$V_{SO,Low}$	$V_{SI} < 1.20\text{ V}$ ; $V_Q > 3\text{ V}$ ; $R_{SO,INT}$	-	0.03	0.4	V
Sense Resistor Pullup	$R_{SO,INT}$	-	10	20	40	k $\Omega$
Sense Input Current	$I_{SI}$	-	-1.0	0.1	1.0	$\mu\text{A}$

### THERMAL SHUTDOWN

Thermal Shutdown Temperature (Note 6)	$T_{SD}$	$I_{out} = 1\text{ mA}$	150	-	200	$^{\circ}\text{C}$
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Values based on design and/or characterization.

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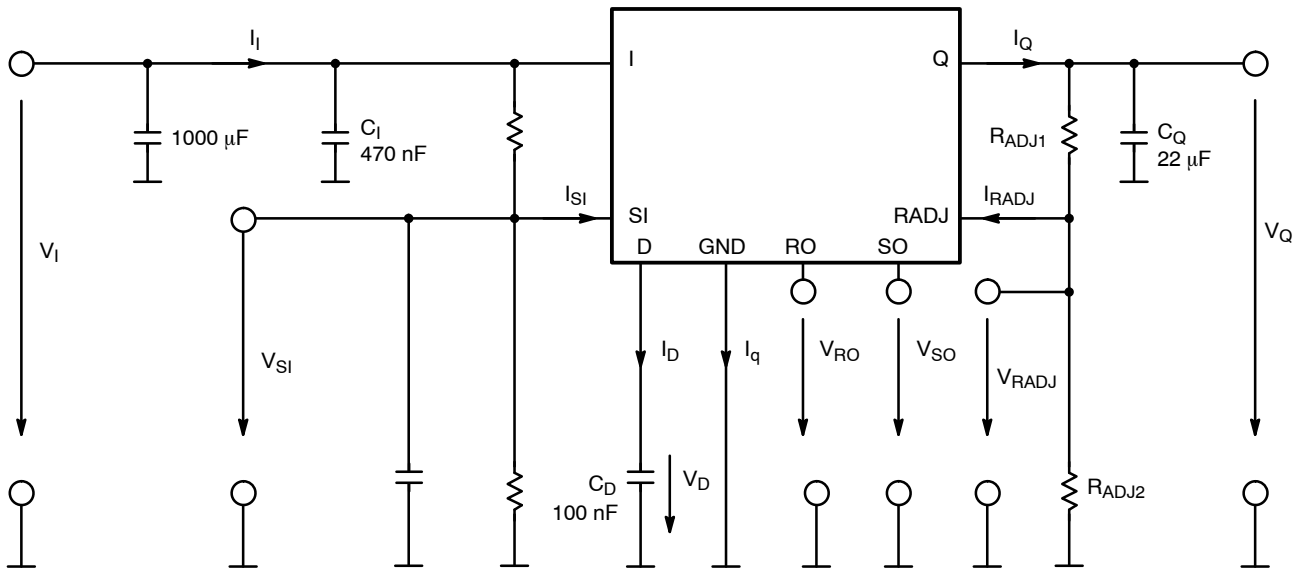


Figure 2. Measuring Circuit

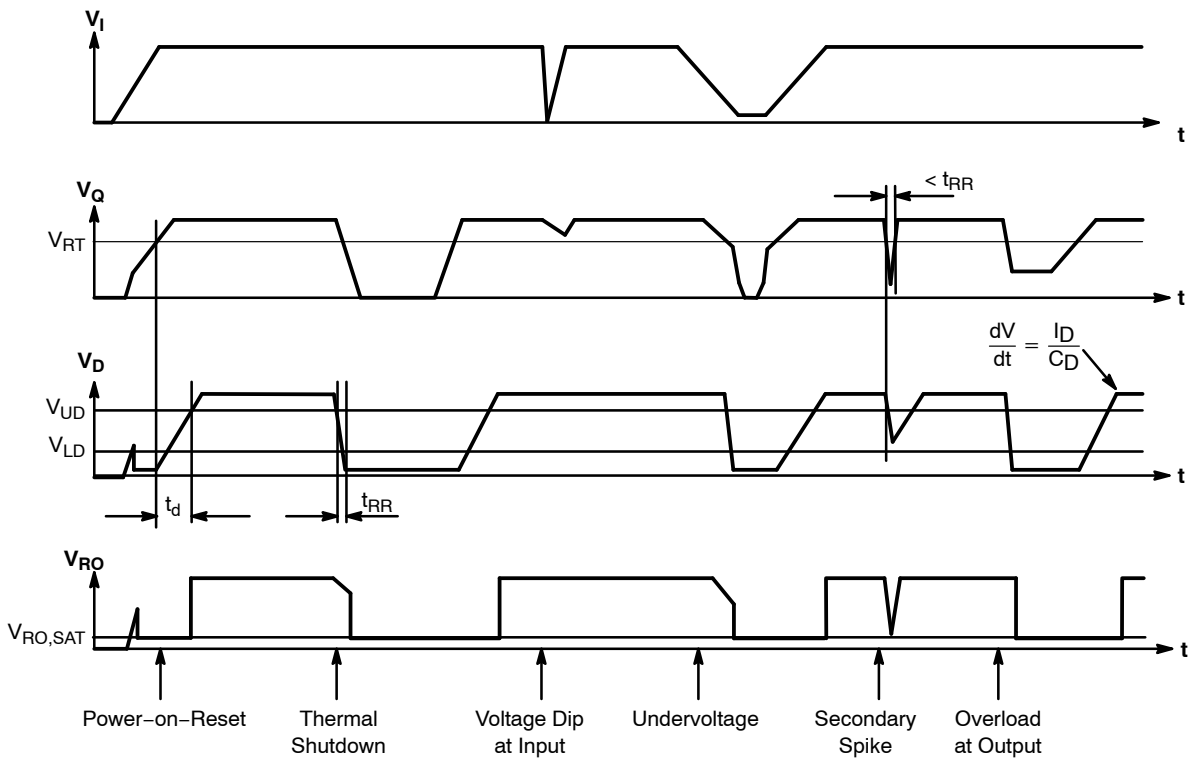


Figure 3. Reset Timing Diagram

# NCV4269C

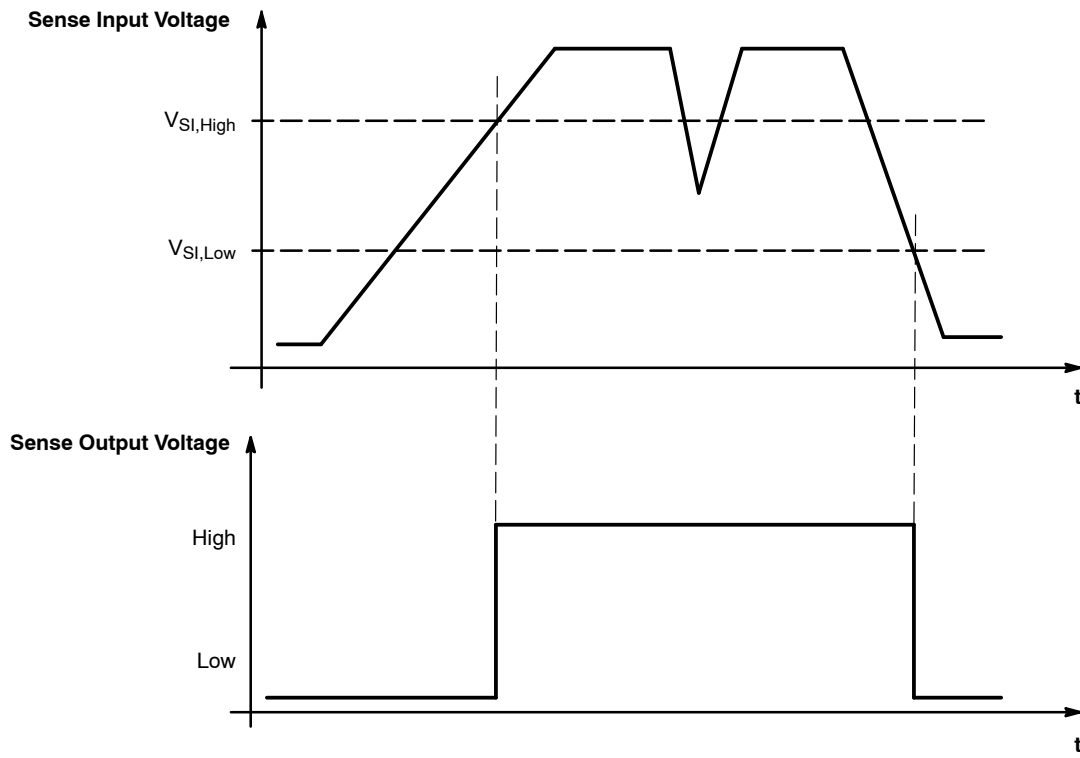


Figure 4. Sense Timing Diagram

## TYPICAL PERFORMANCE CHARACTERISTICS

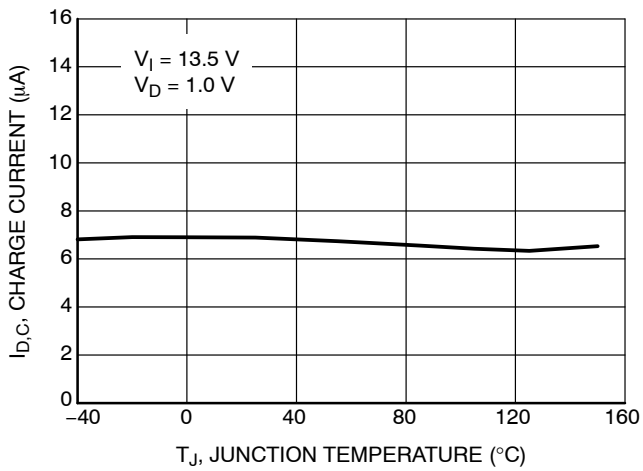


Figure 5. Charge Current  $I_{D,C}$  vs. Temperature  $T_J$

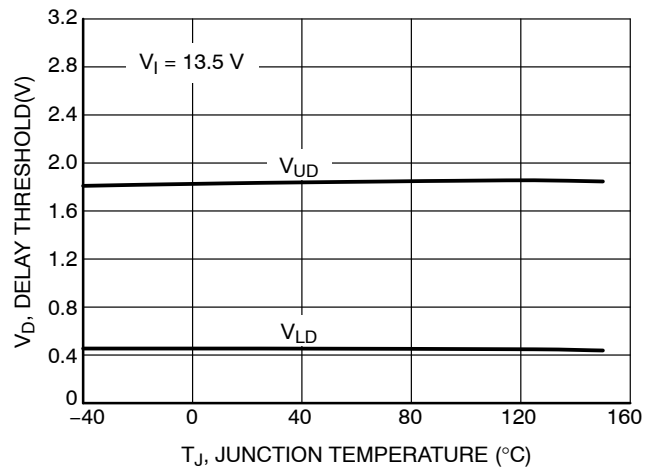


Figure 6. Switching Voltage  $V_{UD}$  and  $V_{LD}$  vs. Temperature  $T_J$

TYPICAL PERFORMANCE CHARACTERISTICS

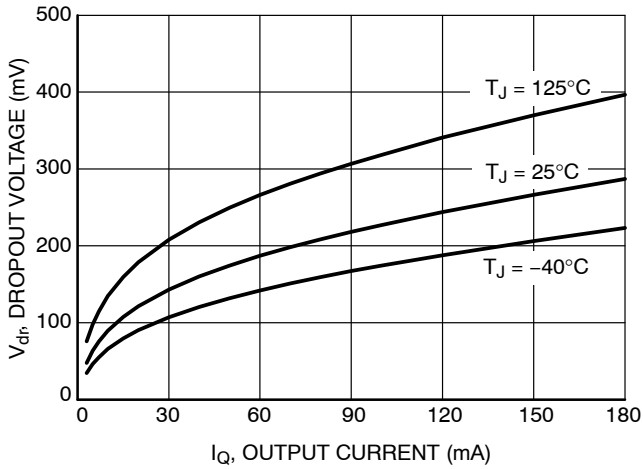


Figure 7. Drop Voltage  $V_{dr}$  vs. Output Current  $I_Q$

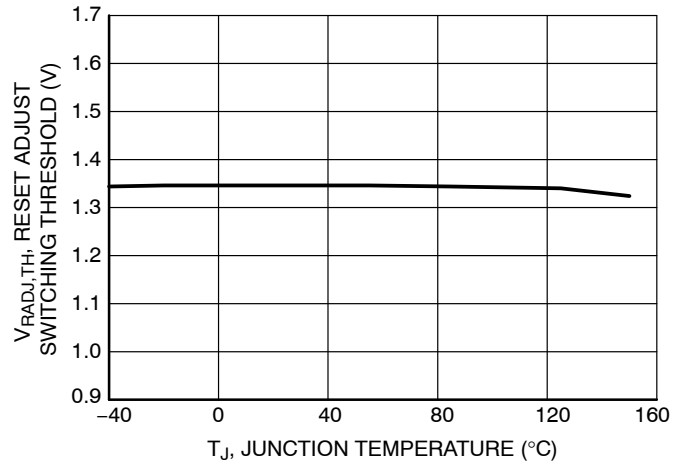


Figure 8. Reset Adjust Switching Threshold,  $V_{RADJ,TH}$  vs. Temperature  $T_J$

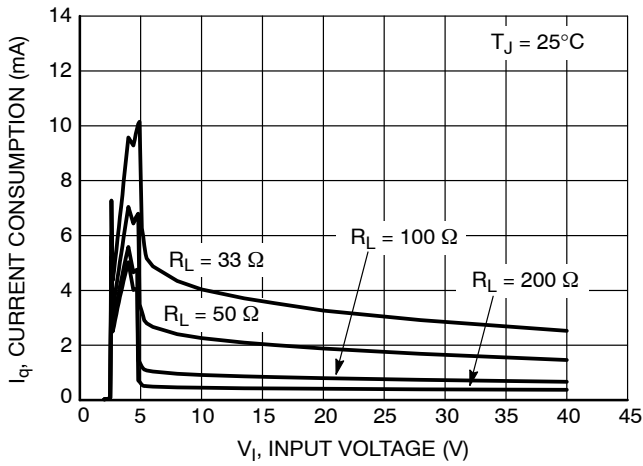


Figure 9. Current Consumption  $I_q$  vs. Input Voltage  $V_I$

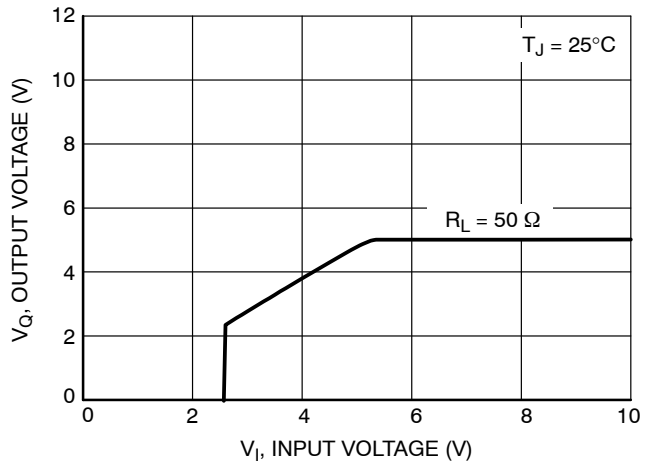


Figure 10. Output Voltage  $V_Q$  vs. Input Voltage  $V_I$

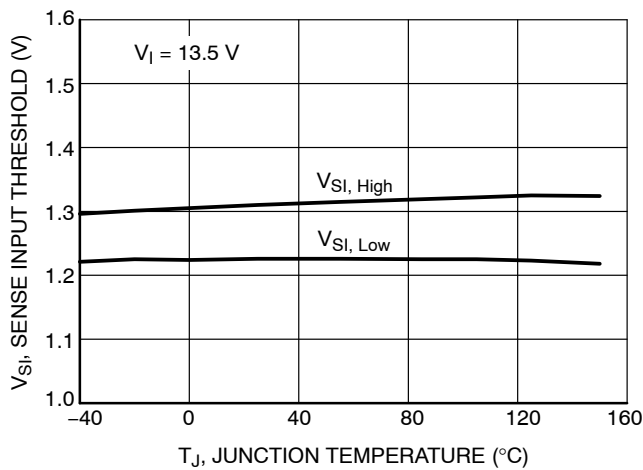


Figure 11. Sense Threshold  $V_{Sl}$  vs. Temperature  $T_J$

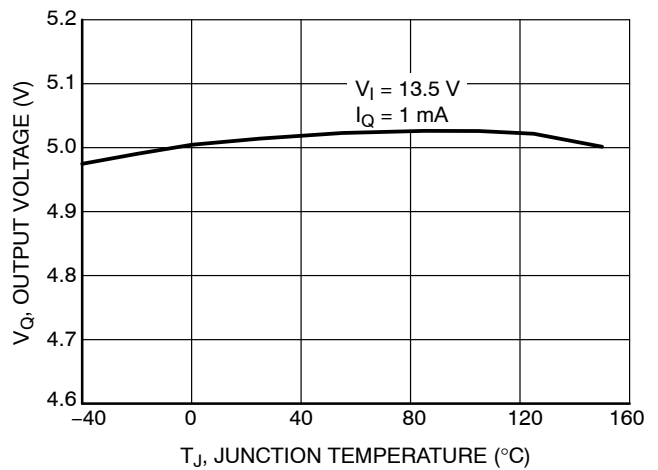


Figure 12. Output Voltage  $V_Q$  vs. Temperature  $T_J$



TYPICAL PERFORMANCE CHARACTERISTICS

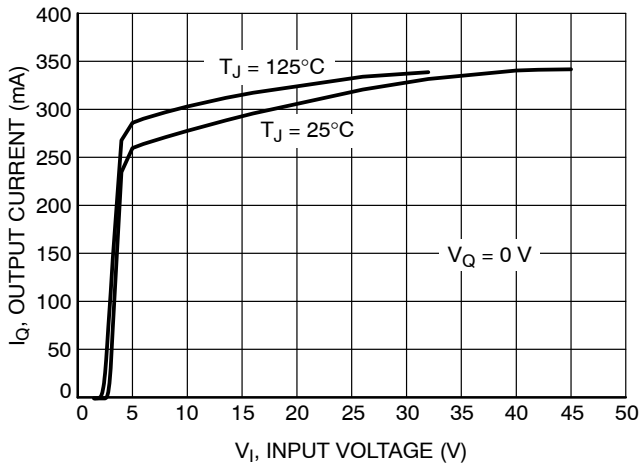


Figure 13. Output Current  $I_Q$  vs. Input Voltage  $V_I$

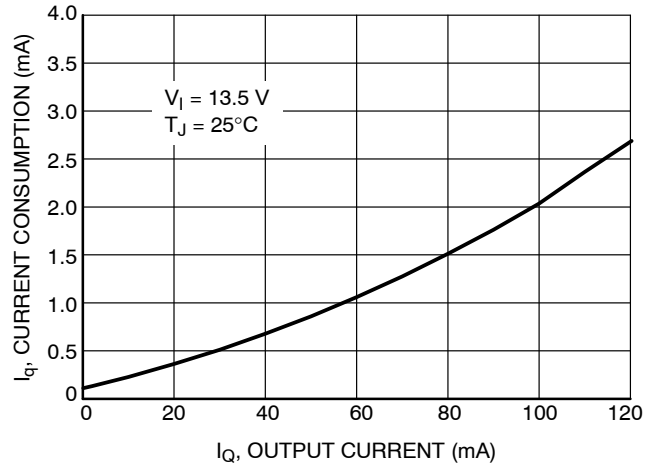


Figure 14. Current Consumption  $I_q$  vs. Output Current  $I_Q$

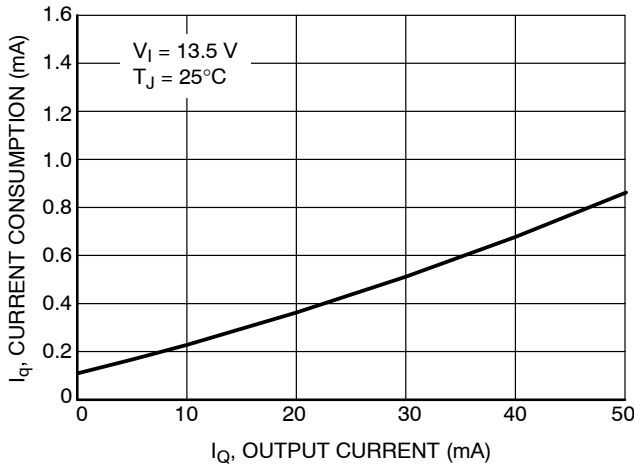


Figure 15. Current Consumption  $I_q$  vs. Output Current  $I_Q$

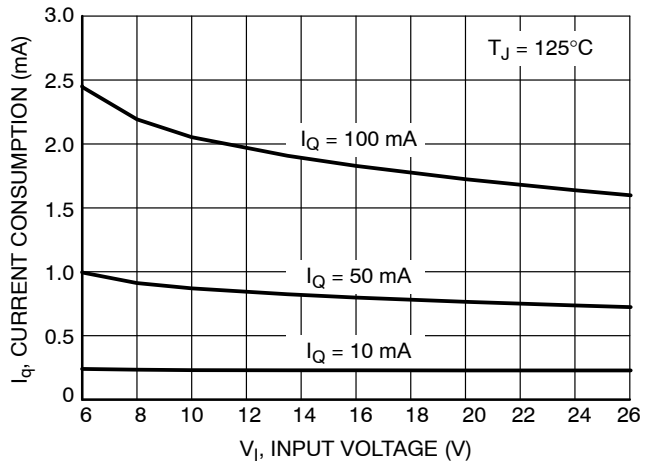


Figure 16. Quiescent Current  $I_q$  vs. Input Voltage  $V_I$

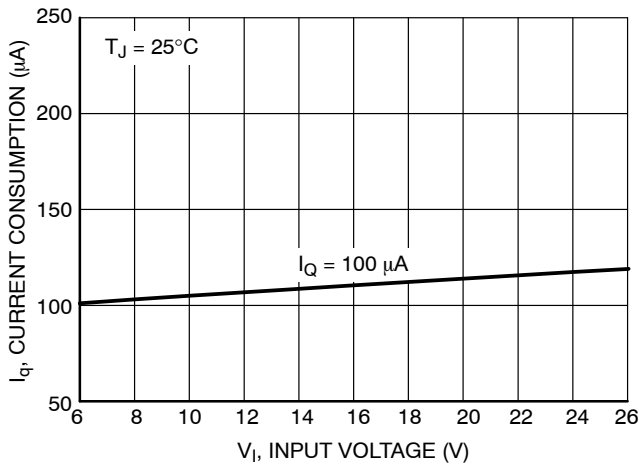


Figure 17. Quiescent Current  $I_q$  vs. Input Voltage  $V_I$

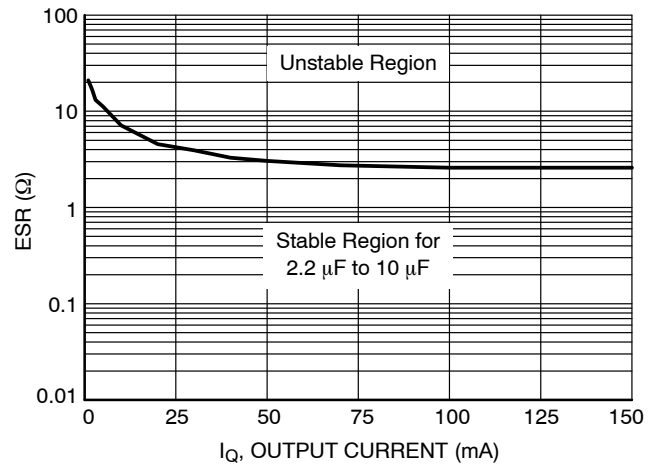


Figure 18. Output Stability, Capacitance ESR vs. Output Load Current

# NCV4269C

## TYPICAL THERMAL CHARACTERISTICS

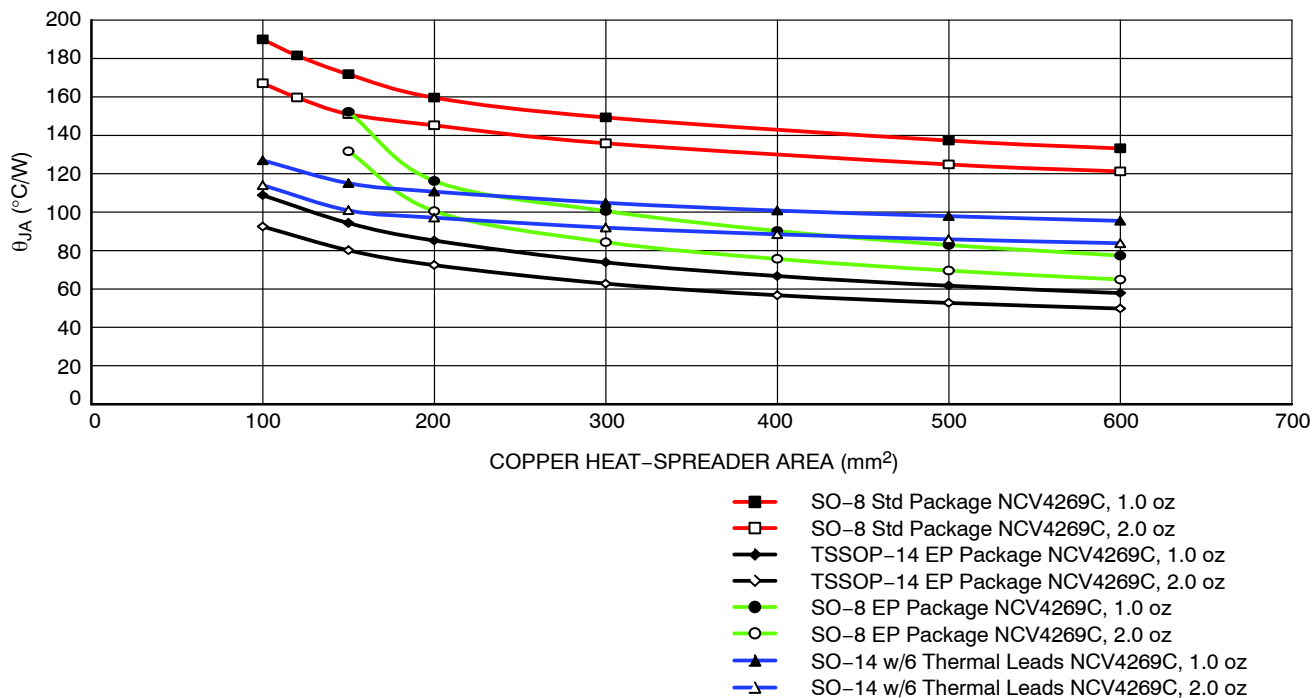


Figure 19. Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) vs. Heat Spreader Area

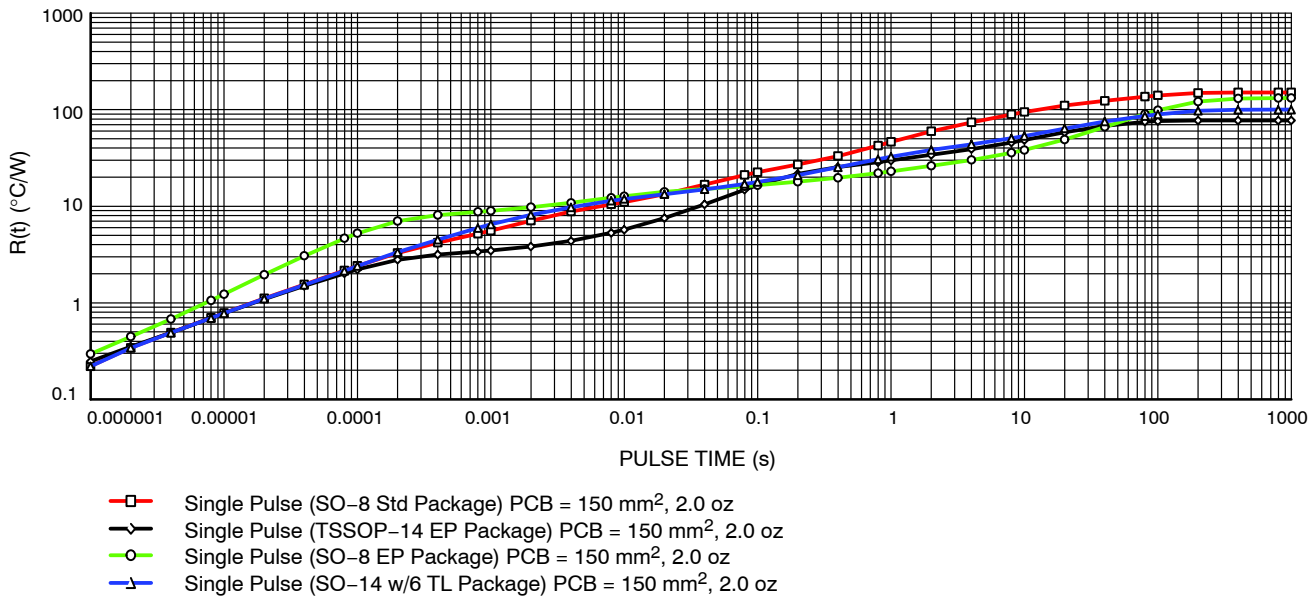


Figure 20.  $R(t)$  vs. Pulse Time

APPLICATION DESCRIPTION

OUTPUT REGULATOR

The output is controlled by a precision trimmed reference. The PNP output has base drive quiescent current control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

RESET OUTPUT (RO)

A reset signal, Reset Output, RO, (low voltage) is generated as the IC powers up. After the output voltage  $V_Q$  increases above the reset threshold voltage  $V_{RT}$ , the delay timer D is started. When the voltage on the delay timer  $V_D$  passes  $V_{UD}$ , the reset signal RO goes high. A discharge of the delay timer  $V_D$  is started when  $V_Q$  drops and stays below the reset threshold voltage  $V_{RT}$ . When the voltage of the delay timer  $V_D$  drops below the lower threshold voltage  $V_{LD}$  the reset output voltage  $V_{RO}$  is brought low to reset the processor.

The reset output RO is an open collector NPN transistor with an internal 20 kΩ pullup resistor connected to the output Q, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that RO is valid for  $V_Q$  as low as 1.0 V.

RESET ADJUST ( $R_{ADJ}$ )

The reset threshold  $V_{RT}$  can be decreased from a typical value of 4.65 V to as low as 3.5 V by using an external voltage divider connected from the Q lead to the pin  $R_{ADJ}$ , as shown in Figure 21. The resistor divider keeps the voltage above the  $V_{RADJ,TH}$  (typical 1.35 V) for the desired input voltages, and overrides the internal threshold detector. Adjust the voltage divider according to the following relationship:

$$V_{RT} = V_{RADJ,TH} \cdot (R_{ADJ1} + R_{ADJ2}) / R_{ADJ2} \quad (\text{eq. 1})$$

If the reset adjust option is not needed, the  $R_{ADJ}$  pin should be connected to GND causing the reset threshold to go to its default value (typically 4.65 V).

RESET DELAY (D)

The reset delay circuit provides a delay (programmable by capacitor  $C_D$ ) on the reset output lead RO. The delay lead D provides charge current  $I_{D,C}$  (typically 6.5  $\mu\text{A}$ ) to the external delay capacitor  $C_D$  during the following times:

1. During Powerup (once the regulation threshold has been exceeded).
2. After a reset event has occurred and the device is back in regulation. The delay capacitor is set to discharge when the regulation ( $V_{RT}$ , reset threshold voltage) has been violated. When the delay capacitor discharges to  $V_{LD}$ , the reset signal RO pulls low.

SETTING THE DELAY TIME

The delay time is set by the delay capacitor  $C_D$  and the charge current  $I_D$ . The time is measured by the delay capacitor voltage charging from the low level of  $V_{DSAT}$  to the higher level  $V_{UD}$ . The time delay follows the equation:

$$t_d = [C_D (V_{UD} - V_{D,SAT})] / I_{D,C} \quad (\text{eq. 2})$$

Example:

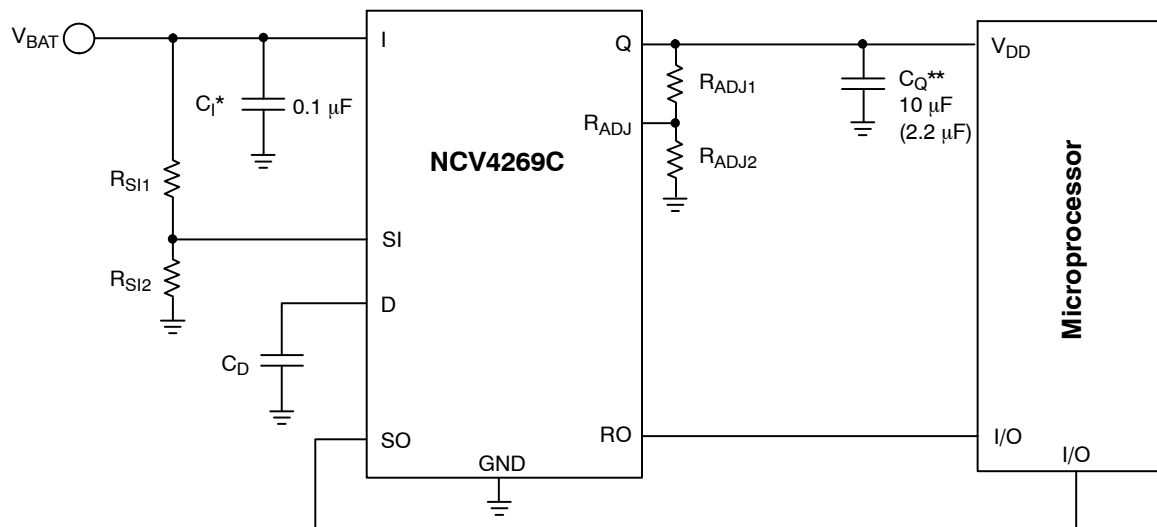
Using  $C_D = 100 \text{ nF}$ .

Use the typical value for  $V_{D,SAT} = 0.1 \text{ V}$ .

Use the typical value for  $V_{UD} = 1.8 \text{ V}$ .

Use the typical value for Delay Charge Current  $I_D = 6.5 \mu\text{A}$ .

$$t_d = [100 \text{ nF} (1.8 - 0.1 \text{ V})] / 6.5 \mu\text{A} = 26.2 \text{ ms} \quad (\text{eq. 3})$$



\* $C_1$  required if regulator is located far from the power supply filter.

\*\*  $C_Q$  - minimum cap required for stability is 2.2  $\mu\text{F}$  while higher over/under-shoots may be expected. Cap must operate at minimum temperature expected.

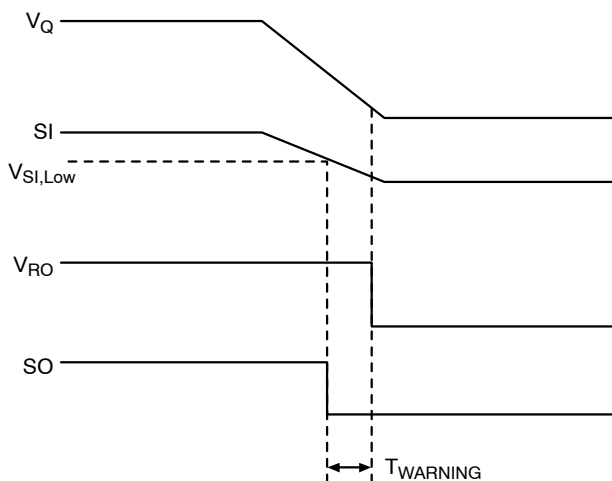
Figure 21. Application Diagram

**SENSE INPUT (SI) / SENSE OUTPUT (SO) VOLTAGE MONITOR**

An on-chip comparator is available to provide early warning to the microprocessor of a possible reset signal (Figure 4). The output is from an open collector driver with an internal 20 kΩ pull up resistor to output Q. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor SI (Figure 21). The values for R<sub>SI1</sub> and R<sub>SI2</sub> are selected for a typical threshold of 1.20 V on the SI Pin.

**SIGNAL OUTPUT**

Figure 22 shows the SO Monitor timing waveforms as a result of the circuit depicted in Figure 21. As the output voltage (V<sub>Q</sub>) falls, the monitor threshold (V<sub>SI,Low</sub>), is crossed. This causes the voltage on the SO output to go low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. T<sub>WARNING</sub> is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal. When the voltage on the SO goes low and the RO stays high the current consumption is typically 530 μA at 1 mA load current.



**Figure 22. SO Warning Waveform Time Diagram**

**STABILITY CONSIDERATIONS**

The input capacitor C<sub>1</sub> in Figure 21 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1.0 Ω in series with C<sub>1</sub>.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures

(–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer’s data sheet usually provides this information.

The 10 μF output capacitor C<sub>O</sub> shown in Figure 21 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at C<sub>O</sub> is min 2.2 μF and max ESR is 2.5 Ω. There is no min ESR limit which was proved with MURATA’s ceramic caps GRM31MR71A225KA01 (2.2 μF, 10 V, X7R, 1206) and GRM31CR71A106KA01 (10 μF, 10 V, X7R, 1206) directly soldered between output and ground pins.

**CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR**

The maximum power dissipation for a single output regulator (Figure 21) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad (\text{eq. 4})$$

where:

V<sub>I(max)</sub> is the maximum input voltage,

V<sub>Q(min)</sub> is the minimum output voltage,

I<sub>Q(max)</sub> is the maximum output current for the application,

and I<sub>q</sub> is the quiescent current the regulator consumes at I<sub>Q(max)</sub>.

Once the value of P<sub>D(max)</sub> is known, the maximum permissible value of R<sub>θJA</sub> can be calculated:

$$R_{\theta JA} = (150^{\circ}\text{C} - T_A) / P_D \quad (\text{eq. 5})$$

The value of R<sub>θJA</sub> can then be compared with those in the package section of the data sheet. Those packages with R<sub>θJA</sub>’s less than the calculated value in equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

**HEATSINKS**

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of R<sub>θJA</sub>:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (\text{eq. 6})$$

where:

R<sub>θJC</sub> = the junction-to-case thermal resistance,

R<sub>θCS</sub> = the case-to-heat sink thermal resistance, and

R<sub>θSA</sub> = the heat sink-to-ambient thermal resistance.

R<sub>θJC</sub> appears in the package section of the data sheet. Like R<sub>θJA</sub>, it too is a function of package type. R<sub>θCS</sub> and R<sub>θSA</sub> are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers. Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor website.

# NCV4269C

## ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV4269CD150R2G	5.0 V	SO-8 (Pb-Free)	2500 / Tape & Reel
NCV4269CPD50R2G		SO-8 EP (Pb-Free)	2500 / Tape & Reel
NCV4269CD250R2G		SO-14 (Pb-Free)	2500 / Tape & Reel
NCV4269CPA50R2G		TSSOP-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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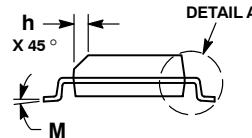
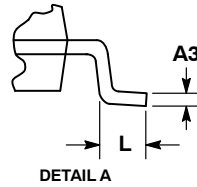
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

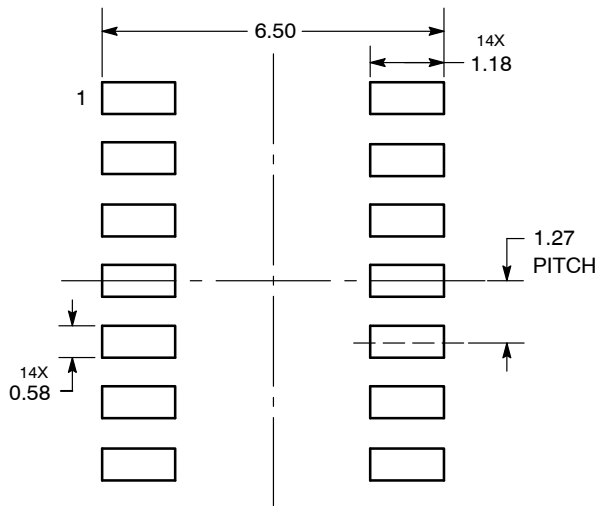
DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

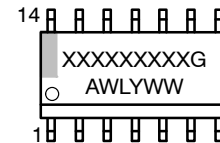
### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

### STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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<b>DESCRIPTION:</b>	<b>SOIC-14 NB</b>	<b>PAGE 2 OF 2</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



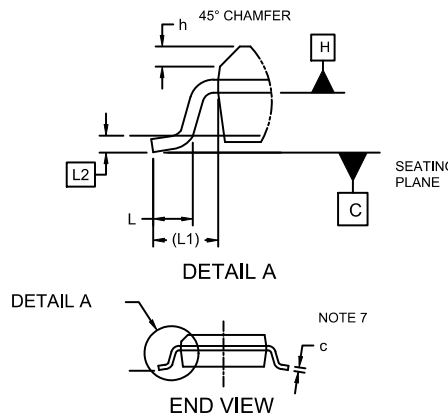
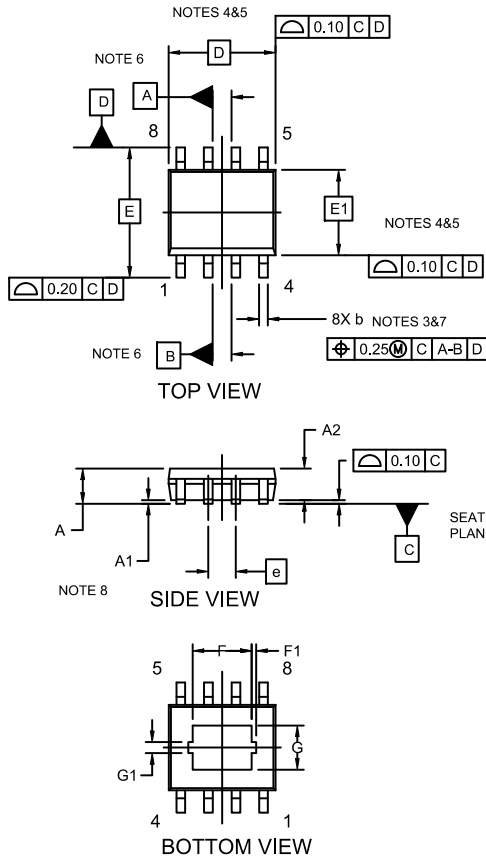
SCALE 1:1

## SOIC-8 EP CASE 751AC ISSUE E

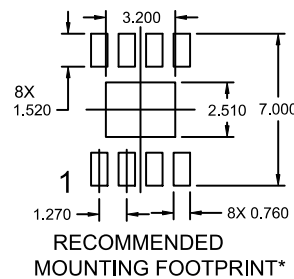
DATE 05 OCT 2022

### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
- DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
- A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

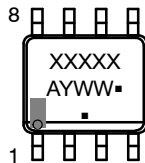


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.20 REF		
G	1.55	2.03	2.51
G1	0.46 REF		
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
∅	0°	4°	8°



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

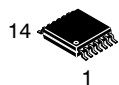
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOIC-8 EP	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

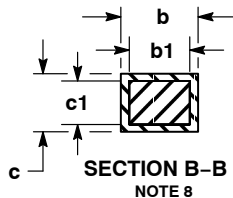
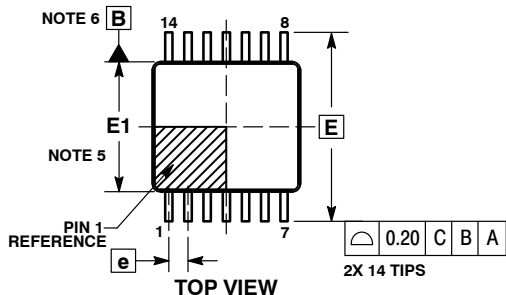
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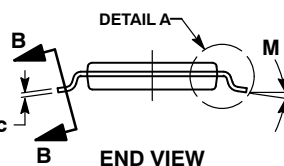
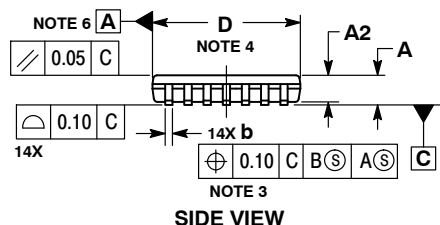
SCALE 1:1

## TSSOP-14 EP CASE 948AW ISSUE C

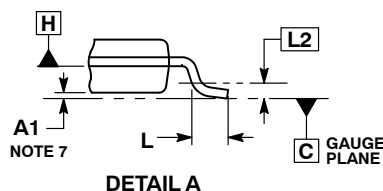
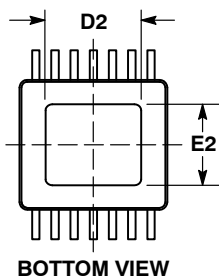
DATE 09 OCT 2012



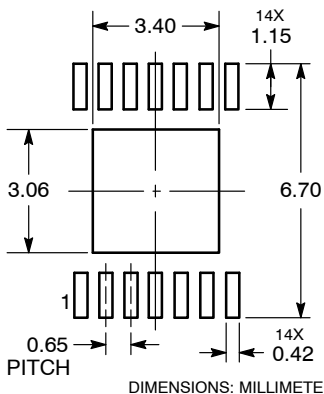
- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  - CONTROLLING DIMENSION: MILLIMETERS.
  - DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADII OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
  - DIMENSION *D* DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *D* IS DETERMINED AT DATUM H.
  - DIMENSION *E1* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION *E1* IS DETERMINED AT DATUM H.
  - DATUMS A AND B ARE DETERMINED AT DATUM H.
  - A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
  - SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.



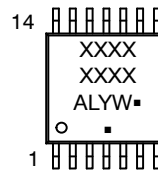
MILLIMETERS		
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
A2	0.80	1.05
<i>b</i>	0.19	0.30
<i>b1</i>	0.19	0.25
<i>c</i>	0.09	0.20
<i>c1</i>	0.09	0.16
<i>D</i>	4.90	5.10
<i>D2</i>	3.09	3.62
<i>E</i>	6.40 BSC	
<i>E1</i>	4.30	4.50
<i>E2</i>	2.69	3.22
<i>e</i>	0.65 BSC	
<i>L</i>	0.45	0.75
<i>L2</i>	0.25 BSC	
<i>M</i>	0°	8°



### RECOMMENDED SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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