

NTB5426N, NTP5426N, NVB5426N



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Power MOSFET 120 Amps, 60 Volts N-Channel D²PAK, TO-220

Features

- Low $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- AEC Q101 Qualified – NVB5426N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	60	V	
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V	
Gate-to-Source Voltage – Nonrepetitive ($T_P < 10 \mu\text{s}$)	V_{GS}	30	V	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	I_D 120	A
		$T_C = 100^\circ\text{C}$	85	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D 215	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM} 260	A	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	60	A	
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 V_{dc}, V_{GS} = 10 V_{dc}, I_{L(pk)} = 70 \text{ A}, L = 0.3 \text{ mH}, R_G = 25 \Omega$)	E_{AS}	735	mJ	
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$	

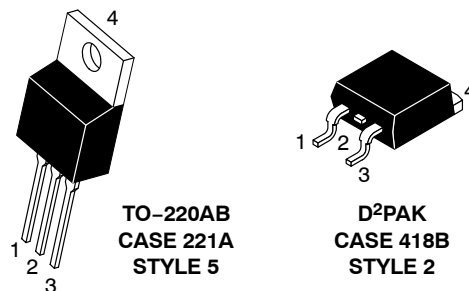
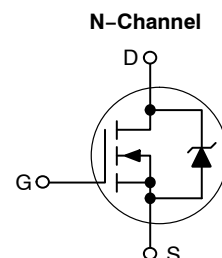
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State (Note 1)	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

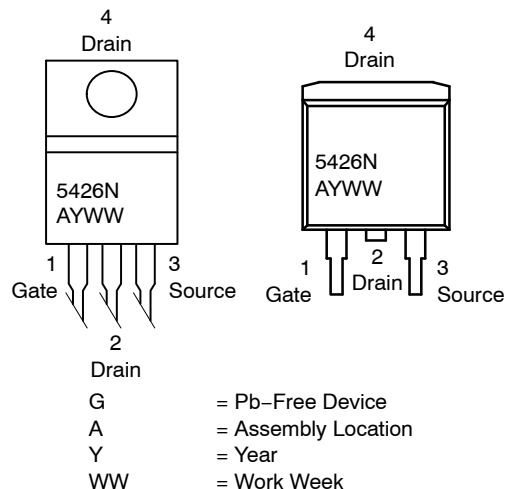
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$ (Note 1)
60 V	6.0 m Ω @ 10 V	120 A



MARKING DIAGRAMS & PIN ASSIGNMENTS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			64		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 150^\circ\text{C}$		25	
Gate-Body Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0	3.1	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$			9.2		mV/°C
Drain-to-Source On Voltage	$V_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		0.3	0.36	V
		$V_{GS} = 10\text{ V}, I_D = 60\text{ A}, 150^\circ\text{C}$		0.6		
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		4.9	6.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		65		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		5800		pF
Output Capacitance	C_{oss}			1000		
Transfer Capacitance	C_{rss}			370		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 60\text{ A}$		150	170	nC
Threshold Gate Charge	$Q_{G(TH)}$			6.0		
Gate-to-Source Charge	Q_{GS}			28		
Gate-to-Drain Charge	Q_{GD}			67		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 48\text{ V},$ $I_D = 60\text{ A}, R_G = 3.0\ \Omega$		15		ns
Rise Time	t_r			100		
Turn-Off Delay Time	$t_{d(off)}$			105		
Fall Time	t_f			95		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}$ $I_S = 60\text{ A}$	$T_J = 25^\circ\text{C}$		0.88	1.1	V_{dc}
			$T_J = 100^\circ\text{C}$		0.78		
Reverse Recovery Time	t_{rr}	$I_S = 60\text{ A}_{dc}, V_{GS} = 0\text{ V}_{dc},$ $di_S/dt = 100\text{ A}/\mu\text{s}$			75		ns
Charge Time	t_a				50		
Discharge Time	t_b				25		
Reverse Recovery Stored Charge	Q_{RR}				235		

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTP5426N	TO-220AB (Pb-Free)	50 Units / Rail
NTB5426NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NVB5426NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

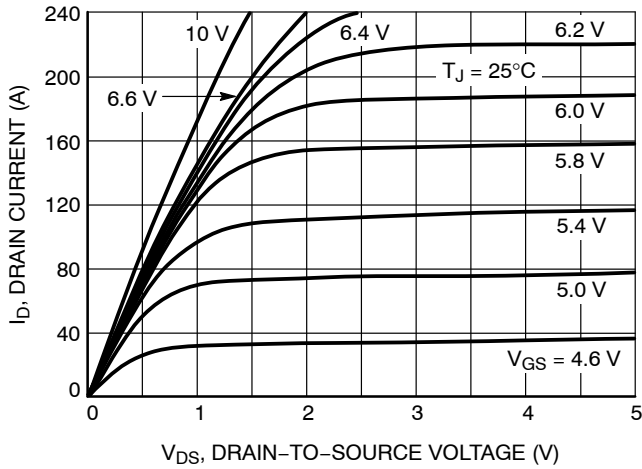


Figure 1. On-Region Characteristics

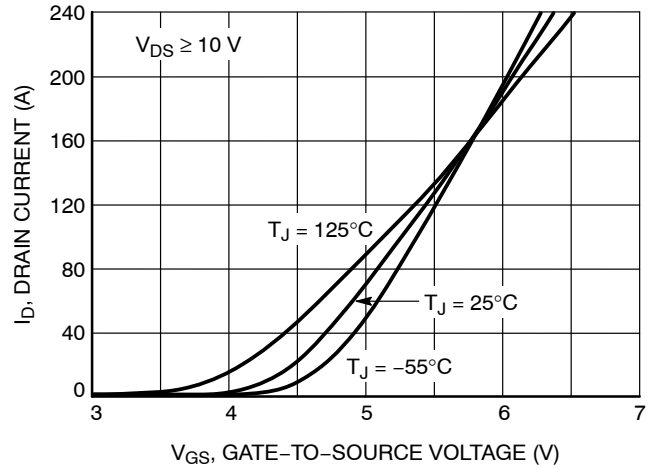


Figure 2. Transfer Characteristics

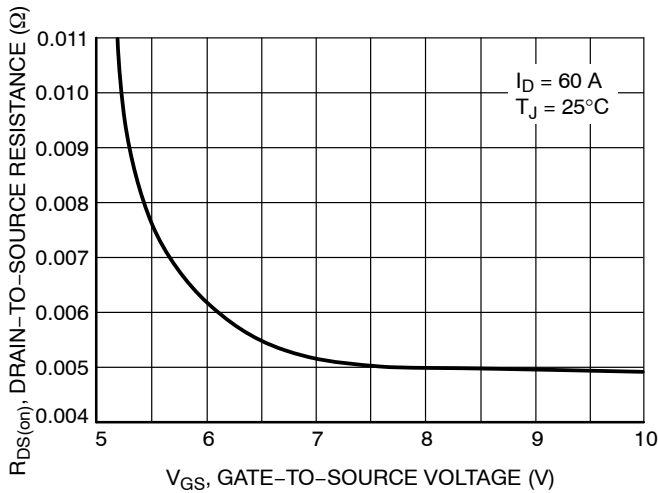


Figure 3. On-Resistance vs. Gate Voltage

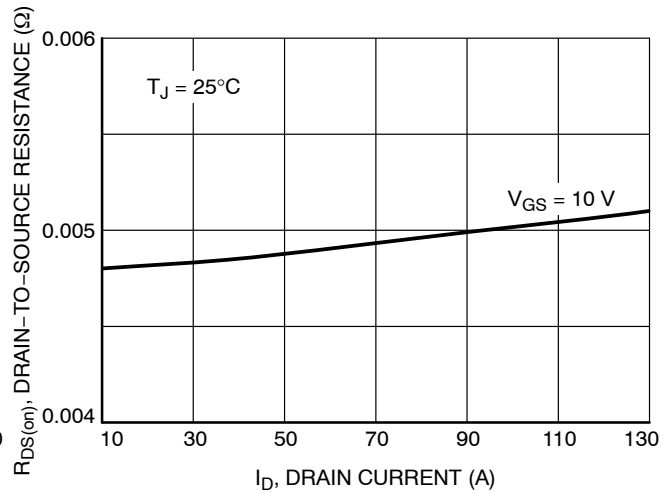


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

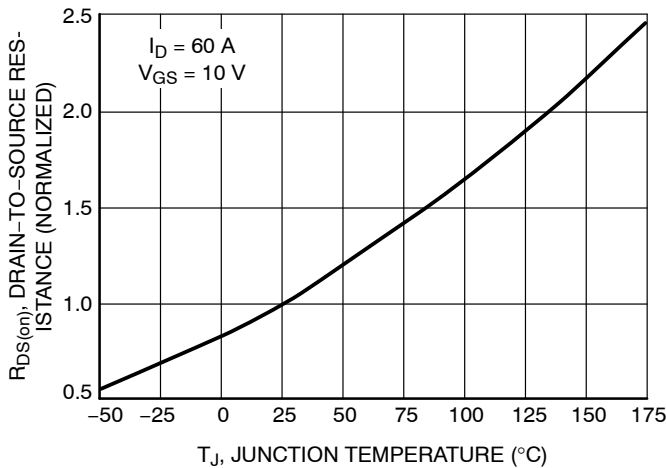


Figure 5. On-Resistance Variation with Temperature

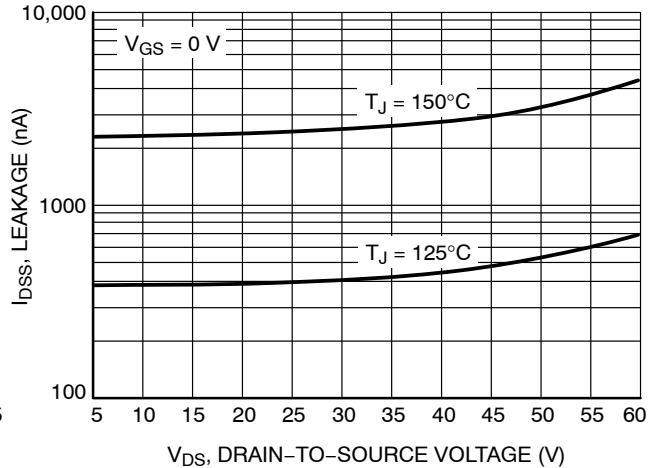


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

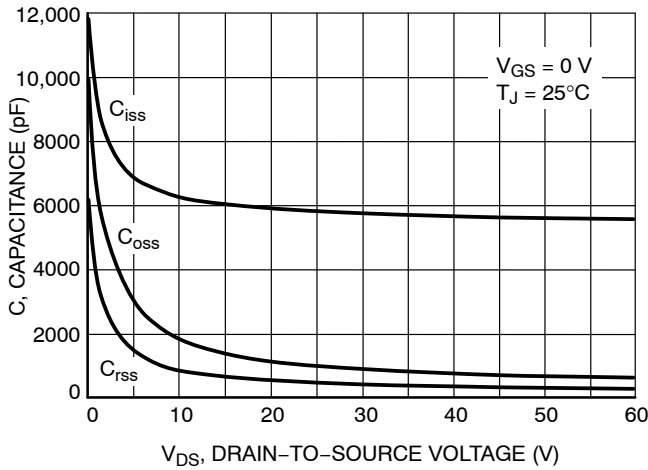


Figure 7. Capacitance Variation

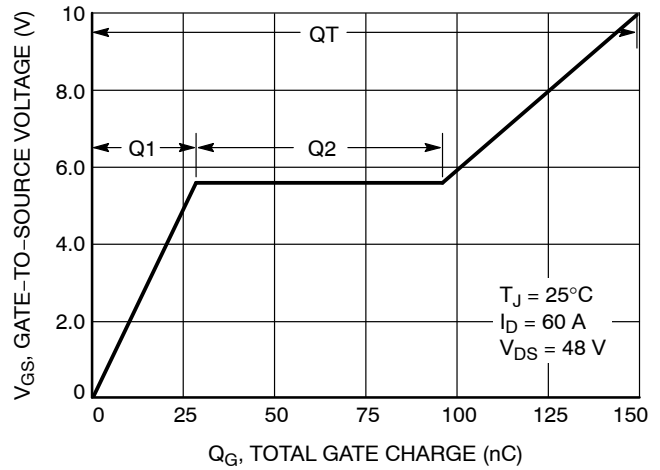


Figure 8. Gate-to-Source Voltage vs. Total Charge

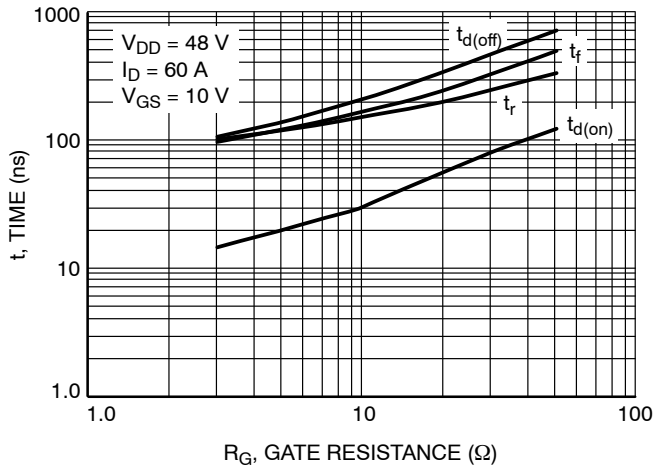


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

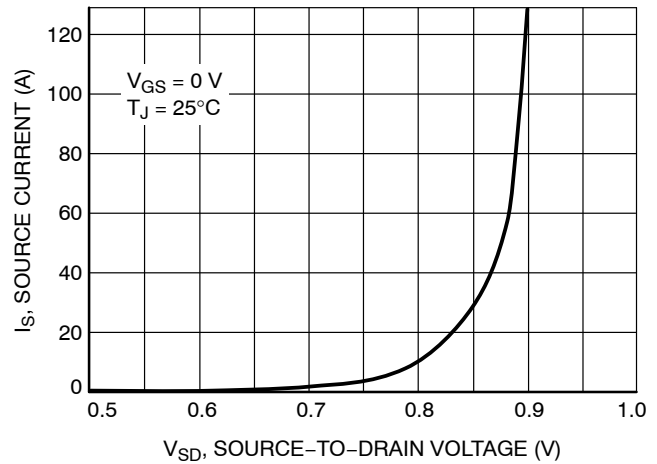


Figure 10. Diode Forward Voltage vs. Current

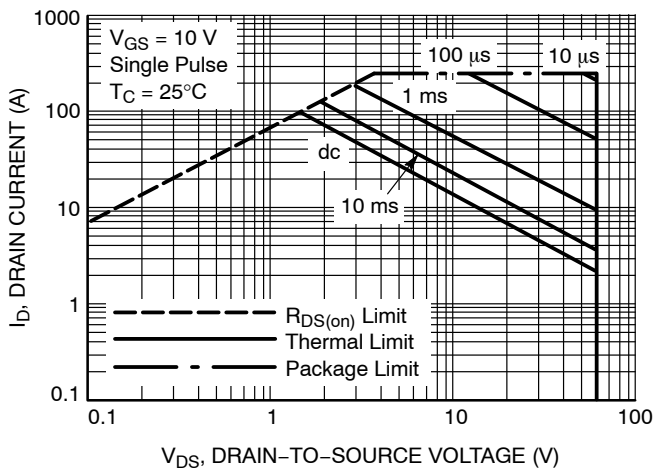


Figure 11. Maximum Rated Forward Biased Safe Operating Area

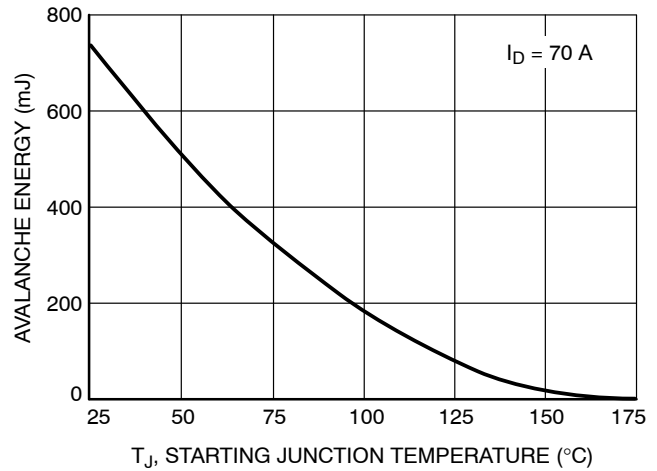


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL CHARACTERISTICS

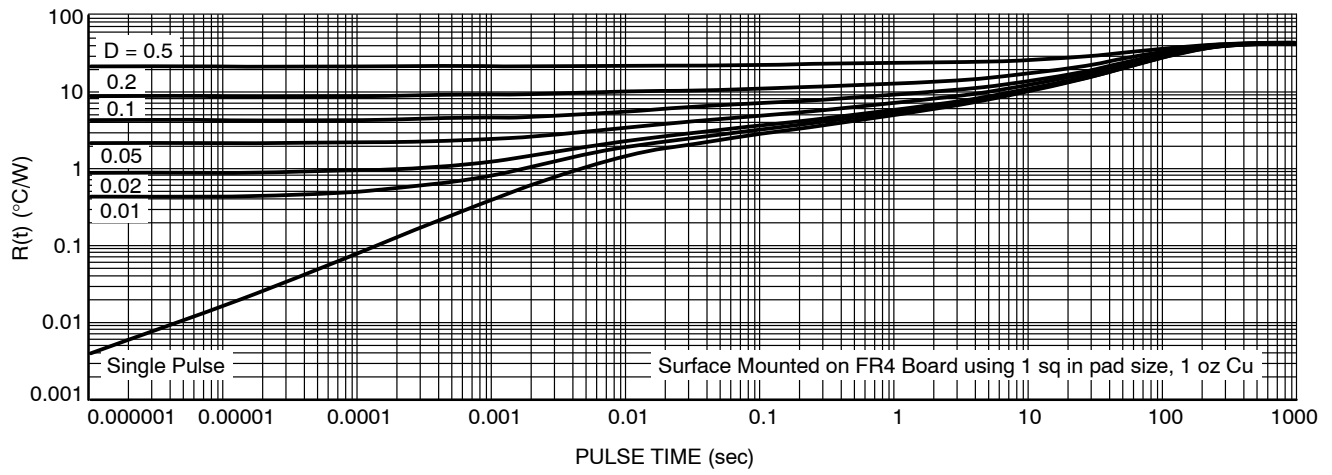
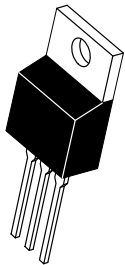
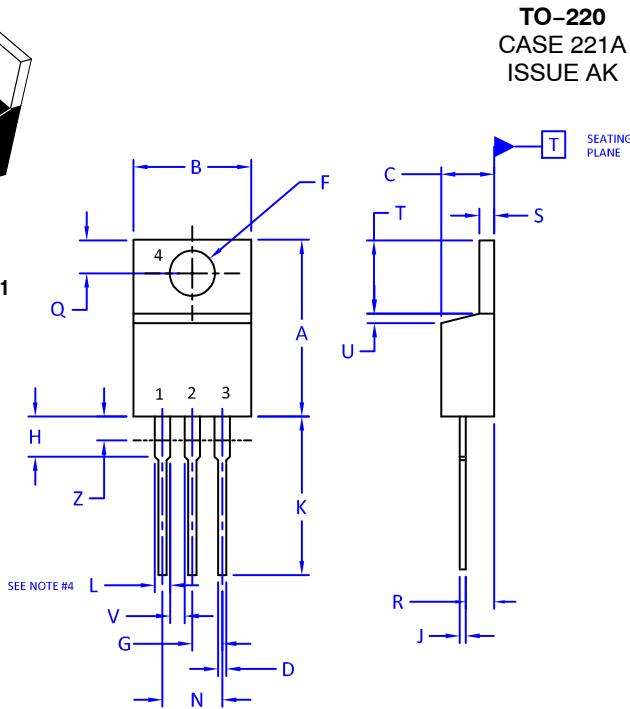


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1



TO-220
CASE 221A
ISSUE AK

DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

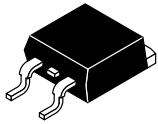
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

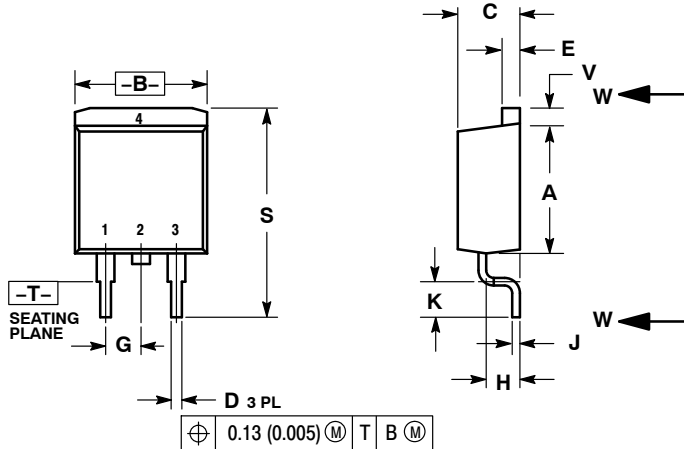
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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

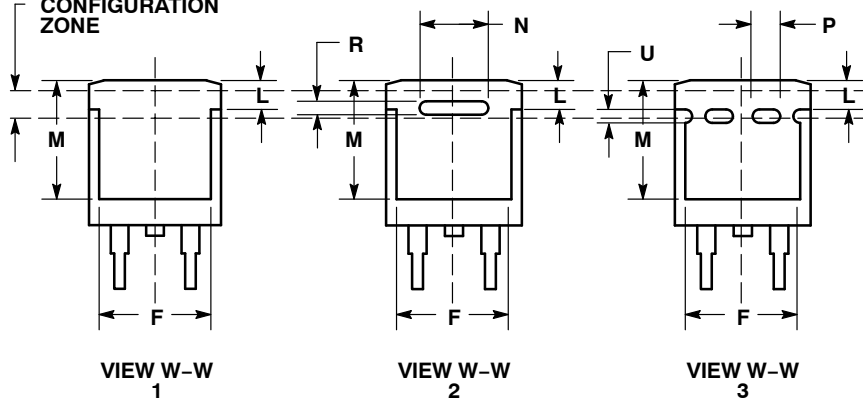
SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- | | | | | | |
|---|--|--|---|--|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE |
|---|--|--|---|--|---|

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

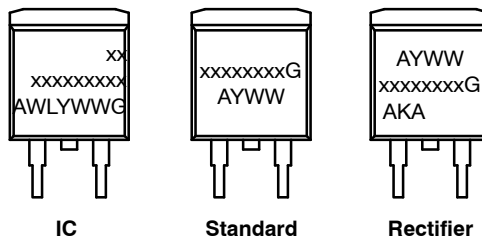
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CASE 418B-04
ISSUE L

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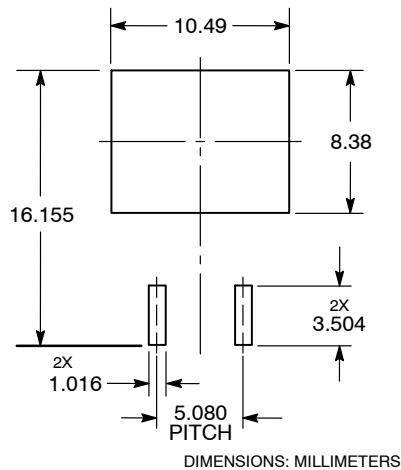
**GENERIC
MARKING DIAGRAM***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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