P2N2222A

Amplifier Transistors

NPN Silicon

ON Semiconductor®

http://onsemi.com

Features

- These are Pb−Free Devices*

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	40	Vdc
Collector – Base Voltage	V_{CBO}	75	Vdc
Emitter – Base Voltage	V_{EBO}	6.0	Vdc
Collector Current – Continuous	I_C	600	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
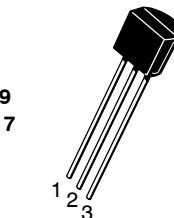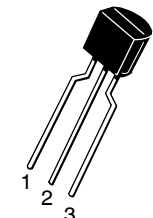
COLLECTOR
1

2
BASE

3
EMITTER

TO−92
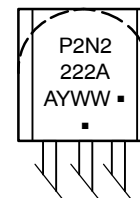**CASE 29**
STYLE 17

1
2
3
STRAIGHT LEAD
BULK PACK

1
2
3
BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAM

P2N2
222A
AYWW ▪

A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping[†]
P2N2222AG	TO−92 (Pb−Free)	5000 Units/Bulk
P2N2222ARL1G	TO−92 (Pb−Free)	2000/Tape & Ammo

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

P2N2222A

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	–	Vdc
Collector – Base Breakdown Voltage (I_C = 10 µAdc, I_E = 0)	$V_{(BR)CBO}$	75	–	Vdc
Emitter – Base Breakdown Voltage (I_E = 10 µAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	–	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{CEX}	–	10	nAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	– –	0.01 10	µAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	10	nAdc
Collector Cutoff Current (V_{CE} = 10 V)	I_{CEO}	–	10	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{BEX}	–	20	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = –55°C) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (Note 1) (I_C = 150 mAdc, V_{CE} = 1.0 Vdc) (Note 1) (I_C = 500 mAdc, V_{CE} = 10 Vdc) (Note 1)	h_{FE}	35 50 75 35 100 50 40	– – – – 300 – –	–
Collector – Emitter Saturation Voltage (Note 1) (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	– –	0.3 1.0	Vdc
Base – Emitter Saturation Voltage (Note 1) (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE(sat)}$	0.6 –	1.2 2.0	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Current – Gain – Bandwidth Product (Note 2) (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)C	f_T	300	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	–	8.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	–	25	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{ie}	2.0 0.25	8.0 1.25	kΩ
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{re}	– –	8.0 4.0	X 10^{-4}
Small–Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	50 75	300 375	–
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{oe}	5.0 25	35 200	µMhos
Collector Base Time Constant (I_E = 20 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)	$rb'C_c$	–	150	ps
Noise Figure (I_C = 100 µAdc, V_{CE} = 10 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)	N_F	–	4.0	dB

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
2. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = −2.0 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (Figure 1)	t_d	–	10	ns
Rise Time		t_r	–	25	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (Figure 2)	t_s	–	225	ns
Fall Time		t_f	–	60	ns

SWITCHING TIME EQUIVALENT TEST CIRCUITS

Scope rise time < 4 ns
*Total shunt capacitance of test jig, connectors, and oscilloscope.
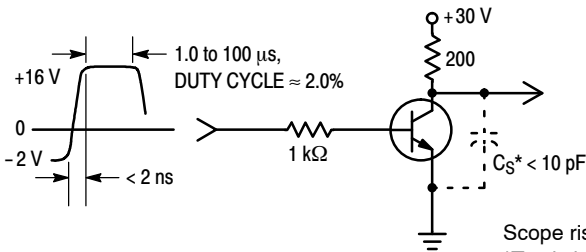
Figure 1. Turn−On Time
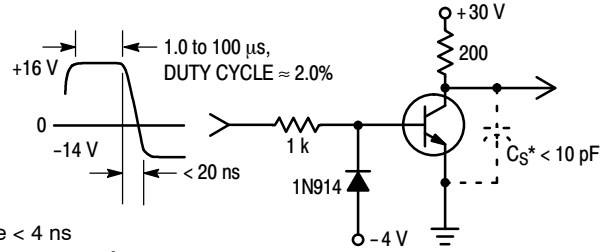
Figure 2. Turn−Off Time

Figure 3. DC Current Gain
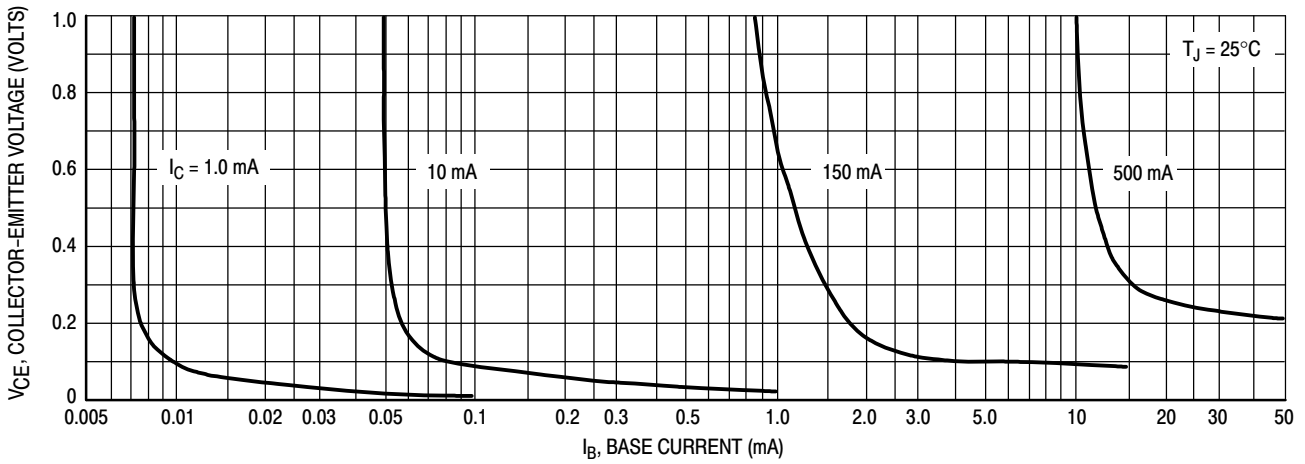
Figure 4. Collector Saturation Region
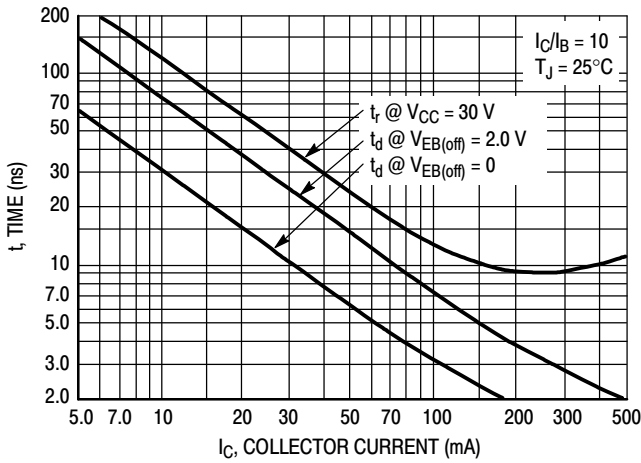
Figure 5. Turn–On Time
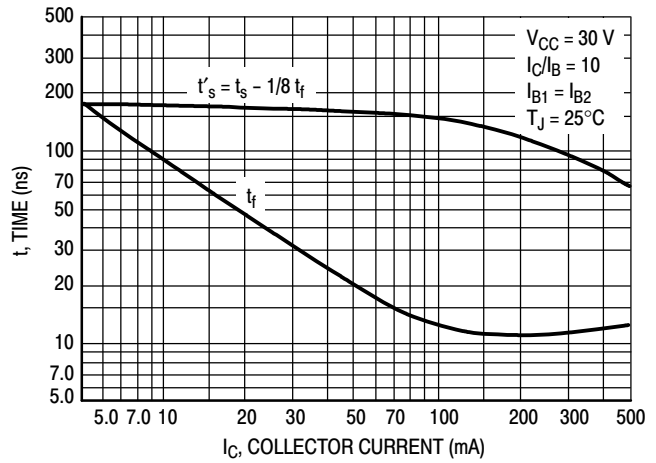
Figure 6. Turn–Off Time
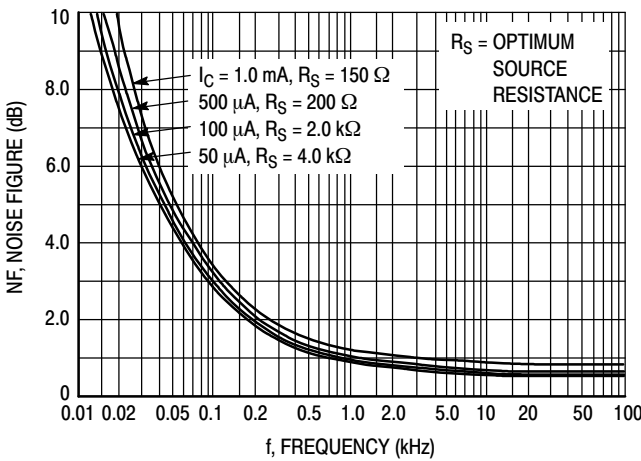
Figure 7. Frequency Effects
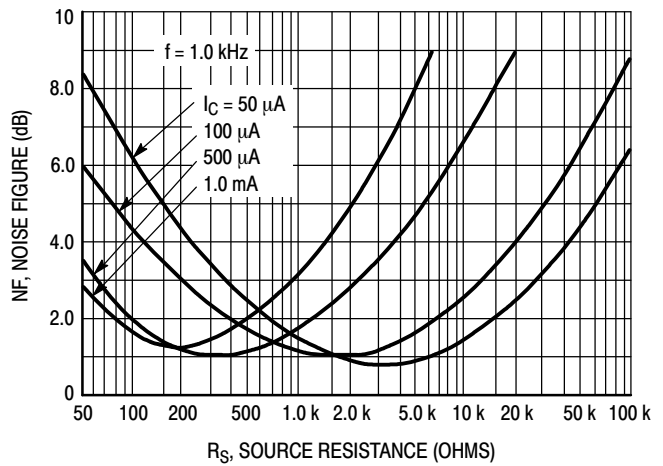
Figure 8. Source Resistance Effects
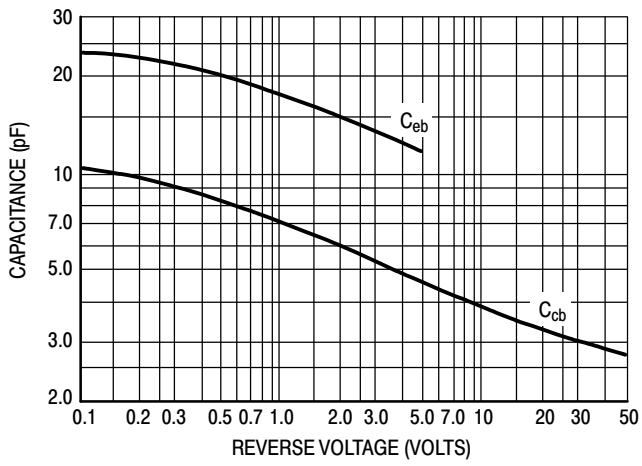
Figure 9. Capacitances
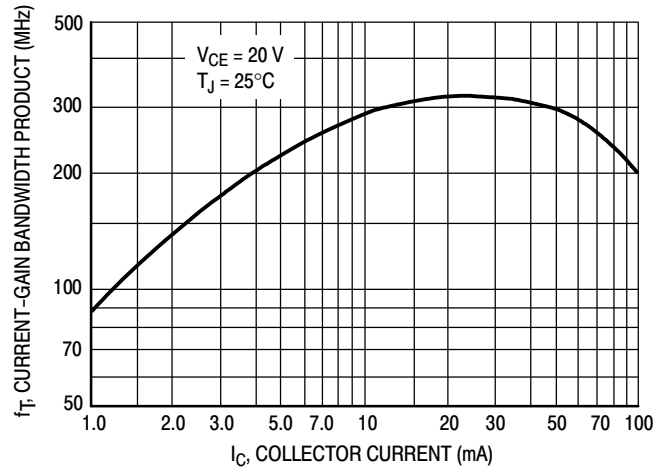
Figure 10. Current−Gain Bandwidth Product
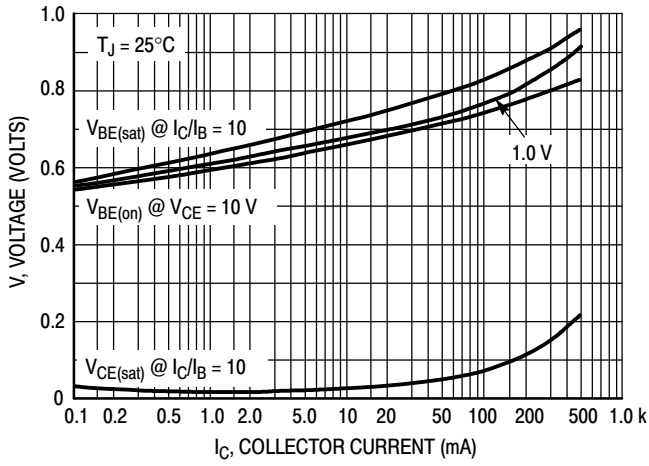
Figure 11. "On" Voltages
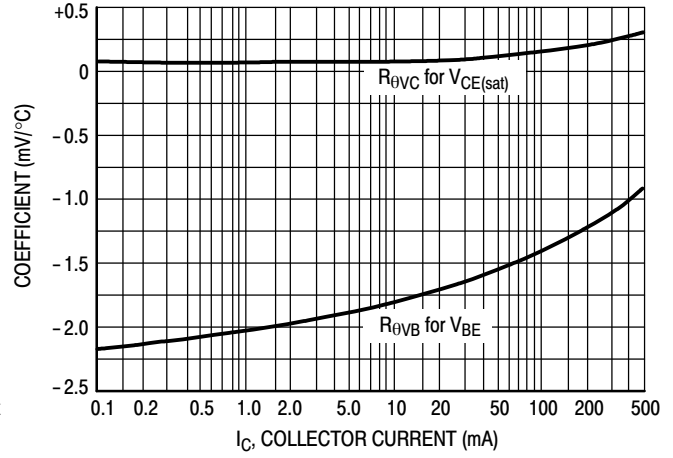
Figure 12. Temperature Coefficients
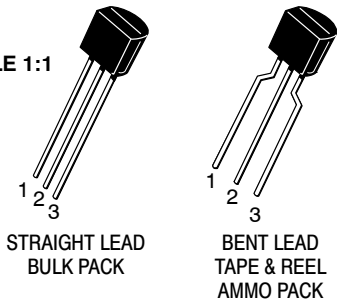
SCALE 1:1

TO−92 (TO−226)
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

STRAIGHT LEAD
BULK PACK

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

SEATING PLANE

SECTION X−X

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

BENT LEAD
TAPE & REEL
AMMO PACK
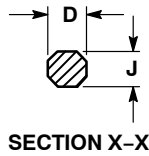
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

SEATING PLANE

SECTION X−X

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

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NEW STANDARD:		
DESCRIPTION:	TO−92 (TO−226)	PAGE 1 OF 3

STYLE 1:
PIN 1. EMITTER
   2. BASE
   3. COLLECTOR

STYLE 2:
PIN 1. BASE
   2. EMITTER
   3. COLLECTOR

STYLE 3:
PIN 1. ANODE
   2. ANODE
   3. CATHODE

STYLE 4:
PIN 1. CATHODE
   2. CATHODE
   3. ANODE

STYLE 5:
PIN 1. DRAIN
   2. SOURCE
   3. GATE

STYLE 6:
PIN 1. GATE
   2. SOURCE & SUBSTRATE
   3. DRAIN

STYLE 7:
PIN 1. SOURCE
   2. DRAIN
   3. GATE

STYLE 8:
PIN 1. DRAIN
   2. GATE
   3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
   2. EMITTER
   3. BASE 2

STYLE 10:
PIN 1. CATHODE
   2. GATE
   3. ANODE

STYLE 11:
PIN 1. ANODE
   2. CATHODE & ANODE
   3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
   2. GATE
   3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
   2. GATE
   3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
   2. COLLECTOR
   3. BASE

STYLE 15:
PIN 1. ANODE 1
   2. CATHODE
   3. ANODE 2

STYLE 16:
PIN 1. ANODE
   2. GATE
   3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
   2. BASE
   3. EMITTER

STYLE 18:
PIN 1. ANODE
   2. CATHODE
   3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
   2. ANODE
   3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
   2. CATHODE
   3. ANODE

STYLE 21:
PIN 1. COLLECTOR
   2. EMITTER
   3. BASE

STYLE 22:
PIN 1. SOURCE
   2. GATE
   3. DRAIN

STYLE 23:
PIN 1. GATE
   2. SOURCE
   3. DRAIN

STYLE 24:
PIN 1. EMITTER
   2. COLLECTOR/ANODE
   3. CATHODE

STYLE 25:
PIN 1. MT 1
   2. GATE
   3. MT 2

STYLE 26:
PIN 1. V_{CC}
   2. GROUND 2
   3. OUTPUT

STYLE 27:
PIN 1. MT
   2. SUBSTRATE
   3. MT

STYLE 28:
PIN 1. CATHODE
   2. ANODE
   3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
   2. ANODE
   3. CATHODE

STYLE 30:
PIN 1. DRAIN
   2. GATE
   3. SOURCE

STYLE 31:
PIN 1. GATE
   2. DRAIN
   3. SOURCE

STYLE 32:
PIN 1. BASE
   2. COLLECTOR
   3. EMITTER

STYLE 33:
PIN 1. RETURN
   2. INPUT
   3. OUTPUT

STYLE 34:
PIN 1. INPUT
   2. GROUND
   3. LOGIC

STYLE 35:
PIN 1. GATE
   2. COLLECTOR
   3. EMITTER

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STATUS:	**ON SEMICONDUCTOR STANDARD**	
NEW STANDARD:		
DESCRIPTION:	**TO−92 (TO−226)**	**PAGE 2 OF 3**

ISSUE	REVISION	DATE
AM	ADDED BENT–LEAD TAPE & REEL VERSION. REQ. BY J. SUPINA.	09 MAR 2007

PUBLICATION ORDERING INFORMATION

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