February 2004

# FDS7079ZN3

## 30 Volt P-Channel PowerTrench® MOSFET

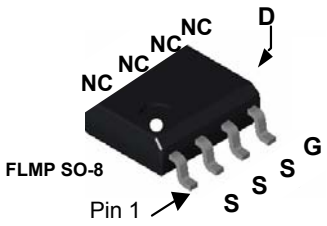
### General Description

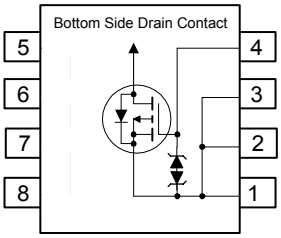
Advanced P Channel MOSFET combined with Advanced SO8 FLMP package providing a device with extremely low thermal impedance and improved electrical performance.

Applications for this device include multi-cell battery protection and charging, including protection and load switching in notebook computer and notebook battery packs.

Features

- –16 A, –30 V. $R_{DS(ON)}$ = 7.5 mΩ @ $V_{GS}$ = –10 V
  $R_{DS(ON)}$ = 11.5 mΩ @ $V_{GS}$ = – 4.5 V
- ESD protection diode (note 3)
- ESD rating: 4kV
- High performance trench technology for extremely low $R_{DS(ON)}$
- FLMP SO-8 package for enhanced thermal performance in industry-standard package size




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | –30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±25 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | –16 | A |
| | – Pulsed | | –60 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 3.13 | W |
| | | (Note 1b) | 1.5 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 40 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 0.5 | |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDS7079ZN3 | FDS7079ZN3 | 13'' | 12mm | 2500 units |

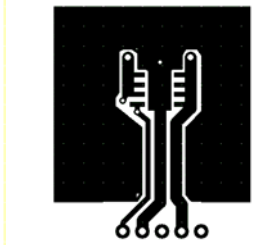
## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 μA | –30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 μA,Referenced to 25°C | | –20 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –24 V, $V_{GS}$ = 0 V | | | –1 | μA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±25 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | –1 | –1.5 | –3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 μA,Referenced to 25°C | | 0.5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –10 V, $I_D$ = –16 A<br>$V_{GS}$ = –4.5 V, $I_D$ = –13 A<br>$V_{GS}$= –10 V, $I_D$ =–16A, $T_J$=125°C | | 6.7<br>9.4<br>9.2 | 7.5<br>11.5 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –10 V, $I_D$ = –16 A | | 47 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 3630 | | pF |
| $C_{oss}$ | Output Capacitance | | | 985 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 490 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 3.0 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –15 V, $I_D$ = –1 A, $V_{GS}$ = –10 V, $R_{GEN}$ = 6 Ω | | 10 | 19 | ns |
| $t_r$ | Turn–On Rise Time | | | 20 | 35 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 64 | 102 | ns |
| $t_f$ | Turn–Off Fall Time | | | 98 | 157 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = –15 V, $I_D$ = –16 A, $V_{GS}$ = –5 V | | 39 | 55 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 10 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 15 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | –2.5 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –2.5 A (Note 2) | | –0.7 | –1.2 | V |
| $t_{RR}$ | Reverse Recovery Time | $I_F$ = –16 A, $d_{iF}/d_t$ = 100 A/μs (Note 2) | | 38 | | ns |
| $Q_{RR}$ | Reverse Recovery Charge | | | 24 | | nC |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1in$^2$ pad of 2 oz copper

b) 85°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

**3.** The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## Typical Characteristics

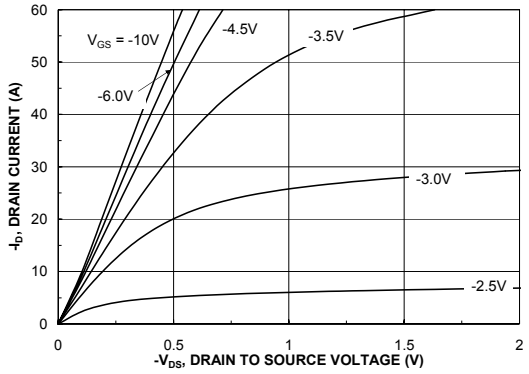



**Figure 1. On-Region Characteristics.**

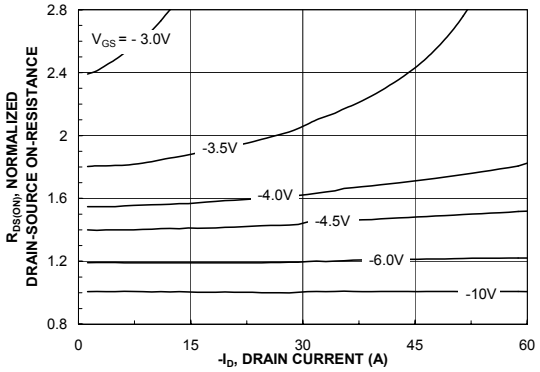
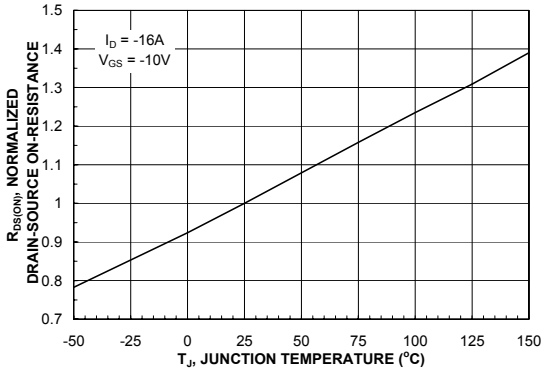



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**




**igure 3. On-Resistance Variation with Temperature.**

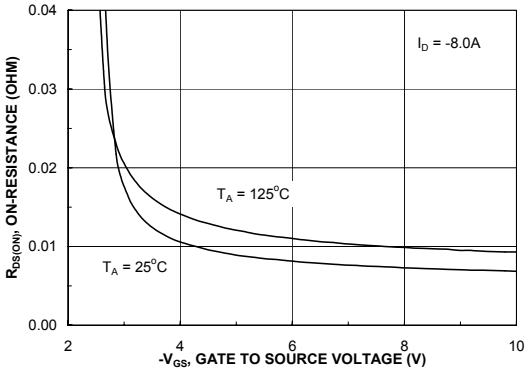



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

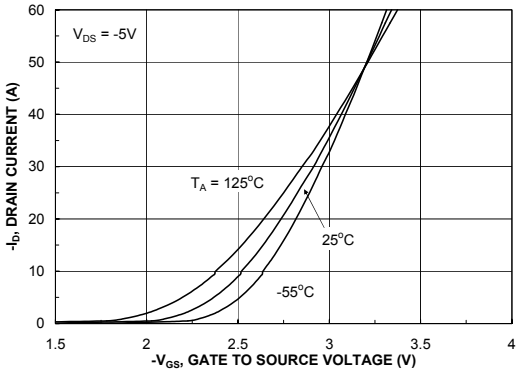



**Figure 5. Transfer Characteristics.**

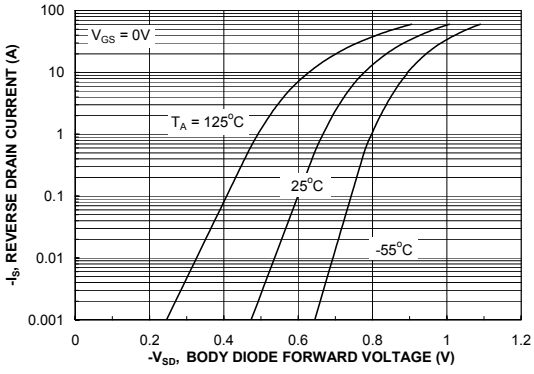



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

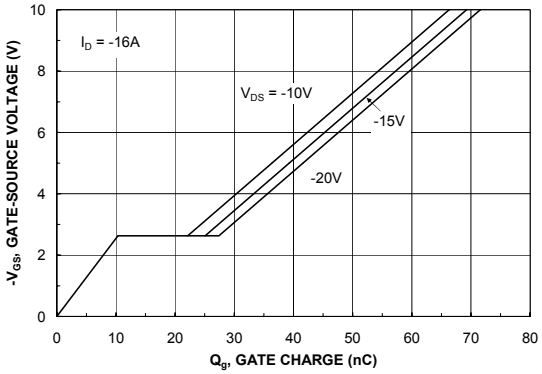



**Figure 7. Gate Charge Characteristics.**

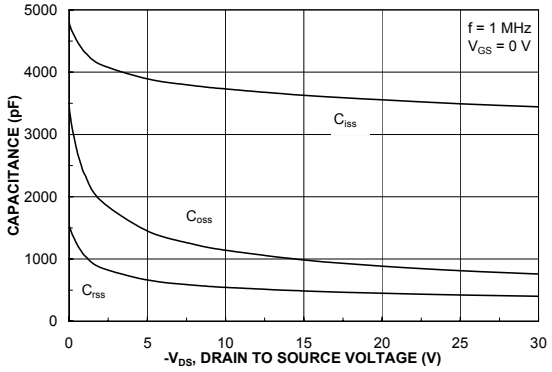



**Figure 8. Capacitance Characteristics.**

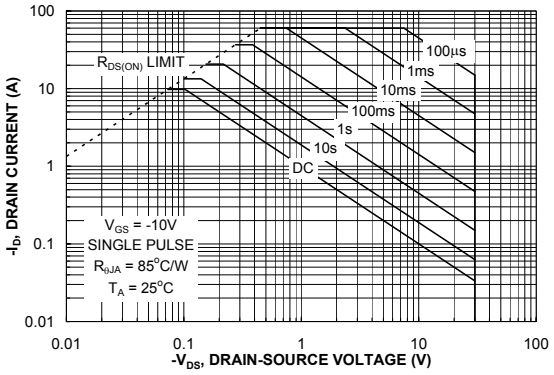



**Figure 9. Maximum Safe Operating Area.**

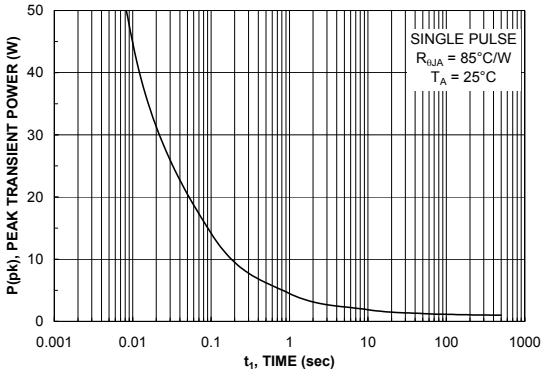



**Figure 10. Single Pulse Maximum Power Dissipation.**

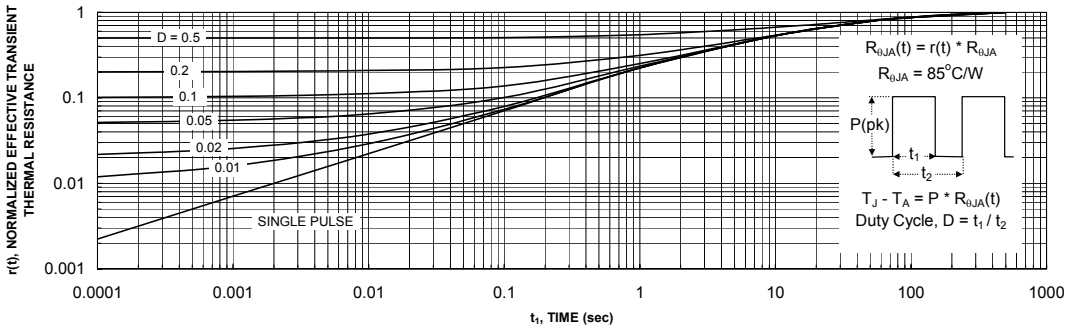
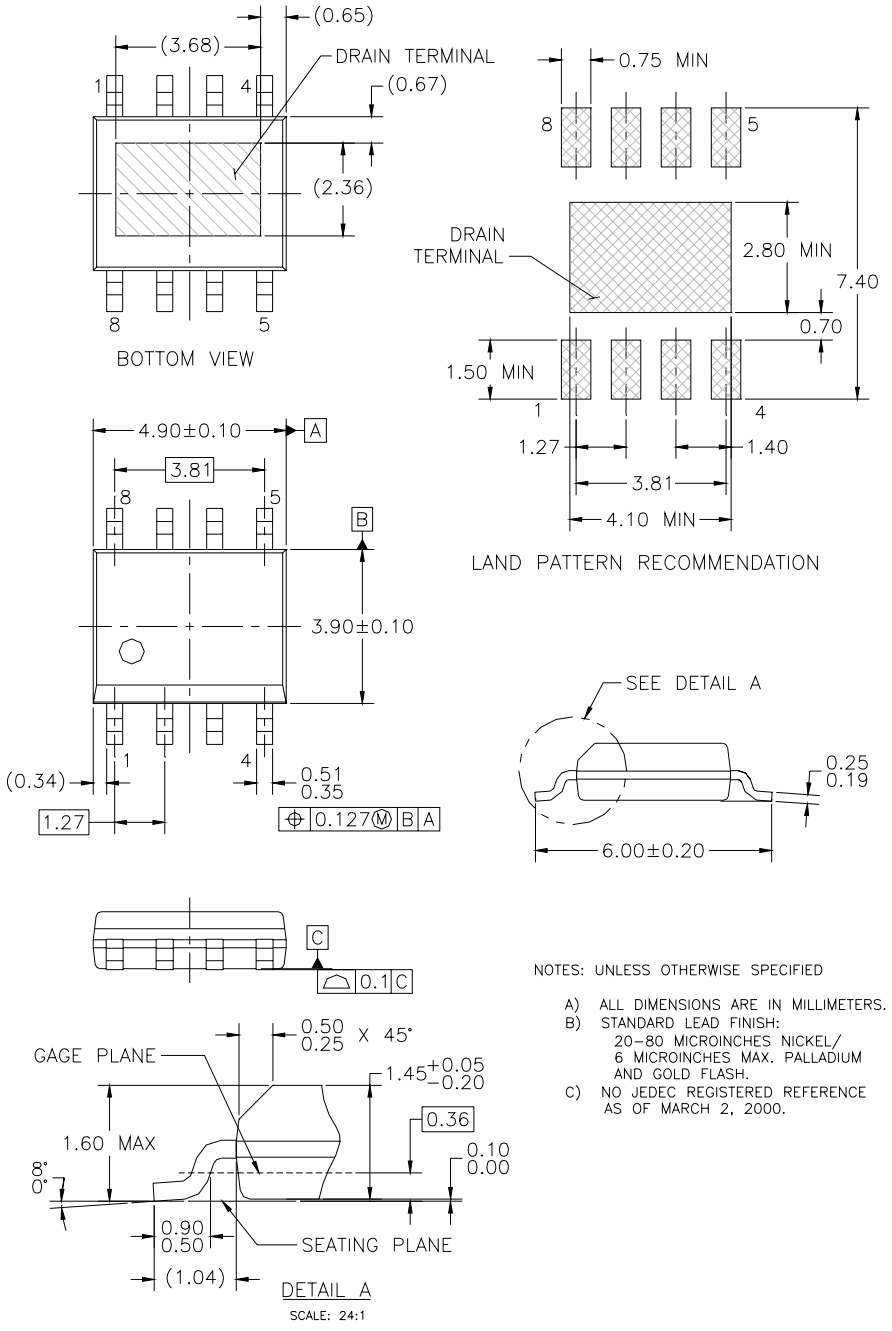



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

## Dimensional Outline and Pad Layout




NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) STANDARD LEAD FINISH:
20–80 MICROINCHES NICKEL/
6 MICROINCHES MAX. PALLADIUM
AND GOLD FLASH.
C) NO JEDEC REGISTERED REFERENCE
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