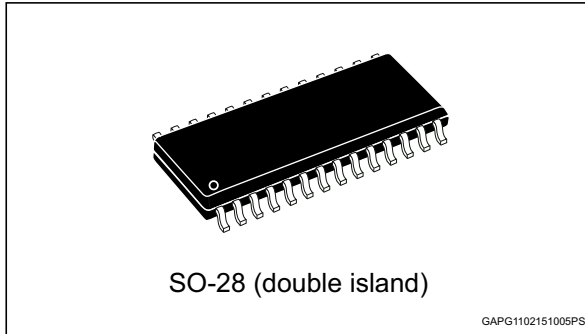


## Double channel high-side driver

Datasheet - production data



- Proportional load current sense
- Current sense disable
- Thermal shutdown protection and diagnosis
- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation

### Description

The VND920P-E is a double chip device designed in STMicroelectronics™ VIPower™ M0-3 technology. The VND920P-E is intended for driving any type of load with one side connected to ground. The active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and automatic restart protects the device against overload.

The device integrates an analog current sense output which delivers a current proportional to the load current. The device automatically turns off in the case where the ground pin becomes disconnected.

### Features

Type	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VND920P-E	16 m $\Omega$	35 A <sup>(1)</sup>	36 V

1. Per channel with all the output pins connected to the PCB.

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Very low standby current
- CMOS compatible input

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28	VND920P-E	VND920PTR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

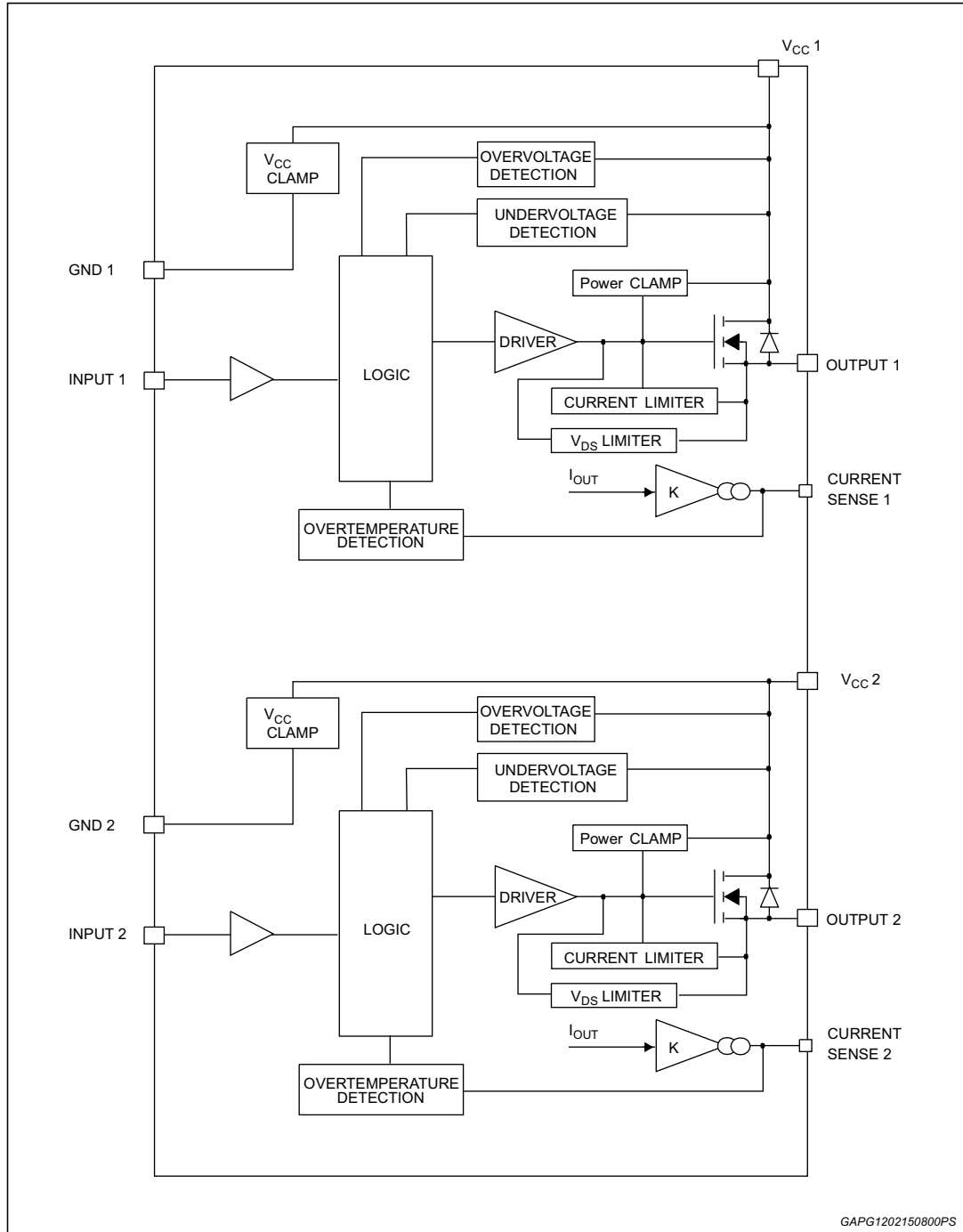


Figure 2. Configuration diagram (top view)

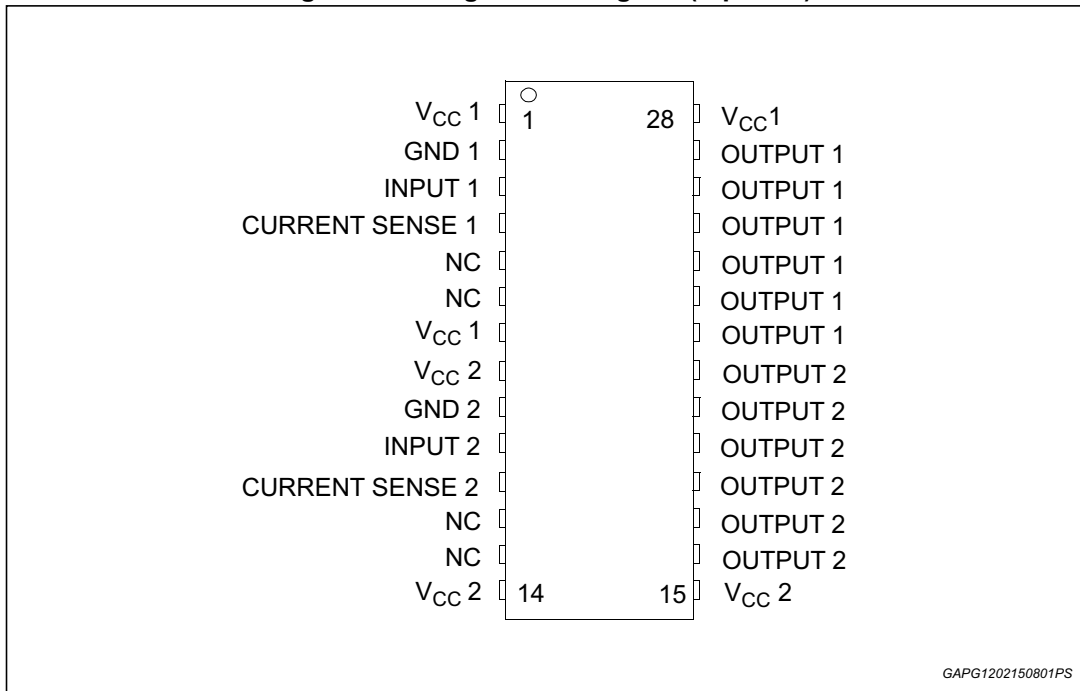
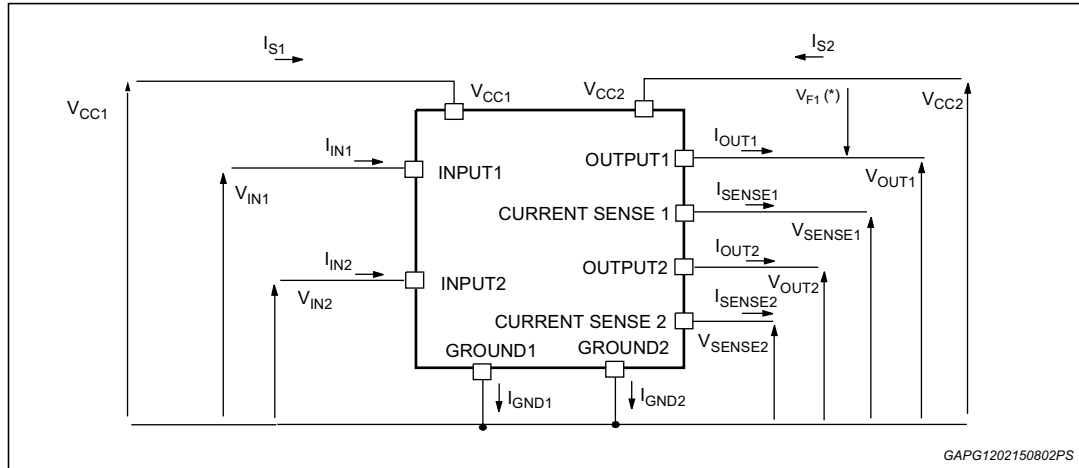


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current Sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1KΩ resistor	X		Through 10 KΩ resistor

## 2 Electrical specifications

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{CCn} - V_{OUTn}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{gnd}$	DC reverse ground pin current	-200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-21	A
$I_{IN}$	DC input current	$\pm 10$	mA
$V_{CSSENSE}$	Current Sense maximum voltage	-3 +15	V V
$V_{ESD}$	Electrostatic discharge (human body model: $R = 1.5\text{ K}\Omega$ ; $C = 100\text{ pF}$ )		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
	- $V_{CC}$	5000	V

**Table 3. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
$E_{MAX}$	Maximum switching energy ( $L = 0.25 \text{ mH}$ ; $R_L = 0 \text{ }\Omega$ ; $V_{bat} = 13.5 \text{ V}$ ; $T_{jstart} = 150 \text{ }^\circ\text{C}$ ; $I_L = 45 \text{ A}$ )	355	mJ
$P_{tot}$	Power dissipation $T_C \leq 25^\circ\text{C}$	6.25	W
$T_j$	Junction operating temperature	Internally limited	$^\circ\text{C}$
$T_C$	Case operating temperature	-40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

## 2.2 Thermal data

**Table 4. Thermal data (per island)**

Symbol	Parameter	Value		Unit
$R_{thj-lead}$	Thermal resistance junction-lead	15		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (one chip ON)	55 <sup>(1)</sup>	45 <sup>(2)</sup>	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (two chips ON)	46 <sup>(1)</sup>	32 <sup>(2)</sup>	$^\circ\text{C}/\text{W}$

1. When mounted on a standard single-sided FR-4 board with 1cm<sup>2</sup> of Cu (at least 35  $\mu\text{m}$  thick) connected to all  $V_{CC}$  pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6cm<sup>2</sup> of Cu (at least 35  $\mu\text{m}$  thick) connected to all  $V_{CC}$  pins. Horizontal mounting and no artificial air flow.



## 2.3 Electrical characteristics

Values specified in this section are for  $8\text{ V} < V_{CC} < 36\text{ V}$ ;  $-40\text{ °C} < T_j < 150\text{ °C}$ , unless otherwise stated.

**Table 5. Power**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		5.5	13	36	V
$V_{USD}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}$	Overvoltage shutdown		36			V
$R_{ON}$	On-state resistance	$I_{OUT} = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ;			16	mΩ
		$I_{OUT} = 10\text{ A}$ ;			32	mΩ
		$I_{OUT} = 3\text{ A}$ ; $V_{CC} = 6\text{ V}$			55	mΩ
$V_{CLAMP}$	Clamp voltage	$I_{CC} = 20\text{ mA}$	41	48	55	V
$I_S$	Supply current	Off-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = V_{OUT} = 0\text{ V}$		10	25	μA
		Off-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = V_{OUT} = 0\text{ V}$ ; $T_j = 25\text{ °C}$		10	20	μA
		On-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = 5\text{ V}$ ; $I_{OUT} = 0\text{ A}$ ; $R_{SENSE} = 3.9\text{ k}\Omega$			5	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$	0		50	μA
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0\text{ V}$ ; $V_{OUT} = 3.5\text{ V}$	-75		0	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 125\text{ °C}$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 25\text{ °C}$			3	μA

Note:  $V_{CLAMP}$  and  $V_{OV}$  are correlated. Typical difference is 5 V.

**Table 6. Switching ( $V_{CC}=13\text{ V}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 1.3\ \Omega$ (see <a href="#">Figure 4.</a> )		50		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 1.3\ \Omega$ (see <a href="#">Figure 4.</a> )		50		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 1.3\ \Omega$ (see <a href="#">Figure 4.</a> )	See <a href="#">Figure 22.</a>			V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 1.3\ \Omega$ (see <a href="#">Figure 4.</a> )	See <a href="#">Figure 24.</a>			V/μs

**Table 7.  $V_{CC}$  output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$-I_{OUT} = 5\text{ A}$ ; $T_j = 150\text{ °C}$	–	–	0.6	V

Table 8. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				1.25	V
$I_{IL}$	Low level input current	$V_{IN} = 1.25$ V	1			$\mu$ A
$V_{IH}$	Input high level voltage		3.25			V
$I_{IH}$	High level input current	$V_{IN} = 3.25$ V			10	$\mu$ A
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1$ mA $I_{IN} = -1$ mA	6	6.8 -0.7	8	V V

Table 9. Current sense (9 V  $\leq$   $V_{CC}$   $\leq$  16 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 1$ A; $V_{SENSE} = 0.5$ V; $T_j = -40$ °C...150 °C	3300	4400	6000	
$dK_1/K_1$	Current sense ratio drift	$I_{OUT} = 1$ A; $V_{SENSE} = 0.5$ V; $T_j = -40$ °C...150 °C	-10		+10	%
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 10$ A; $V_{SENSE} = 4$ V; $T_j = -40$ °C $T_j = 25$ °C...150 °C	4200 4400	4900 4900	6000 5750	
$dK_2/K_2$	Current sense ratio drift	$I_{OUT} = 10$ A; $V_{SENSE} = 4$ V; $T_j = -40$ °C...150 °C	-8		+8	%
$K_3$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 30$ A; $V_{SENSE} = 4$ V; $T_j = -40$ °C $T_j = 25$ °C...150 °C	4200 4400	4900 4900	5500 5250	
$dK_3/K_3$	Current sense ratio drift	$I_{OUT} = 30$ A; $V_{SENSE} = 4$ V; $T_j = -40$ °C...150 °C	-6		+6	%
$I_{SENSE0}$	Analog sense current	$V_{CC} = 6...16$ V; $I_{OUT} = 0$ A; $V_{SENSE} = 0$ V; $T_j = -40$ °C...150 °C	0		10	$\mu$ A
$V_{SENSE}$	Max analog sense output voltage	$V_{CC} = 5.5$ V; $I_{OUT} = 5$ A; $R_{SENSE} = 10$ k $\Omega$ $V_{CC} > 8$ V, $I_{OUT} = 10$ A; $R_{SENSE} = 10$ k $\Omega$	2 4			V V
$V_{SENSEH}$	Sense voltage in overtemperature condition	$V_{CC} = 13$ V; $R_{SENSE} = 3.9$ k $\Omega$		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in overtemperature condition	$V_{CC} = 13$ V; $T_j > T_{TSD}$ ; output open		400		$\Omega$
$t_{DSENSE}$	Current sense delay response	To 90 % $I_{SENSE}^{(1)}$			500	$\mu$ s

1. Current sense signal delay after positive input slope.

Table 10. Protections

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ.	Max.	Unit
$T_{TSD}$	Shutdown temperature		150	175	200	°C
$T_R$	Reset temperature		135			°C
$T_{hyst}$	Thermal hysteresis		7	15		°C
$I_{lim}$	Current limitation	$V_{CC} = 13\text{ V}$ $5\text{ V} < V_{CC} < 36\text{ V}$	30	45	75 75	A A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 2\text{ A}$ ; $V_{IN} = 0\text{ V}$ ; $L = 6\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 1\text{ A}$ ; $T_j = -40\text{ °C} \dots 150\text{ °C}$		50		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_j < T_{TSD})\ 0$
	H	L	$(T_j > T_{TSD})\ V_{SENSEH}$
Short circuit to $V_{CC}$	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				Delays and impedance
	I	II	III	IV	
1	- 25 V <sup>(1)</sup>	- 50 V <sup>(1)</sup>	- 75 V <sup>(1)</sup>	- 100 V <sup>(1)</sup>	2 ms, 10 Ω
2	+ 25 V <sup>(1)</sup>	+ 50 V <sup>(1)</sup>	+ 75 V <sup>(1)</sup>	+ 100 V <sup>(1)</sup>	0.2 ms, 10 Ω
3a	- 25 V <sup>(1)</sup>	- 50 V <sup>(1)</sup>	- 100 V <sup>(1)</sup>	- 150 V <sup>(1)</sup>	0.1 μs, 50 Ω
3b	+ 25 V <sup>(1)</sup>	+ 50 V <sup>(1)</sup>	+ 75 V <sup>(1)</sup>	+ 100 V <sup>(1)</sup>	0.1 μs, 50 Ω
4	- 4 V <sup>(1)</sup>	- 5 V <sup>(1)</sup>	- 6 V <sup>(1)</sup>	- 7 V <sup>(1)</sup>	100 ms, 0.01 Ω
5	+ 26.5 V <sup>(1)</sup>	+ 46.5 V <sup>(2)</sup>	+ 66.5 V <sup>(2)</sup>	+ 86.5 V <sup>(2)</sup>	400 ms, 2 Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 4. Switching characteristics

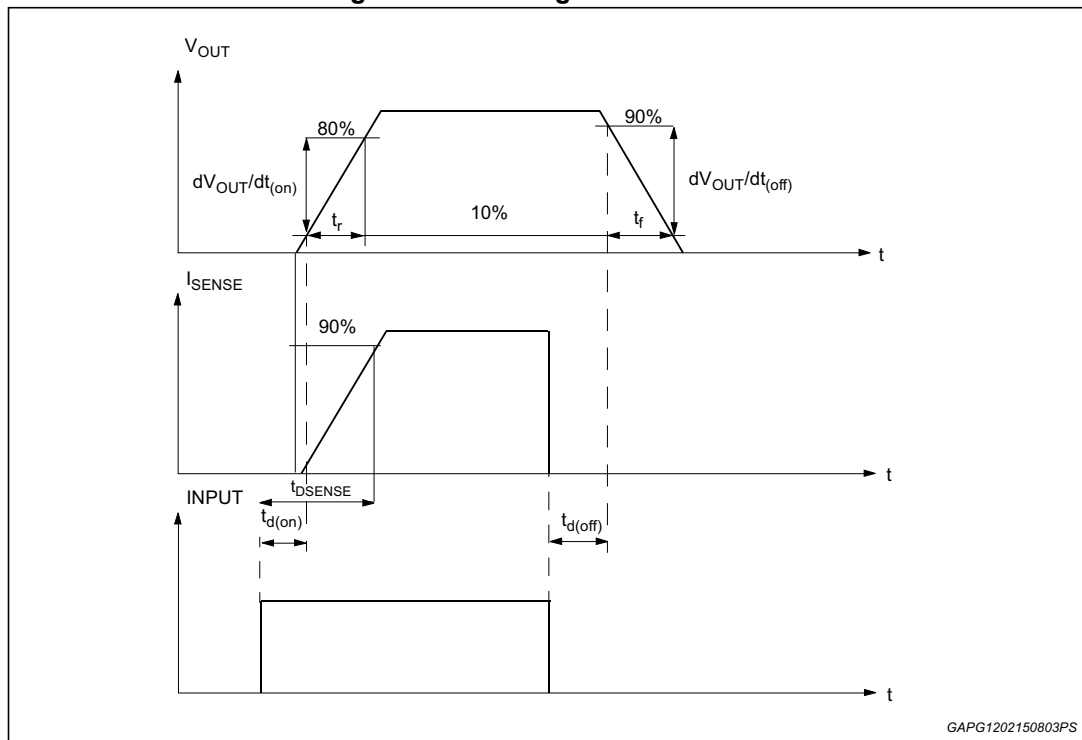


Figure 5.  $I_{OUT}/I_{SENSE}$  versus  $I_{OUT}$

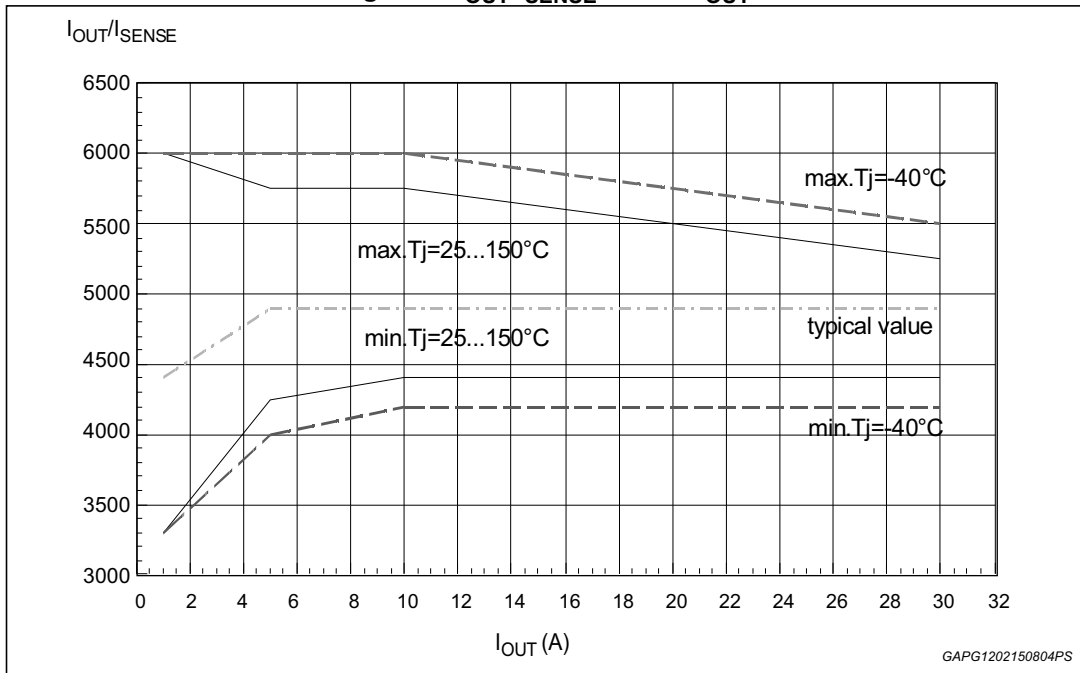
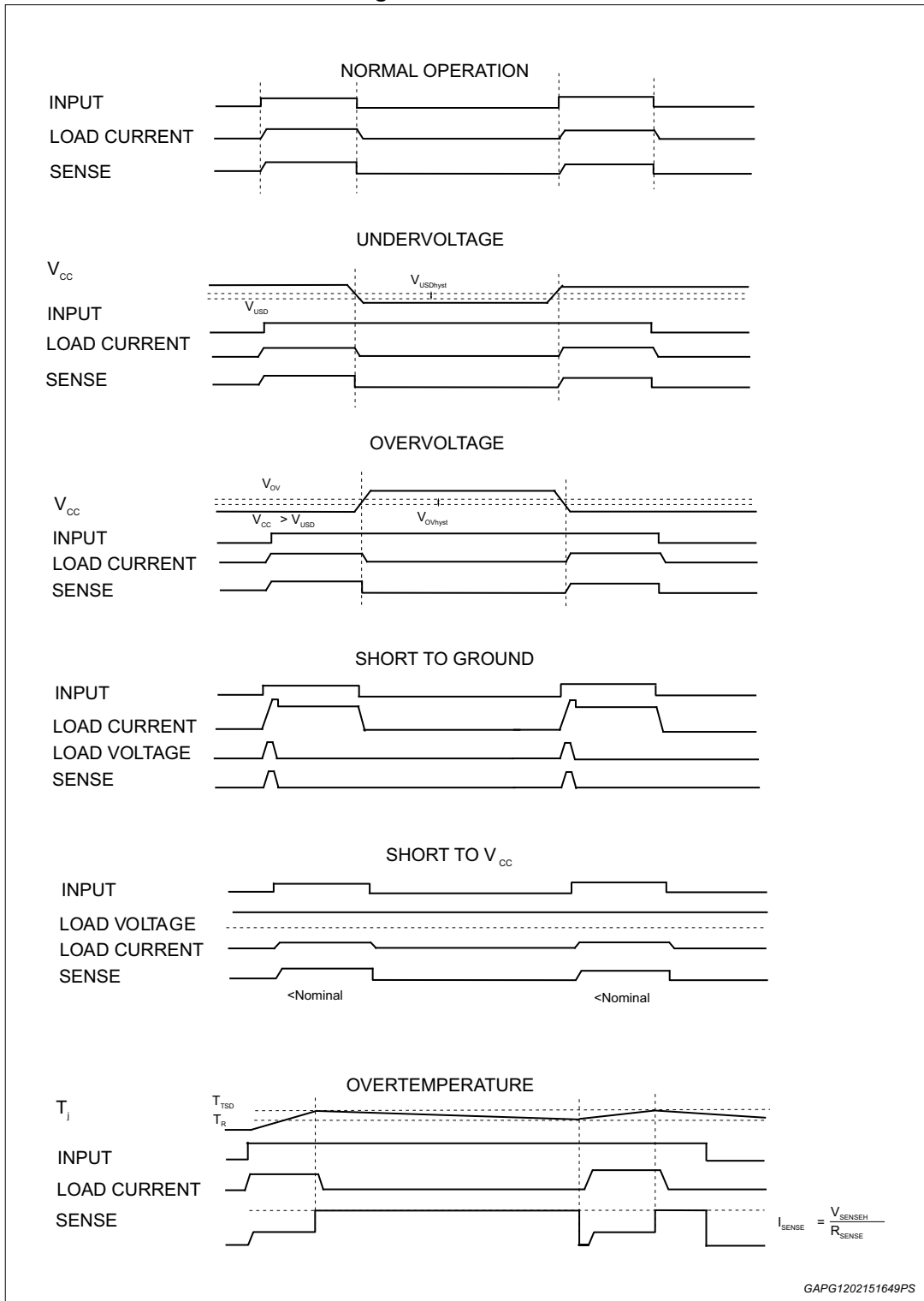
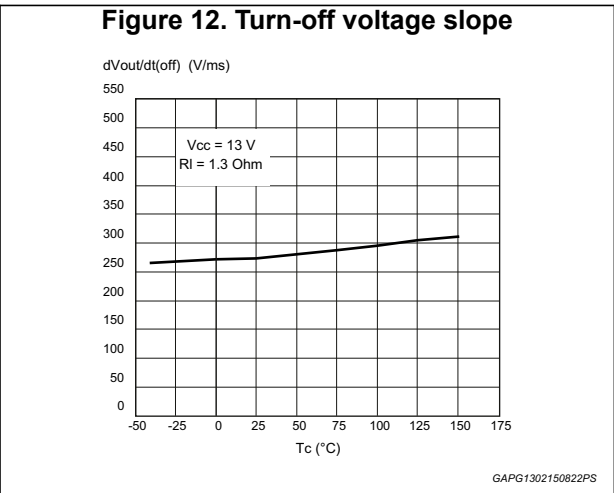
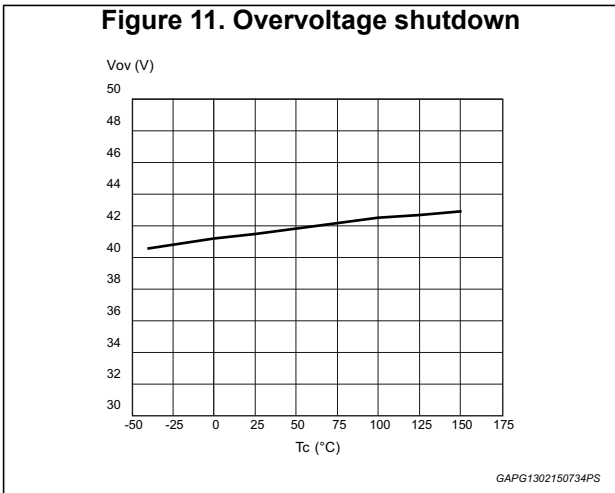
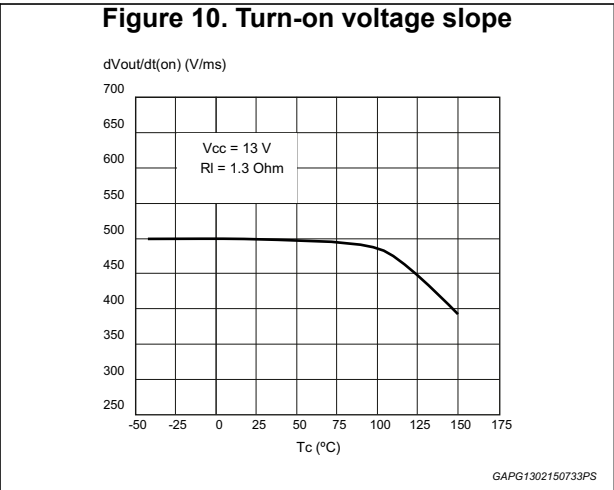
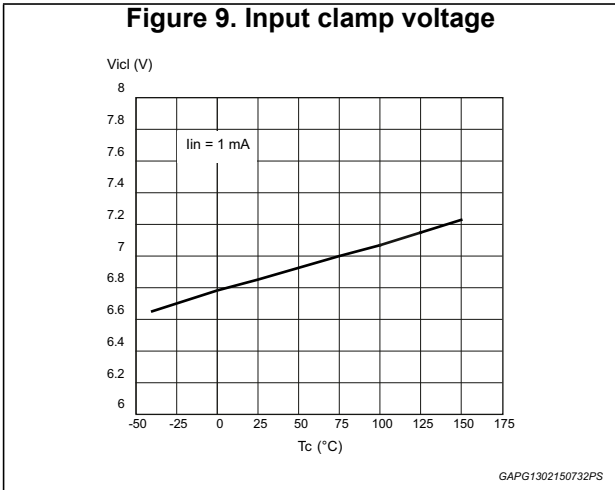
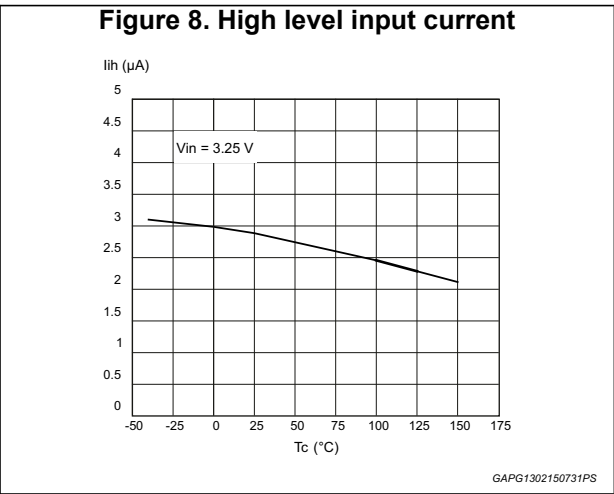
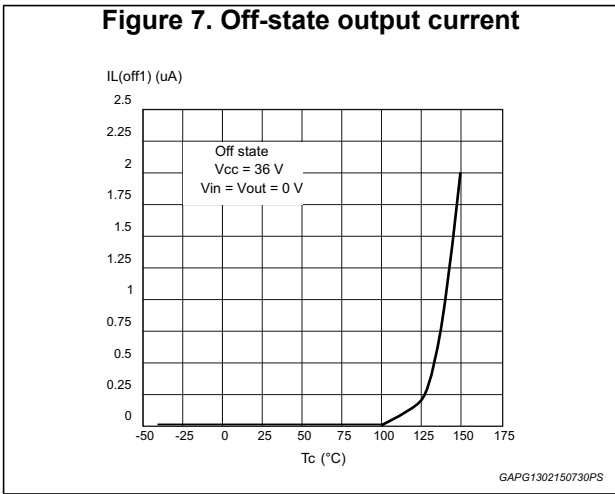
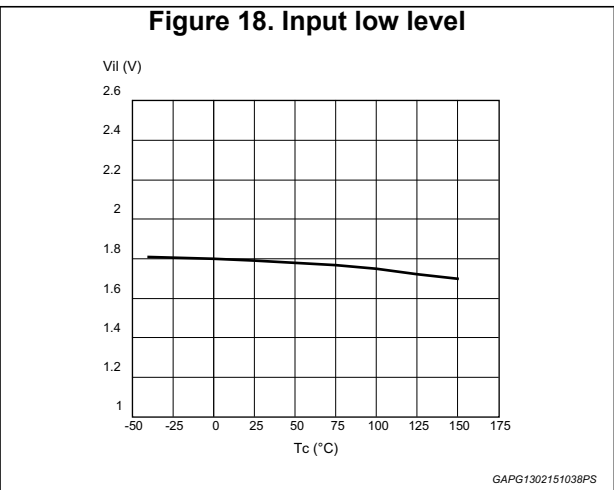
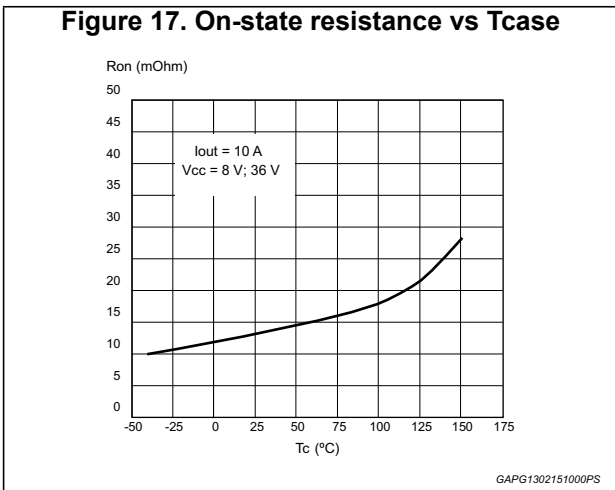
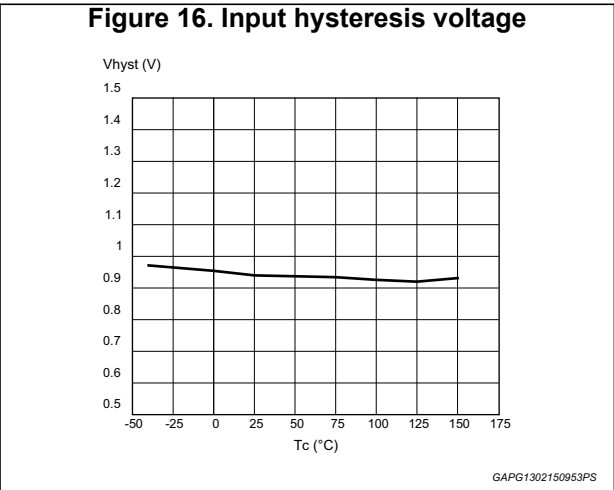
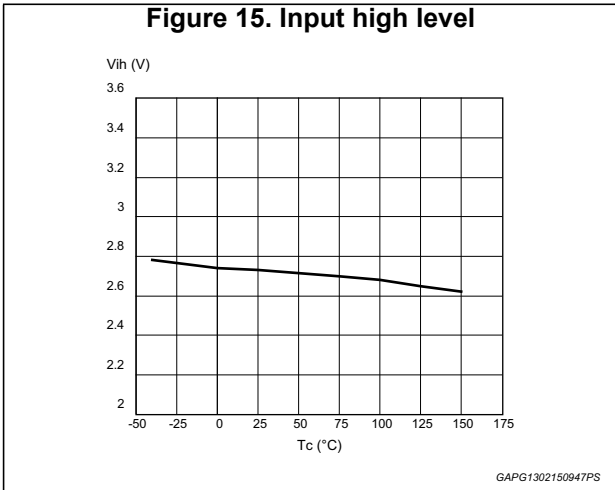
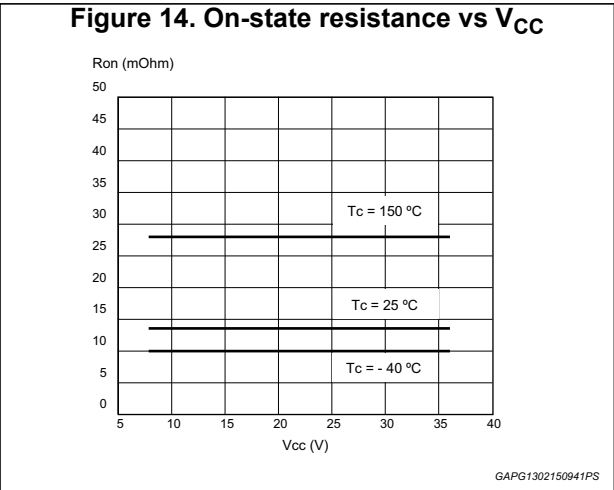
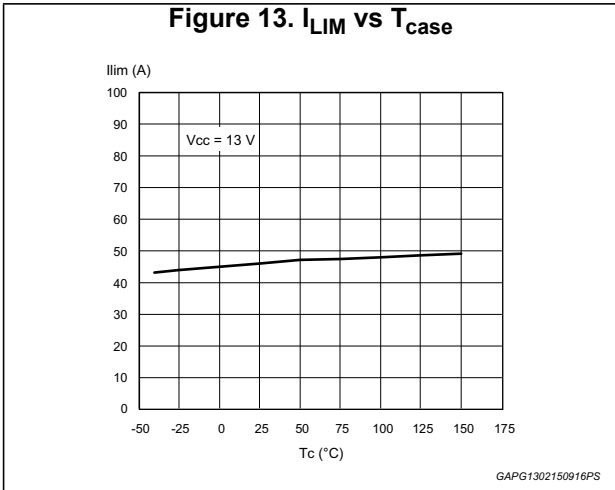


Figure 6. Waveforms



### 3 Electrical characteristics curves

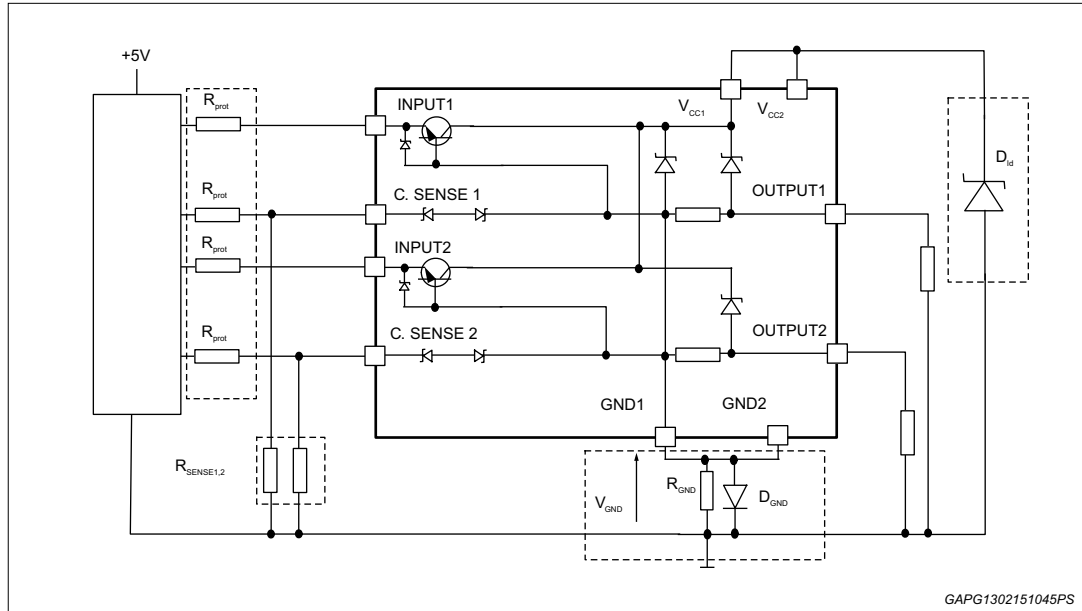






## 4 Application information

Figure 19. Application schematic



### 4.1 GND protection network against reverse battery

#### 4.1.1 Solution 1: resistor in the ground line ( $R_{\text{GND}}$ only)

This can be used with any type of load.

The following is an indication on how to dimension the  $R_{\text{GND}}$  resistor.

1.  $R_{\text{GND}} \leq 600\text{mV} / (I_{\text{S(on)max}})$ .
2.  $R_{\text{GND}} \geq (-V_{\text{CC}}) / (-I_{\text{GND}})$ .

where  $-I_{\text{GND}}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in  $R_{\text{GND}}$  (when  $V_{\text{CC}} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{\text{CC}})^2 / R_{\text{GND}}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{\text{S(on)max}}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the  $R_{\text{GND}}$  produces a shift ( $I_{\text{S(on)max}} * R_{\text{GND}}$ ) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same  $R_{\text{GND}}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to consider [Section 4.1.2](#).

### 4.1.2 Solution 2: diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 1 \text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ( $\sim 600\text{mV}$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## 4.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in [Table 12](#).

## 4.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins are pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the microcontroller I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu\text{C}$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

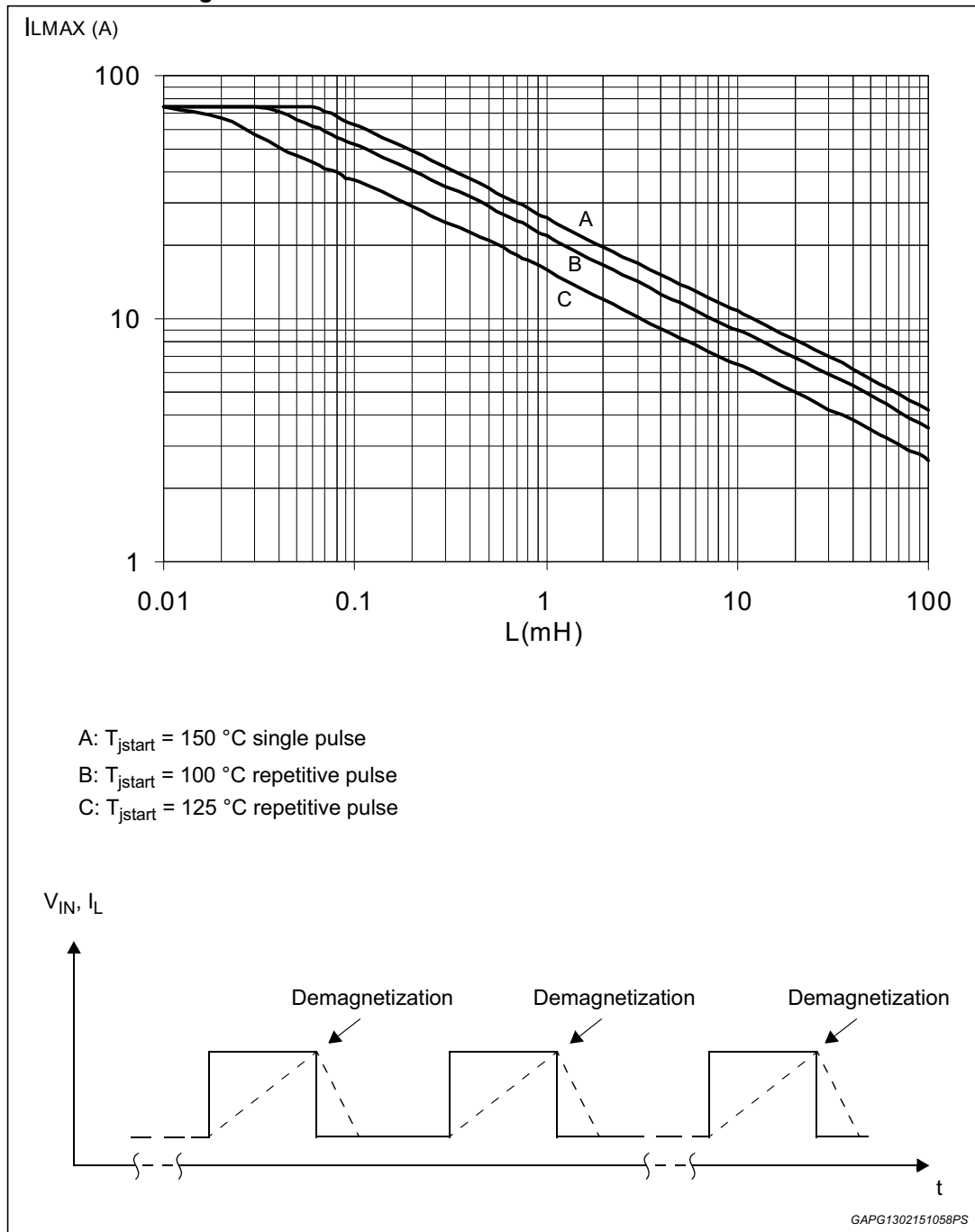
For  $V_{CCpeak} = -100 \text{ V}$  and  $I_{latchup} \geq 20 \text{ mA}$ ;  $V_{OH\mu C} \geq 4.5 \text{ V}$

$5 \text{ k}\Omega \leq R_{prot} \leq 65 \text{ k}\Omega$ .

Recommended values:  $R_{prot} = 10 \text{ k}\Omega$ .

### 4.4 Maximum demagnetization energy ( $V_{CC} = 13.5\text{ V}$ )

Figure 20. Maximum turn-off current versus inductance

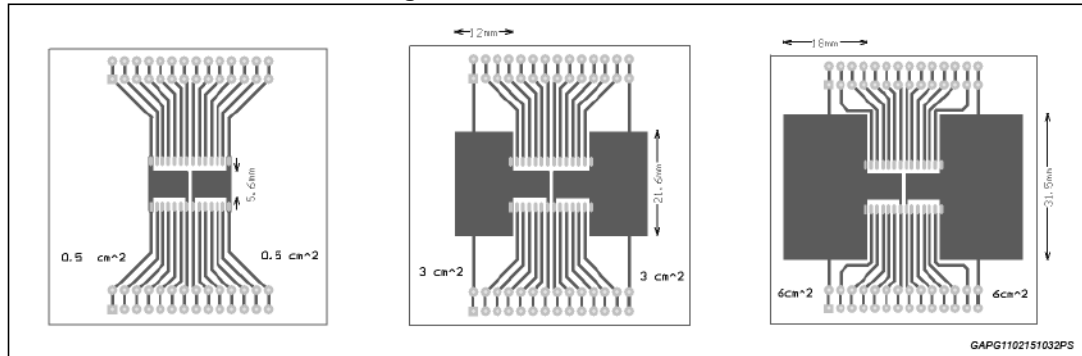


$L \Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 5 Package and PCB thermal data

### 5.1 SO-28 thermal data

Figure 21. SO-28 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35  $\mu$ m, Copper areas: 0.5 cm<sup>2</sup>, 3 cm<sup>2</sup>, 6 cm<sup>2</sup>).

Table 13. Thermal calculation according to the PCB heatsink area

Chip 1	Chip 2	$T_{jchip1}$	$T_{jchip2}$	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1} = P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

$R_{thA}$  = Thermal resistance Junction to Ambient with one chip ON

$R_{thB}$  = Thermal resistance Junction to Ambient with both chips ON and  $P_{dchip1} = P_{dchip2}$

$R_{thC}$  = Mutual thermal resistance

Figure 22.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

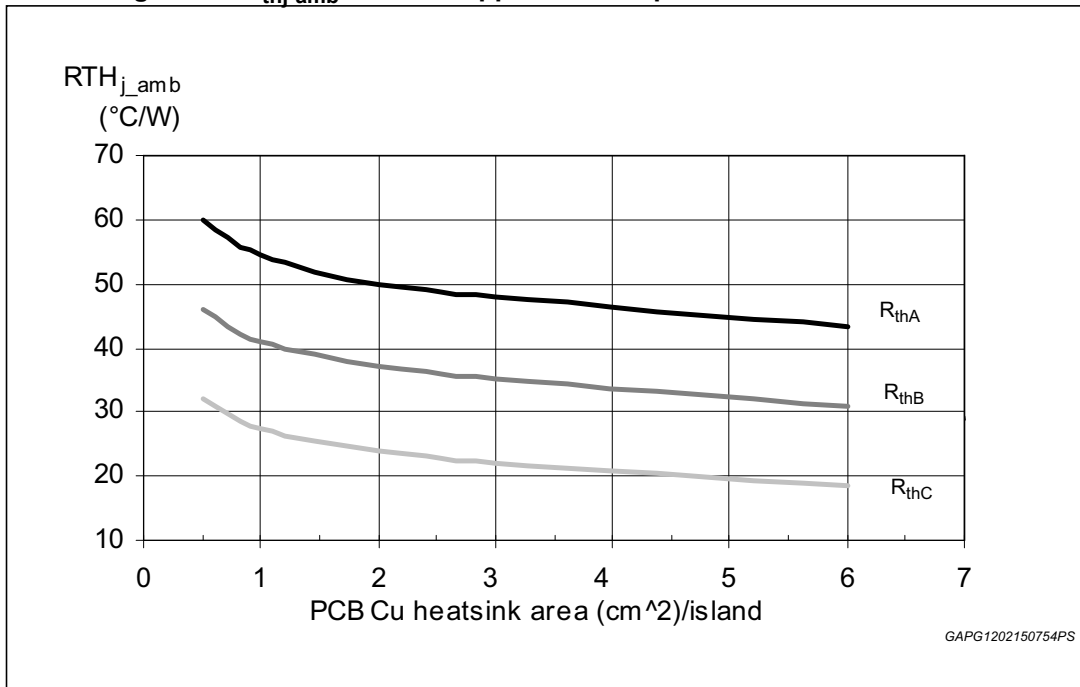
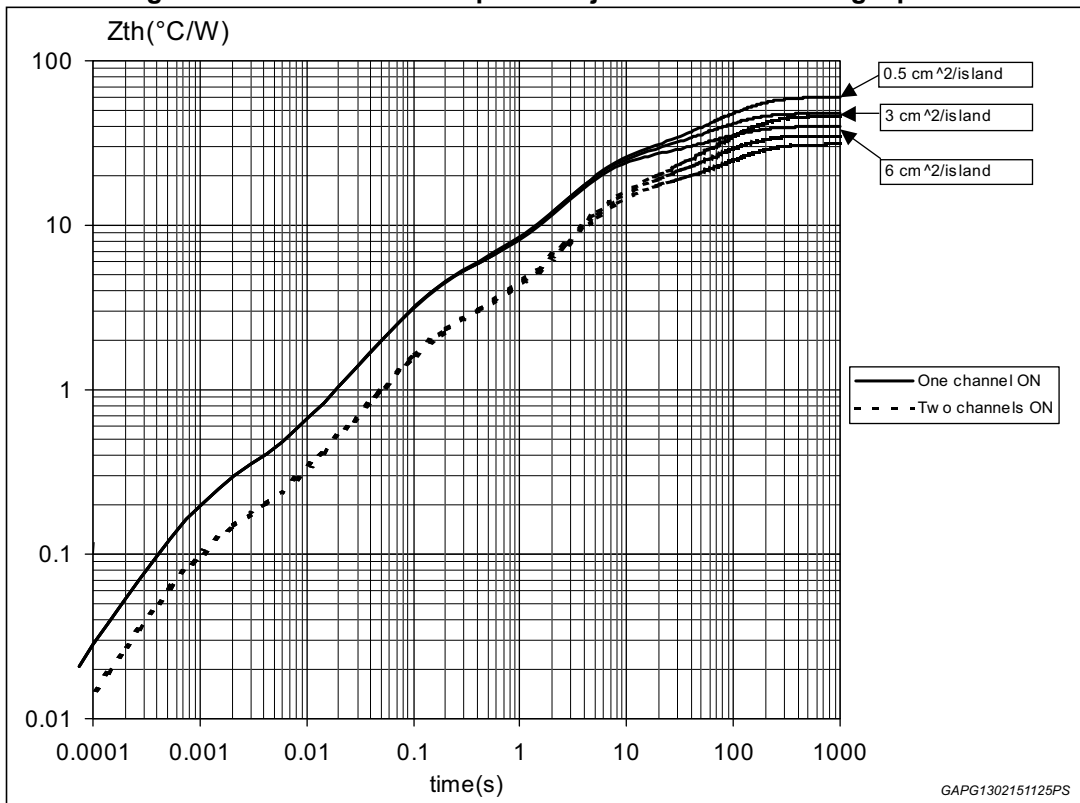


Figure 23. SO-28 thermal impedance junction ambient single pulse

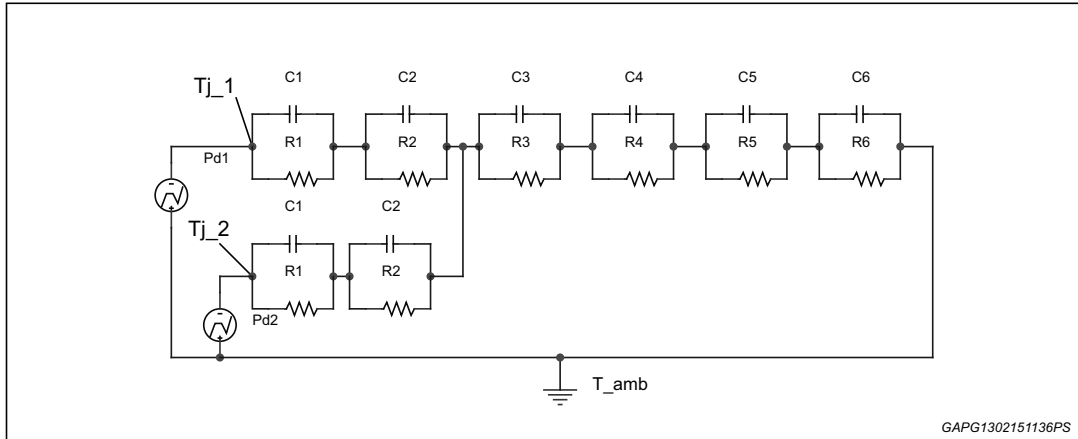


**Equation 1:** pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

**Figure 24. Thermal fitting model of a double channel HSD in SO-28**



GAPG1302151136PS

**Table 14. Thermal parameters**

Area/island (cm <sup>2</sup> )	0.5	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	2.2	
R4 (°C/W)	11	
R5 (°C/W)	15	
R6 (°C/W)	30	13
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7.00E-03	
C3 (W.s/°C)	1.50E-02	
C4 (W.s/°C)	0.2	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	5	8

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 6.1 SO-28 package information

Figure 25. SO-28 package outline

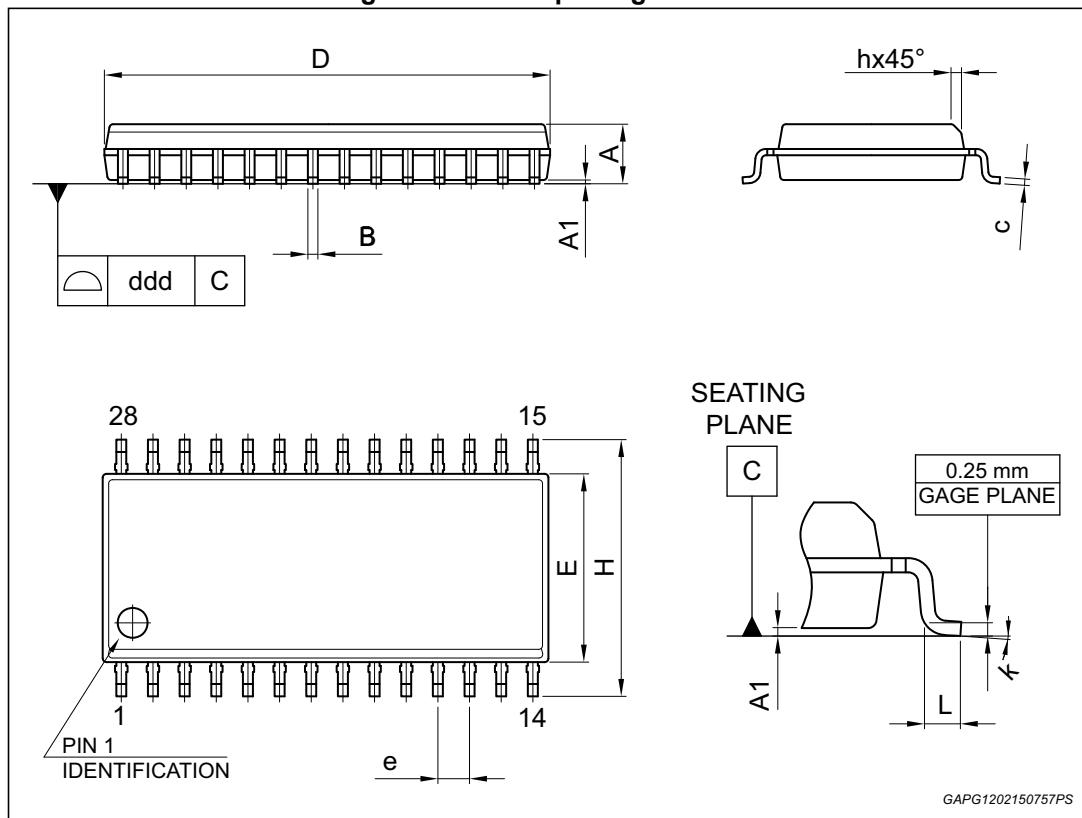


Table 15. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D <sup>(1)</sup>	17.70		18.10

Table 15. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. Dimension "D" does not include mold flash, protrusions or gate burrs.  
Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

## 6.2 SO-28 packing information

Figure 26. SO-28 tube shipment (no suffix)

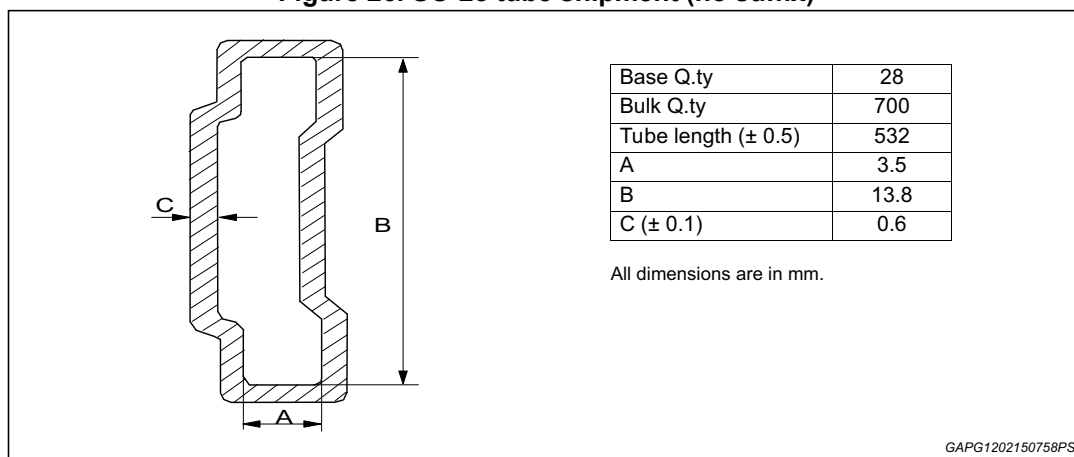
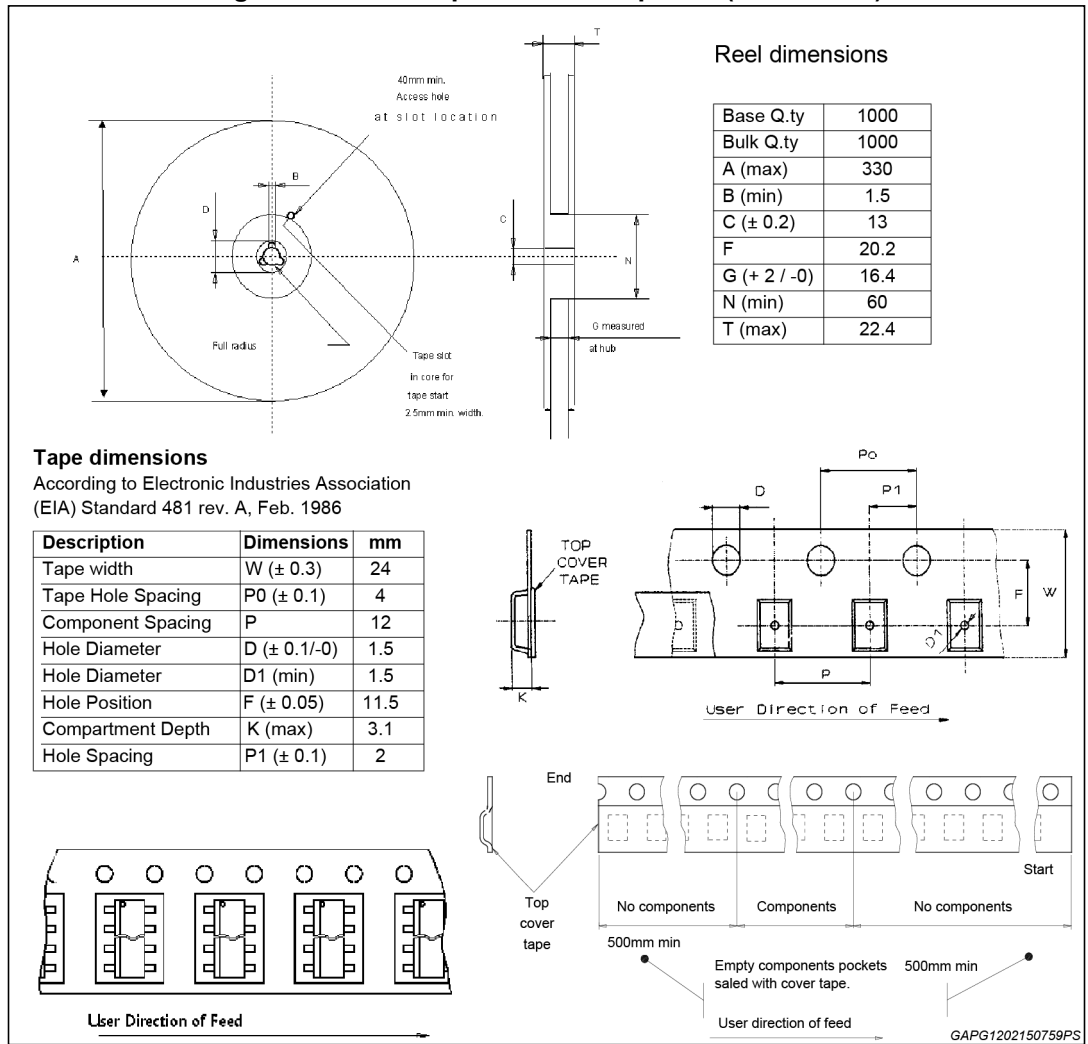




Figure 27. SO-28 tape and reel shipment (suffix "TR")



## 7 Revision history

**Table 16. Document revision history**

Date	Revision	Changes
03-May-2006	1	Initial release.
18-Dec-2008	2	Document reformatted and restructured. Added content, list of figures and tables. Added <i>ECOPACK® packages</i> information.
03-May-2010	3	Changed list.
25-Feb-2011	4	Updated – <i>Figure 13: <math>I_{LIM}</math> vs <math>T_{case}</math></i> – <i>Figure 22: <math>R_{thj-amb}</math> vs PCB copper area in open box free air condition</i>
23-Sep-2013	5	Updated disclaimer.
13-Feb-2015	6	Updated: – <i>Section 6.1: SO-28 package information;</i> – Tape dimensions in <i>Figure 27: SO-28 tape and reel shipment (suffix “TR”) on page 25.</i>

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