

# 8-Bit Serial-Input/Parallel-Output Shift Register

## High-Performance Silicon-Gate CMOS

### MC74HC164A

The MC74HC164A is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

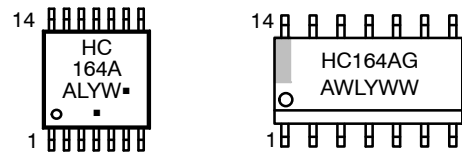
The MC74HC164A is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 V to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 244 FETs or 61 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable\*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



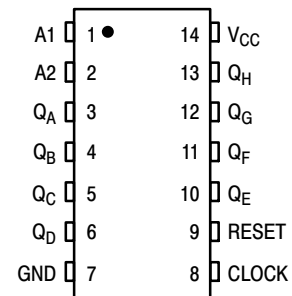
#### MARKING DIAGRAMS



- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or \* = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT



#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74HC164ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74HC164ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC164ADR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC164ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# MC74HC164A

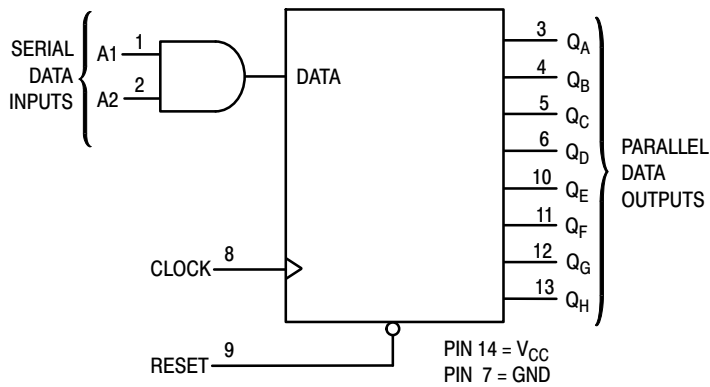


Figure 1. Logic Diagram

## FUNCTION TABLE

Inputs				Outputs			
Reset	Clock	A1	A2	Q <sub>A</sub>	Q <sub>B</sub>	...	Q <sub>H</sub>
L	X	X	X	L	L	...	L
H		X	X	No Change			
H		H	D	D	Q <sub>An</sub>	...	Q <sub>Gn</sub>
H		D	H	D	Q <sub>An</sub>	...	Q <sub>Gn</sub>

D = data input

Q<sub>An</sub> – Q<sub>Gn</sub> = data shifted from the preceding stage on a rising edge at the clock input.

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Package <sup>†</sup> TSSOP Package <sup>†</sup>	500 450	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

<sup>†</sup>Derating — SOIC Package: -7 mW/°C from 65° to 125°C  
TSSOP Package: -6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 5)	2.0	10	10	10	MHz
		3.0	20	20	20	
		4.5	40	35	30	
		6.0	50	45	40	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 2 and 5)	2.0	160	200	250	ns
		3.0	100	150	200	
		4.5	32	40	48	
		6.0	27	34	42	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (Figures 3 and 5)	2.0	175	220	260	ns
		3.0	100	150	200	
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 5)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF	
		180				

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74HC164A

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
$t_{su}$	Minimum Setup Time, A1 or A2 to Clock (Figure 4)	2.0	25	35	40	ns
		3.0	15	20	25	
		4.5	7	8	9	
		6.0	5	6	6	
$t_h$	Minimum Hold Time, Clock to A1 or A2 (Figure 4)	2.0	3	3	3	ns
		3.0	3	3	3	
		4.5	3	3	3	
		6.0	3	3	3	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 3)	2.0	3	3	3	ns
		3.0	3	3	3	
		4.5	3	3	3	
		6.0	3	3	3	
$t_w$	Minimum Pulse Width, Clock (Figure 2)	2.0	50	60	75	ns
		3.0	26	35	45	
		4.5	12	15	20	
		6.0	10	12	15	
$t_w$	Minimum Pulse Width, Reset (Figure 3)	2.0	50	60	75	ns
		3.0	26	35	45	
		4.5	12	15	20	
		6.0	10	12	15	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

## SWITCHING WAVEFORMS

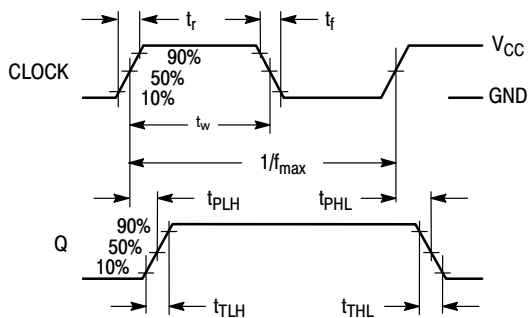


Figure 2.

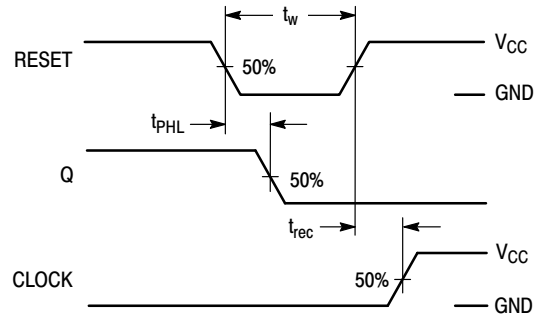


Figure 3.

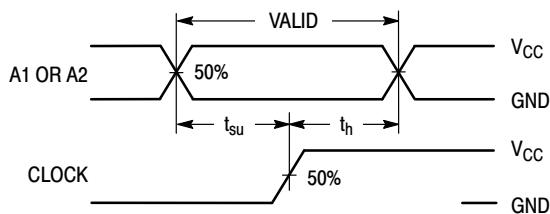
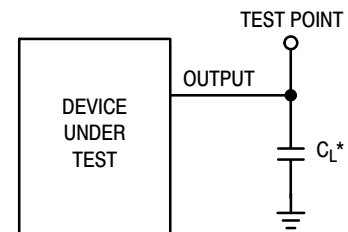


Figure 4.



\*Includes all probe and jig capacitance

Figure 5. Test Circuit

# MC74HC164A

## PIN DESCRIPTIONS

### INPUTS

#### A1, A2 (Pins 1, 2)

Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data-enable input. When only one serial input is used, the other must be connected to  $V_{CC}$ .

#### Clock (Pin 8)

Shift Register Clock. A positive-going transition on this pin shifts the data at each stage to the next stage. The shift register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

### OUTPUTS

#### $Q_A - Q_H$ (Pins 3, 4, 5, 6, 10, 11, 12, 13)

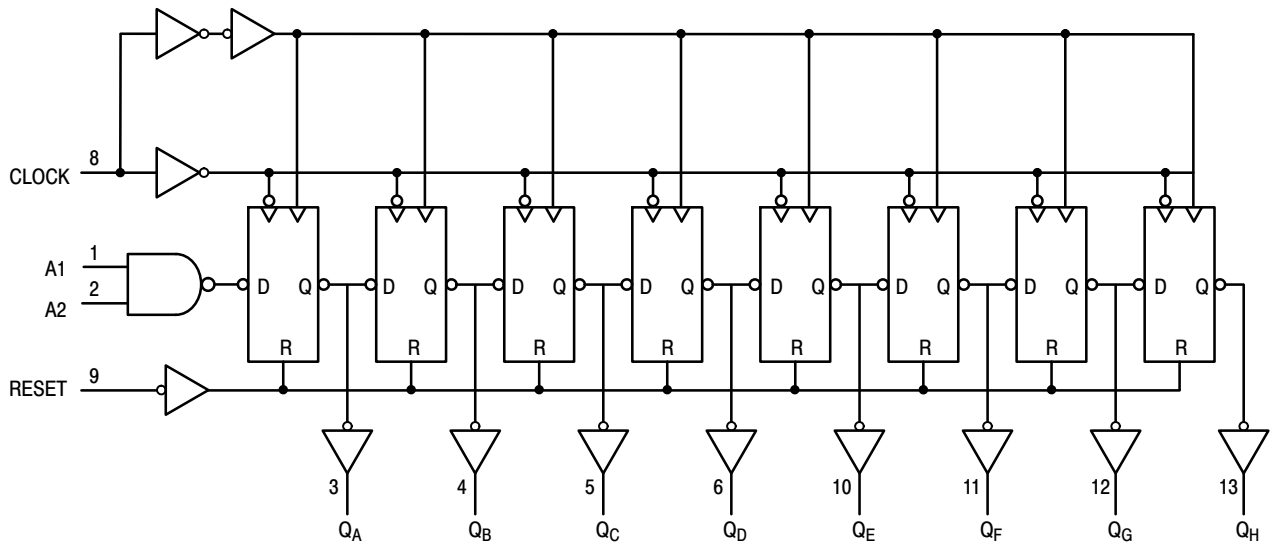
Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

### CONTROL INPUT

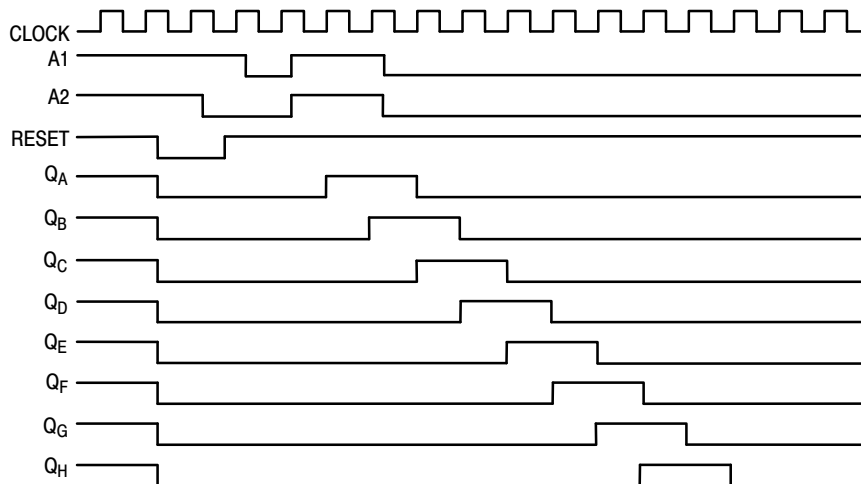
#### Reset (Pin 9)

Active-Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip-flops and sets Outputs  $Q_A - Q_H$  to the low level state.

## EXPANDED LOGIC DIAGRAM



## TIMING DIAGRAM



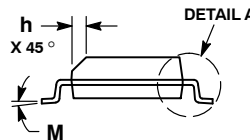
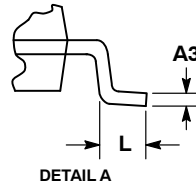
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

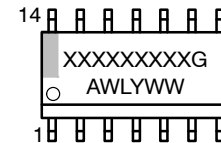
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

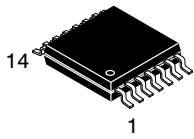
STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

<b>DOCUMENT NUMBER:</b>	<b>98ASB42565B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-14 NB</b>	<b>PAGE 2 OF 2</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***

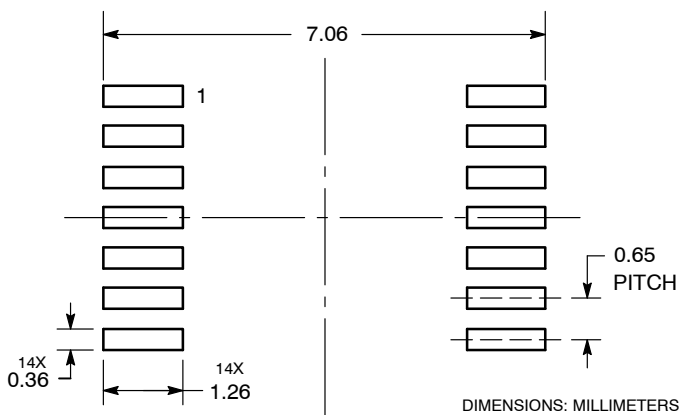


- A = Assembly Location
- L = Wafer Lot
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- W = Work Week
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(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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