May 1996

FAIRCHILD

SEMICONDUCTOR TM

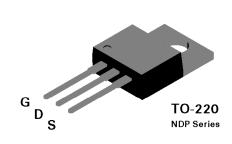
NDP7061 / NDB7061 N-Channel Enhancement Mode Field Effect Transistor

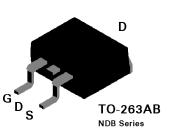
General Description

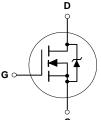
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 64A, 60V. $R_{DS(ON)} = 0.016\Omega @ V_{GS} = 10V.$
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.







Absolute Maximum Ratings T_c = 25°C unless otherwise noted

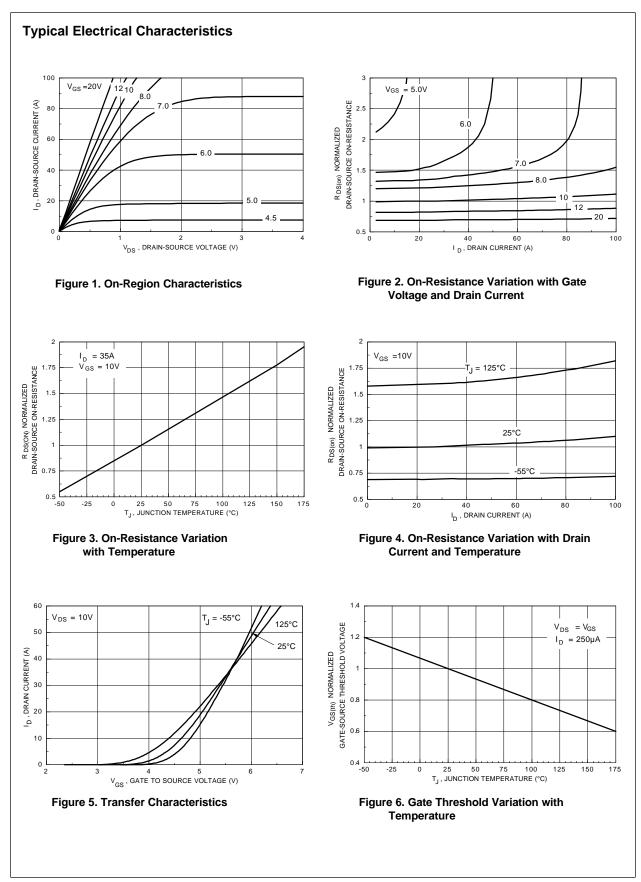
Symbol	Parameter	NDP7061	NDB7061	Units
V _{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \le 1 \text{ M}\Omega$)	60		V
V _{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive ($t_p < 50 \ \mu s$)	± 40		
l _D	Drain Current - Continuous	64		А
	- Pulsed	190		
P _D	Maximum Power Dissipation @ $T_c = 25^{\circ}C$	130		
	Derate above 25°C	0.87		W/°C
T_J,T _{STG}	Operating and Storage Temperature Range	-65 to 175		
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

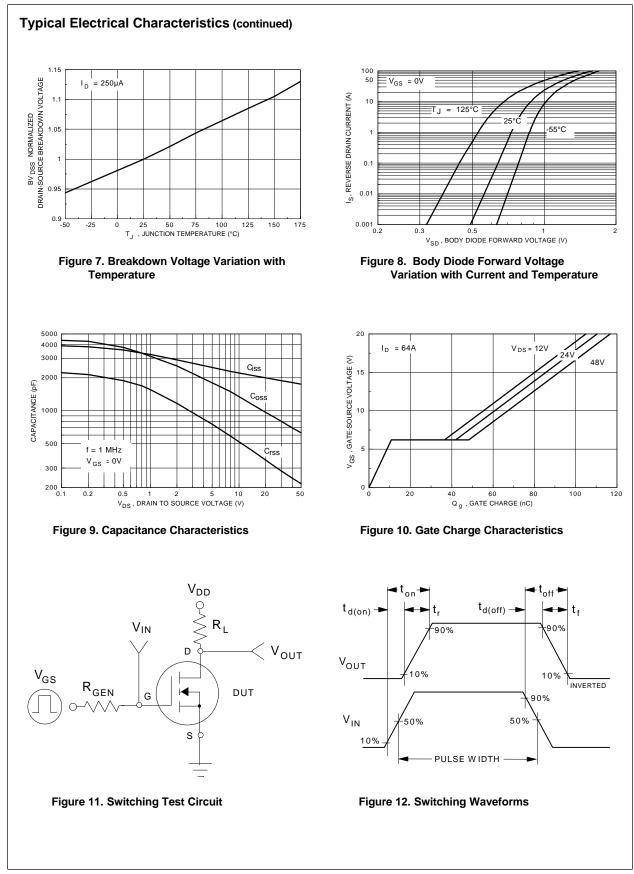
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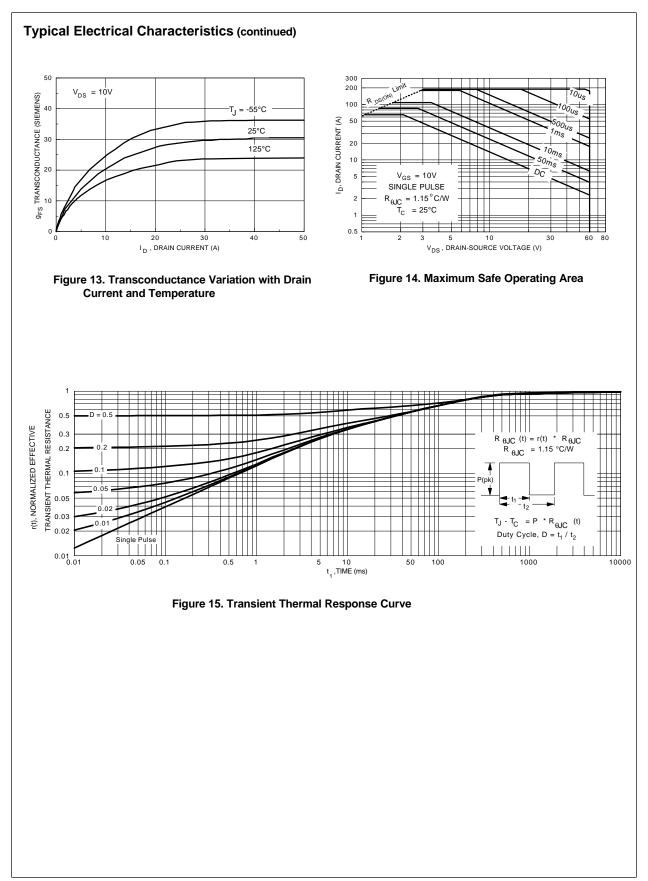
Symbol	Parameter	Conditions		Min	Тур	Max	Units
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30 \text{ V}, \text{ I}_{D} = 64 \text{ A}$				500	mJ
I _{AR}	Maximum Drain-Source Avalanche Curre	ent				64	Α
OFF CH/	ARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		60			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$				10	μA
			T _J = 125°C			1	mA
	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	·			100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHA	RACTERISTICS (Note 1)	·					
V _{GS(th)}	Gate Threshold Voltage	$V_{_{DS}} = V_{_{GS}}, I_{_{D}} = 250 \ \mu A$		2	2.9	4	V
			T _J = 125°C	1.4	2.2	3.6	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 35 \text{ A}$	·		0.013	0.016	Ω
			T _J = 125°C		0.021	0.032	
l _{D(on)}	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$		60			Α
9 _{FS}	Forward Transconductance	$V_{\rm DS} = 10 \text{ V}, I_{\rm D} = 35 \text{ A}$			30		S
DYNAMI	C CHARACTERISTICS	·					
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			1930		pF
C _{oss}	Output Capacitance	f = 1.0 MHz			870		pF
C _{rss}	Reverse Transfer Capacitance	-			310		pF
	NG CHARACTERISTICS (Note 1)			1	1		<u>I</u>
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 25 V, I_{D} = 64 A,$			13	30	nS
t,	Turn - On Rise Time	$V_{\rm GS} = 10 \text{ V}, \text{ R}_{\rm GEN} = 5 \ \Omega$			98	200	nS
t _{D(off)}	Turn - Off Delay Time				36	80	nS
t _f	Turn - Off Fall Time	1			65	150	nS
 Q_	Total Gate Charge	$V_{ps} = 48 V,$			67	100	nC
Q _{gs}	Gate-Source Charge	$V_{DS} = 48 V,$ $I_{D} = 64 A, V_{GS} = 10 V$			11		nC
Q _{gd}	Gate-Drain Charge	1			37.5		nC

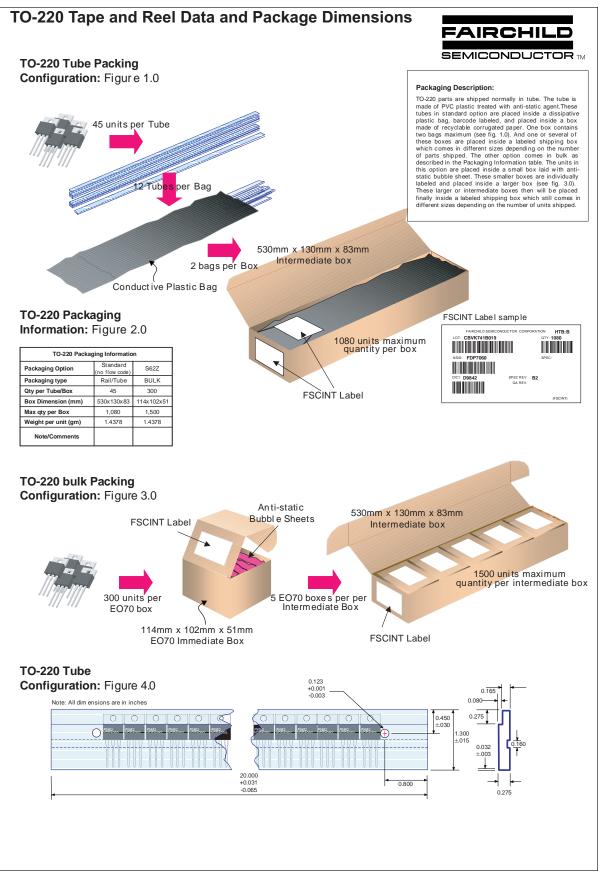
Electrical Characteristics (T _c = 25°C unless otherwise noted)							
Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE DIODE CHARACTERISTICS	-					
I _s	Maximum Continuos Drain-Source Diode Forward Current				64	Α	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				190	Α	
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{S} = 35 \text{ A} (\text{Note 1})$			0.9	1.3	V
			T _J = 125°C		0.8	1.2	
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, \text{ I}_{\text{F}} = 64 \text{ A}, \text{ dI}_{\text{F}}/\text{dt} = 100 \text{ A}/\mu\text{s}$		40	105	150	ns
l _m	Reverse Recovery Current			2	4.5	10	Α
THERMA	L CHARACTERISTICS	·			•		•
R _{θJC}	Thermal Resistance, Junction-to-Case					1.15	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient				62.5	°C/W	
Note:							

Note: 1. Pulse Test: Pulse Width \leq 300 µs, Duty Cycle \leq 2.0%.

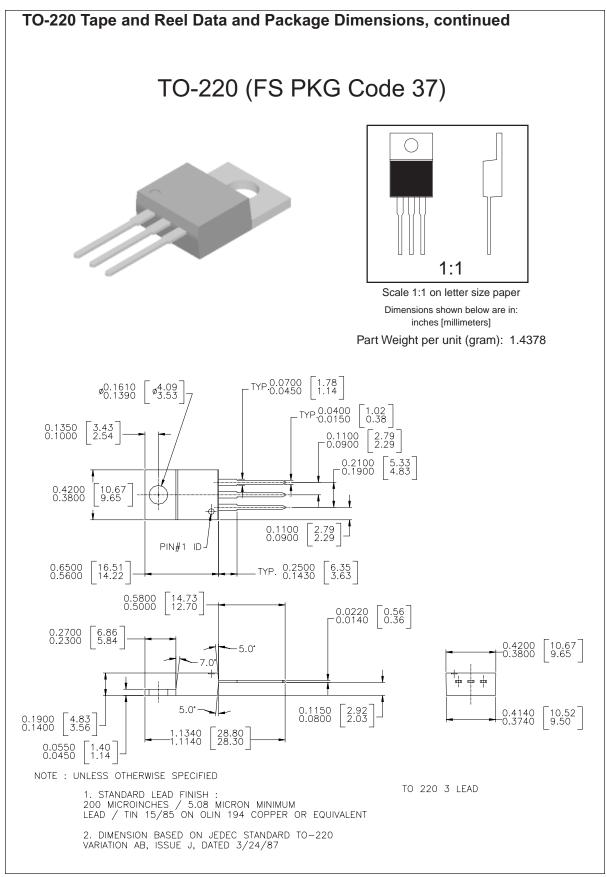




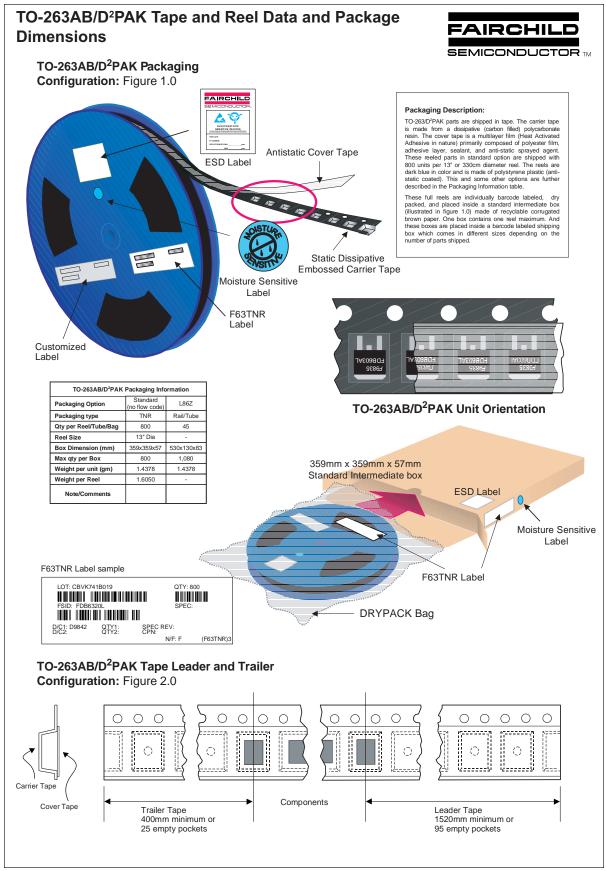




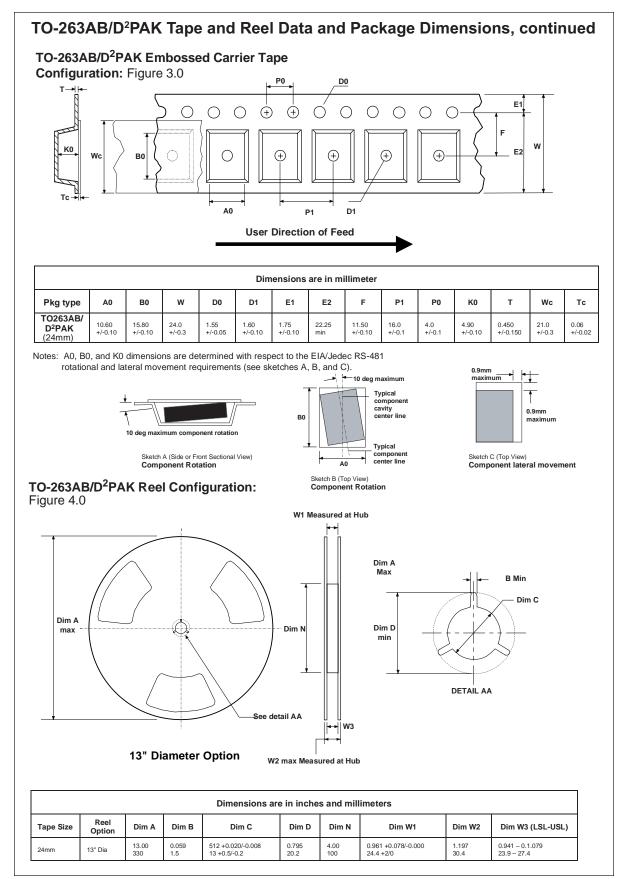
August 1999, Rev. B

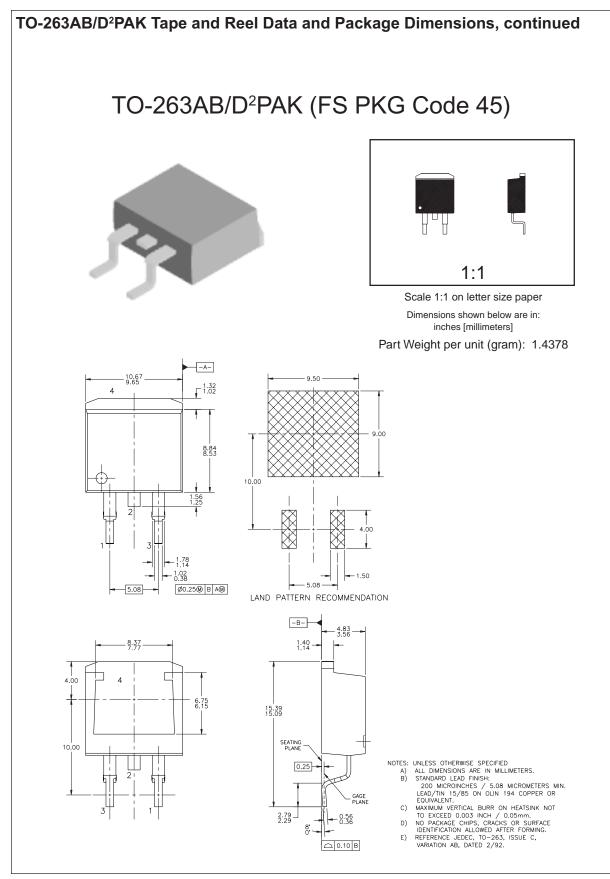


September 1998, Rev. A



September 1999, Rev. B





August 1998, Rev. A

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