Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

October 2006

FDW2508PB
Dual P-Channel –1.8V Specified PowerTrench® MOSFET
–12V, –6A, 18mΩ

Features

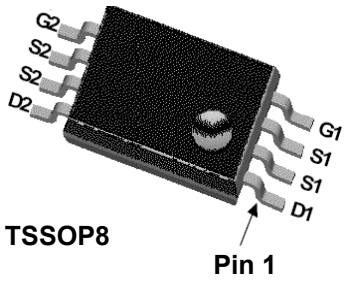
- Max $r_{DS(on)}$ = 18mΩ at V_{GS} = –4.5V, I_D = –6A
- Max $r_{DS(on)}$ = 22mΩ at V_{GS} = –2.5V, I_D = –5A
- Max $r_{DS(on)}$ = 30mΩ at V_{GS} = –1.8V, I_D = –4A
- Low gate charge
- High performance trench technology for extremely low $r_{DS(on)}$
- Low profile TSSOP-8 package
- RoHS compliant

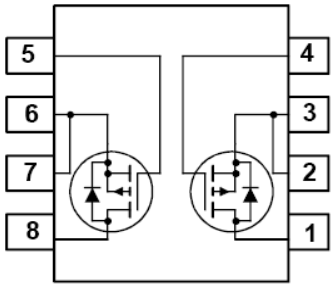
General Description

This P-Channel –1.8V specified MOSFET uses Fairchild Semiconductor's advanced low voltage PowerTrench®. It has been optimized for battery power management applications.

Application

- Power management
- Load switch
- Battery protection





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		–12	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	Drain Current -Continuous	(Note 1a)	–6	A
	-Pulsed		–30	
P_D	Power Dissipation-Dual Operation		2	W
	Power Dissipation-Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	125	

Package Marking and Ordering Information

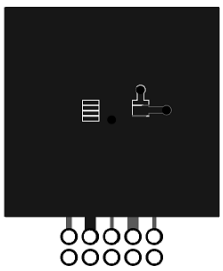
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2508PB	FDW2508PB	TSSOP-8	13"	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = –250μA, V_{GS} = 0V	–12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250μA, referenced to 25°C		–12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –10V, V_{GS} = 0V			–1	μA
		V_{GS} = 0V, T_J = 125°C			–100	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8V, V_{DS} = 0V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = –250μA	–0.4	–0.6	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = –250μA, referenced to 25°C		3		mV/°C
$r_{DS(on)}$	Static Drain to Source On-Resistance	V_{GS} = –4.5V, I_D = –6A		15	18	mΩ
		V_{GS} = –2.5V, I_D = –5A		18	22	
		V_{GS} = –1.8V, I_D = –4A		22	30	
		V_{GS} = –4.5V, I_D = –6A, T_J = 125°C		23	30	
g_{FS}	Forward Transconductance	V_{DS} = –5V, I_D = –6A		35		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –6V, V_{GS} = 0V, f = 1MHz		2835	3775	pF
C_{oss}	Output Capacitance			440	590	pF
C_{rss}	Reverse Transfer Capacitance			370	555	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = –6V, I_D = –6A, V_{GS} = –4.5V, R_{GEN} = 6Ω		8	16	ns
t_r	Rise Time			16	29	ns
$t_{d(off)}$	Turn-Off Delay Time			254	407	ns
t_f	Fall Time			106	170	ns
Q_g	Total Gate Charge	V_{GS} = –4.5V, V_{DD} = –6V, I_D = –6A		32	45	nC
Q_{gs}	Gate to Source Gate Charge			4.3		nC
Q_{gd}	Gate to Drain “Miller” Charge			7.1		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = –1.1A (Note 2)		–0.6	–1.2	V
t_{rr}	Reverse Recovery Time	I_F = –6A, di/dt = 100A/μs		106	159	ns
Q_{rr}	Reverse Recovery Charge			110	165	nC

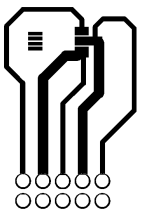
Notes:

1: $R_{\theta JA}$ is the sum of junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as solder mounting surface of the drian pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $R_{\theta JA}$ is 80°C/W(steady state) when mounted on a 1 in^2 pad of 2 oz copper.

Scale 1 : 1 on letter size paper



b.$R_{\theta JA}$ is 125°C/W(steady state) when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

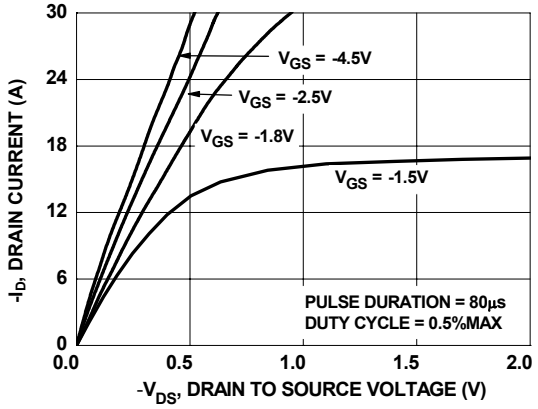


Figure 1. On Region Characteristics

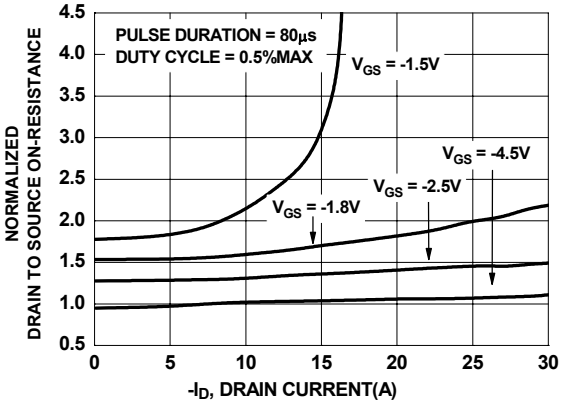


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

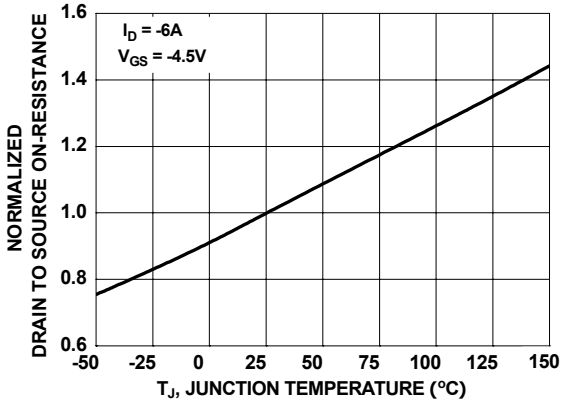


Figure 3. Normalized On Resistance vs Junction Temperature

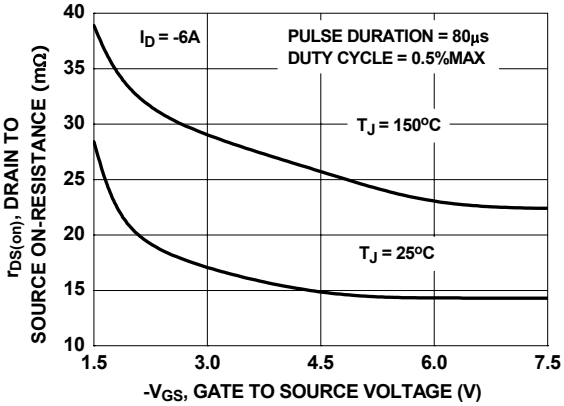


Figure 4. On-Resistance vs Gate to Source Voltage

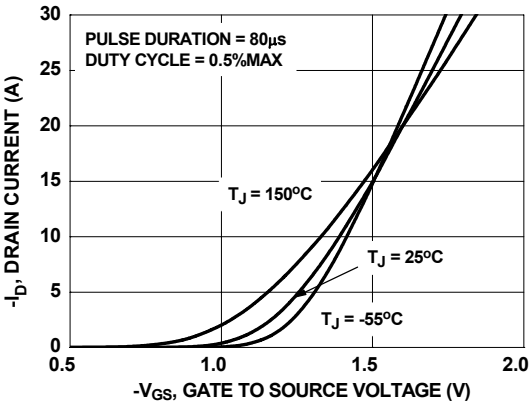


Figure 5. Transfer Characteristics

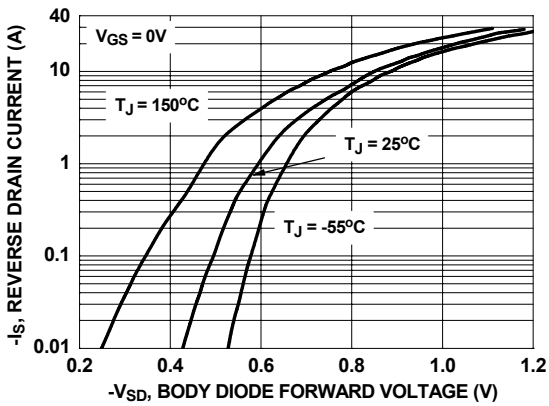


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

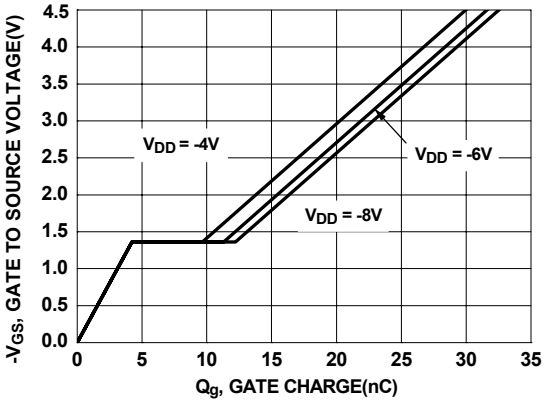


Figure 7. Gate Charge Characteristics

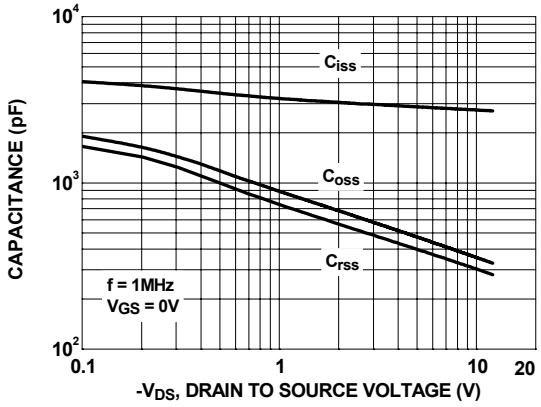


Figure 8. Capacitance vs Drain to Source Voltage

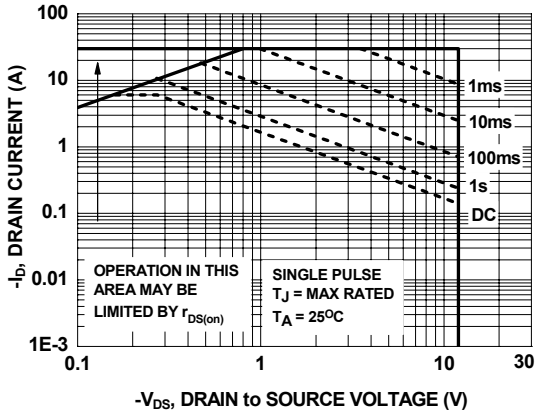


Figure 9. Forward Bias Safe Operating Area

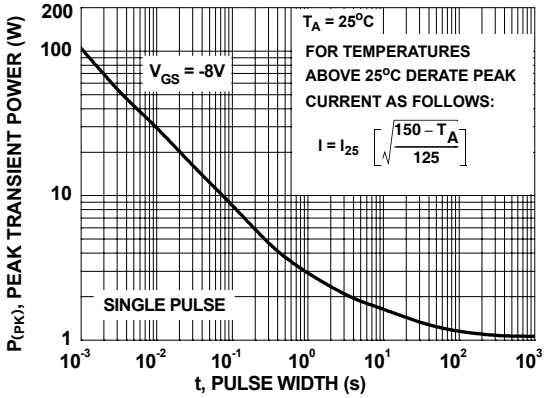


Figure 10. Single Pulse Maximum Power Dissipation

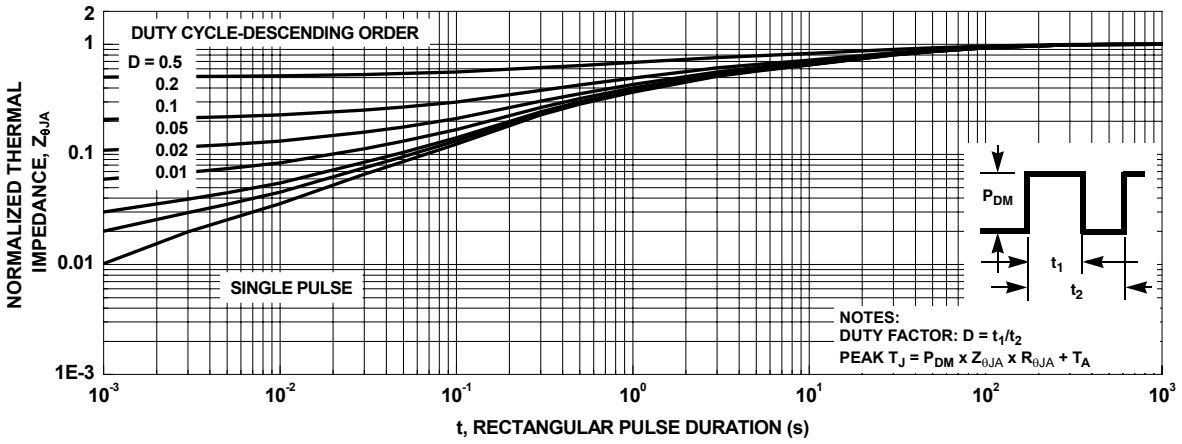
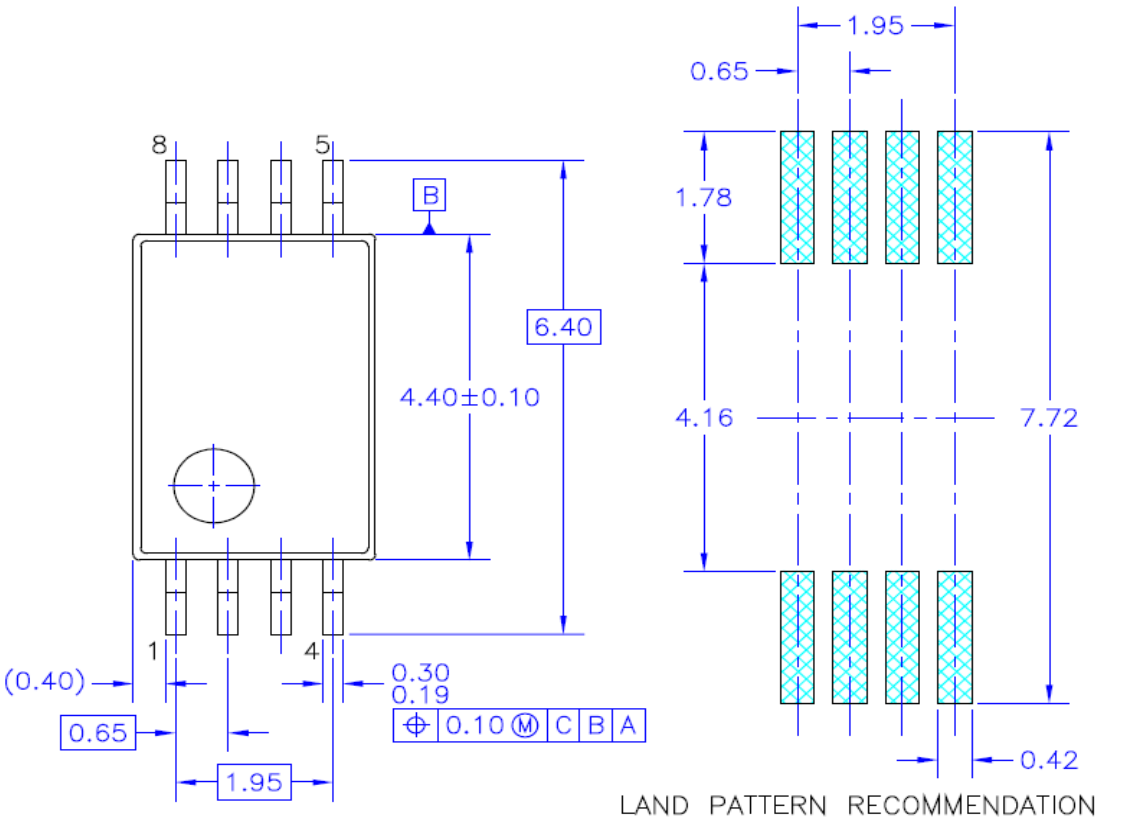
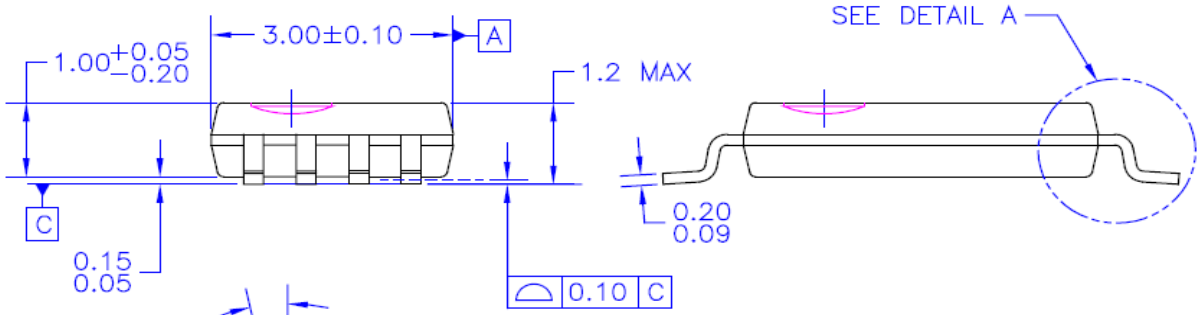
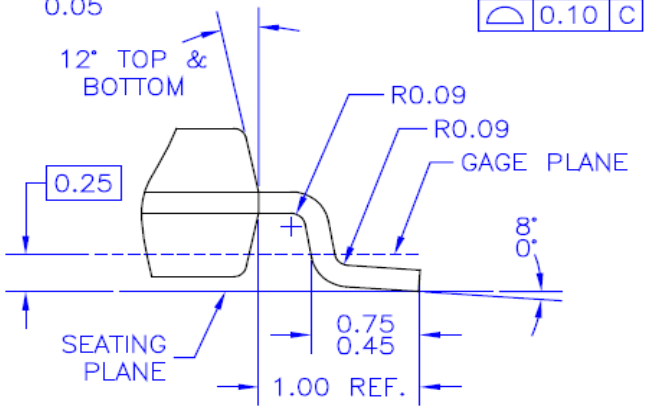


Figure 11. Transient Thermal Response Curve







NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MO–153, ISSUE E, VARIATION AA, DATED OCTOBER 1997.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC08REVB

FAIRCHILD
SEMICONDUCTOR®

FAIRCHILD SEMICONDUCTOR TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT Quiet Series™	OCX™	SILENT SWITCHER®	UniFET™
ActiveArray™	GlobalOptoisolator™	OCXPro™	SMART START™	VCX™
Bottomless™	GTO™	OPTOLOGIC®	SPM™	Wire™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	
CoolFET™	I^2C™	PACMAN™	SuperFET™	
CROSSVOLT™	*i-Lo*™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E^2CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC®	
Programmable Active Droop™				

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative