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December 2013

## IRLS640A

# **N-Channel Logic Level A-FET** 200 V, 9.8 A, 180 mΩ

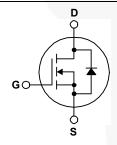
### **Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, DC-AC converters for uninterrupted power supply and motor control.

#### **Features**

- 9.8 A, 200 V,  $R_{DS(on)}$  = 180 m $\Omega$  @  $V_{GS}$  = 5 V Low Gate Charge (Typ. 40 nC)
- Low Crss (Typ. 95 pF)
- Fast Switching
- 100% Avalanche Tested
- · Improved dv/dt Capability
- · Logic-Level Gate Drive





# **Absolute Maximum Ratings**

Symbol	Characteristic	Value	Units	
$V_{DSS}$	Drain-to-Source Voltage	200	V	
,	Continuous Drain Current (T <sub>C</sub> =25°C)	9.8		
l <sub>D</sub>	Continuous Drain Current (T <sub>C</sub> =100 °C)	6.2	Α	
I <sub>DM</sub>	Drain Current-Pulsed ①	63	Α	
$V_{GS}$	Gate-to-Source Voltage	±20	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy ②	64	mJ	
I <sub>AR</sub>	Avalanche Current ①	18	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy ①	4.0	mJ	
dv/dt	Peak Diode Recovery dv/dt 3	5	V/ns	
	Total Power Dissipation (T <sub>C</sub> =25℃)	40	W	
$P_{D}$	Linear Derating Factor	0.32	W/℃	
	Operating Junction and	FF 1: .450		
$T_J$ , $T_STG$	Storage Temperature Range	- 55 to +150		
	Maximum Lead Temp. for Soldering	200	°C	
TL	Purposes, 1/8 " from case for 5-seconds	300		

### Thermal Resistance

Symbol	Characteristic	Тур.	Max.	Units
$R_{ heta JC}$	Junction-to-Case		3.13	0000
$R_{\theta JA}$	Junction-to-Ambient		62.5	°C/W

### **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
IRLS640A	IRLS640A	TO-220F	Tube	N/A	N/A	50 units

# **Electrical Characteristics** (T<sub>C</sub>=25 °C unless otherwise specified)

Symbol	Characteristic		Тур.	Max.	Units	Test Condition	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage		-		V	V <sub>GS</sub> =0V,I <sub>D</sub> =250μA	
$\Delta$ BV/ $\Delta$ T $_{ m J}$	Breakdown Voltage Temp. Coeff.		0.17	-	V/°C	I <sub>D</sub> =250μA <b>See Fig 7</b>	
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1	2.0	٧	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	
	Gate-Source Leakage, Forward			100	nA	V <sub>GS</sub> =20V	
I <sub>GSS</sub>	Gate-Source Leakage, Reverse			-100	IIA	V <sub>GS</sub> =-20V	
	Design to Course I asked Course	1	1	10		V <sub>DS</sub> =200V	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	1	1	100	μ <b>A</b>	$V_{DS}$ =160V, $T_{C}$ =125 $^{\circ}$ C	
R <sub>DS(on)</sub>	Static Drain-Source On-State Resistance	1	1	0.18	Ω	V <sub>GS</sub> =5V,I <sub>D</sub> =4.9A	
$g_{fs}$	Forward Transconductance	-	13.3	-	S	V <sub>DS</sub> =40V,I <sub>D</sub> =4.9A 4	
C <sub>iss</sub>	Input Capacitance	1	1310	1705		\\ -0\\\\ -0\\\\	
C <sub>oss</sub>	Output Capacitance	-	200	250	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$	
C <sub>rss</sub>	Reverse Transfer Capacitance	-	95	120		See Fig 5	
t <sub>d(on)</sub>	Turn-On Delay Time	-	11	30		\/ -100\/ I -10A	
t <sub>r</sub>	Rise Time		8	25		V <sub>DD</sub> =100V,I <sub>D</sub> =18A,	
$t_{d(off)}$	Turn-Off Delay Time	-	46	100	ns	$R_G=4.6\Omega$	
t <sub>f</sub>	Fall Time		15	40		See Fig 13 4 5	
$Q_g$	Total Gate Charge		40	56		V <sub>DS</sub> =160V,V <sub>GS</sub> =5V,	
$Q_{gs}$	Gate-Source Charge		6.8		nC	I <sub>D</sub> =18A	
$Q_{gd}$	Gate-Drain("Miller") Charge		18.6			See Fig 6 & Fig 12 4 5	

# Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition
I <sub>S</sub>	Continuous Source Current	1	-	18	_	Integral reverse pn-diode
I <sub>SM</sub>	Pulsed-Source Current ①			63	Α	in the MOSFET
$V_{SD}$	Diode Forward Voltage 4			1.5	٧	T <sub>J</sub> =25°C,I <sub>S</sub> =9.8A,V <sub>GS</sub> =0V
t <sub>rr</sub>	Reverse Recovery Time	-	224	-	ns	T <sub>J</sub> =25℃,I <sub>F</sub> =18A
$Q_{rr}$	Reverse Recovery Charge	1	1.55	-	μC	di <sub>F</sub> /dt=100A/µs 4

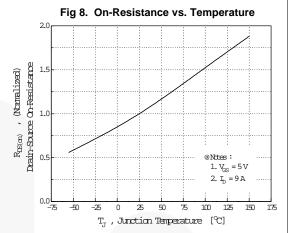
#### Notes:

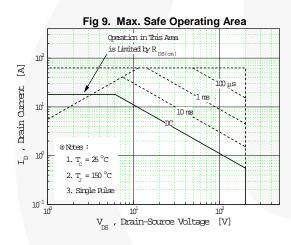
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- (2) L=1mH,  $I_{AS}$ =9.8A,  $V_{DD}$ =50V,  $R_{G}$ =27 $\Omega$ , Starting  $T_{J}$ =25  $^{\circ}$ C (3)  $I_{SD}$ ≤18A, di/dt≤260A/ $\mu$ s,  $V_{DD}$ ≤BV $_{DSS}$ , Starting  $T_{J}$ =25  $^{\circ}$ C (4) Pulse Test : Pulse Width = 250 $\mu$ s, Duty Cycle ≤ 2%
- 5 Essentially Independent of Operating Temperature

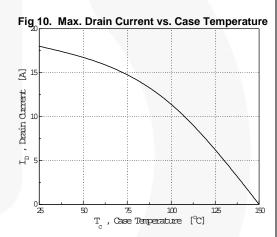
#### **Typical Characteristics** Fig 1. Output Characteristics Fig 2. Transfer Characteristics 7.0V 6.0V 5.5V Z Ø 5.0V 4.5V 4.0V Drain Current , Drain Current 150 °C 3.5V Battom: 3.0V 100 @ Notes : 1. $V_{GS} = 0 V$ H 2. V<sub>DS</sub> = 40 V 10 1. 250 μs Pulse 1 3. 250 $\mu s$ Pulse Test 2. T = 25 °C 10-1 V<sub>DS</sub> , Drain-Source Voltage [V] $V_{\!_{C\!S}}$ , Gate—Source Voltage [V] Fig 3. On-Resistance vs. Drain Current Fig 4. Source-Drain Diode Forward Voltage $\overline{A}$ Drain-Source On-Resistance Reverse Drain Current 10 [Ω], 100 0.1 @ Notes : 1. $V_{GS} = 0 V$ @Note: $T_J = 25$ °C 2. 250 μs Pulse Test 10-1 0.0 0.4 1.0 1.4 I<sub>D</sub> , Drain Current [A] V<sub>SD</sub> , Source-Drain Voltage [V] Fig 5. Capacitance vs. Drain-Source Voltage Fig 6. Gate Charge vs. Gate-Source Voltage 2000 $V_{DS} = 40 \text{ V}$ 1600 $\geq$ $V_{DS} = 100 \text{ V}$ P $V_{\mathbb{G}}$ , Gate-Source Voltage $V_{DS} = 160 \text{ V}$ Capacitance 800 @Notes: 1. $V_{GS} = 0 \text{ V}$ 2. f = 1 MHz400 @ Notes : $I_D = 18 A$ 0 L Q<sub>g</sub> , Total Gate Charge [nC] $\mathbf{V}_{\!\!\! \mathrm{DS}}$ , Drain-Source Voltage [V]

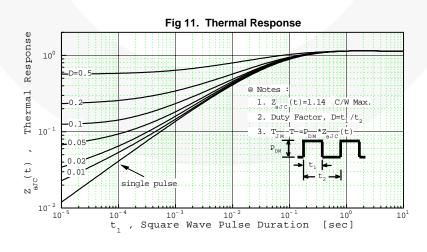
# Typical Characteristics (continued)

Fig 7. Breakdown Voltage vs. Temperature  $\begin{array}{c} 1.2 \\ \hline \\ 0.0 \\ \hline 0.0 \\ \hline \\ 0.0 \\ \hline \\ 0.0 \\ \hline \\ 0.0 \\ \hline \\ 0.0 \\ \hline \\$ 









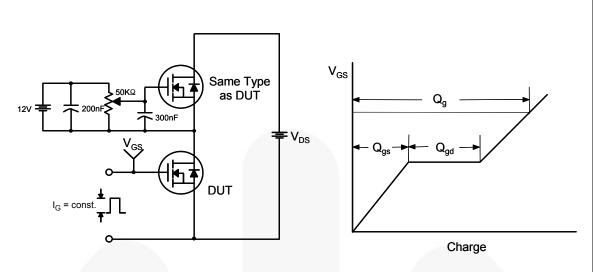


Figure 12. Gate Charge Test Circuit & Waveform

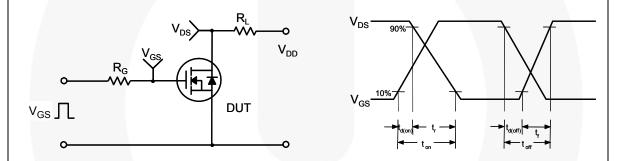


Figure 13. Resistive Switching Test Circuit & Waveforms

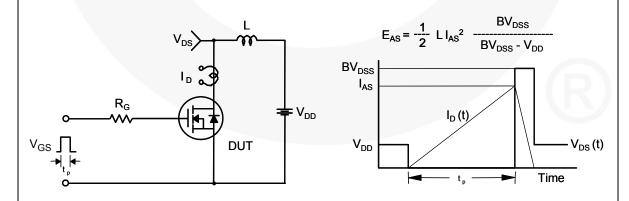
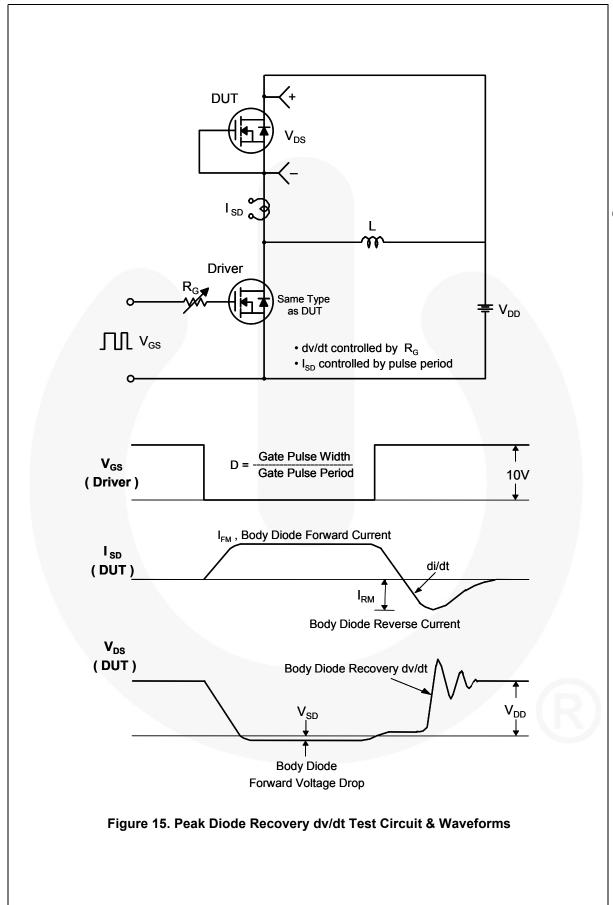


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



### **Mechanical Dimensions**

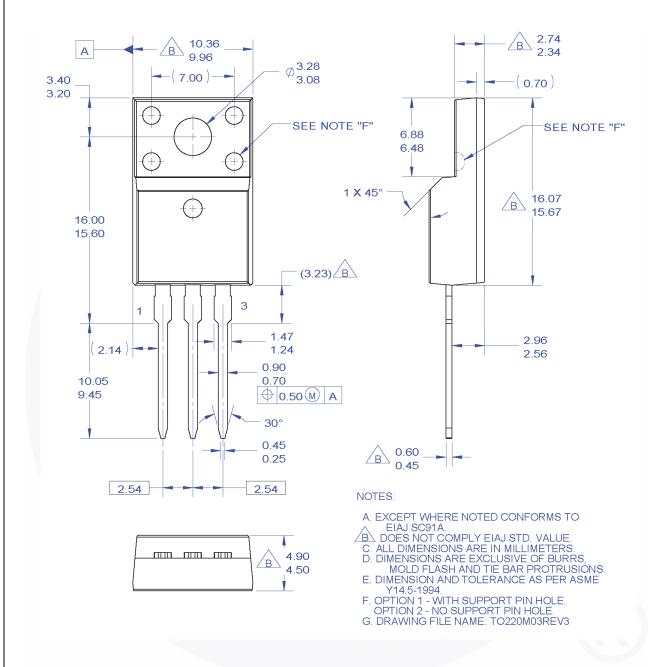


Figure 16. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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