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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

April 2010

FQB25N33TM_F085
330V N-Channel MOSFET

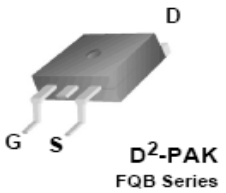
Features

- 25A, 330V, $R_{DS(on)}$ = 0.23Ω @V_{GS} = 10V
- Low gate charge (typical 58nC)
- Low Crss (typical 40pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Qualified to AEC Q101
- RoHS Compliant

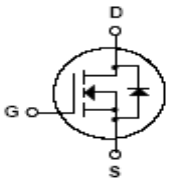
General Description

These N-Channel enhancement mode power field effect transistors are produced using Farichild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimized on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



D²-PAK
FQB Series



Absolute Maximum Ratings

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		330	V
I_D	Drain Current - Continuous (T_C = 25°C)		25	A
	- Continuous (T_C = 100°C)		16.0	A
I_{DM}	Drain Current - Pulsed	(Note 1)	100	A
V_{GSS}	Gate -Source Voltage		±30	V
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	370	mJ
I_{AR}	Avalanche Current	(Note 1)	25	A
E_{AR}	Repetitive Avalance Energy	(Note 1)	37	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		3.1	W
	Power Dissipation (T_C = 25°C)		250	W
	- Derate above 25°C		2.0	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8 from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient *	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	°C/W

*** When mounted on the minimum pad size recommended (PCB Mount)**

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB25N33	FQB25N33TM_F085	D2-PAK	330mm	24mm	800

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	330	--	--	V
$\Delta B_{VDSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	--	0.34	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 330V,V_{GS} = 0V	--	--	1	μA
		V_{DS} = 264V,T_C =125°C	--	--	10	
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30V, V_{DS} = 0V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Forward	V_{GS} = -30V, V_{DS} = 0V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	3.0	--	5.0	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 12.5A,	--	0.18	0.23	Ω
g_{FS}	Forward Transonductance	V_{DS} = 50V, I_D = 12.5A, (Note 4)	--	1	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	--	1510	2010	pF
C_{oss}	Output Capacitance		--	290	385	pF
C_{rss}	Reverse Transfer Capacitance		--	40	60	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 165V, I_D = 25A, R_{GS} = 25Ω (Note 4, 5)	--	20	35	ns
t_r	Turn-On Rise Time		--	100	160	ns
$t_{d(off)}$	Turn-Off Delay Time		--	90	145	ns
t_f	Turn-Off Fall Time		--	70	110	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{DS} = 297V, I_D = 25A, V_{GS} = 15V, (Note 4, 5)	--	58	75	nC
Q_{gs}	Gate to Source Gate Charge		--	11.2	--	nC
Q_{gd}	Gate to Drain Charge		--	21	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	25	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	100	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0, I_S = 25A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0, I_S = 25A, dI_F/dt = 100A/μs (Note 4)	--	275	--	ns
Q_{rr}	Reverse Recovery Charge		--	3.6	--	μC

Notes:
1: Repetitive Rating : Pluse width Limited by maximum junction temperature
2: L = 1.79mH, I_{AS} = 25A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3: I_{SD} ≤ 25A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4: Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5: Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

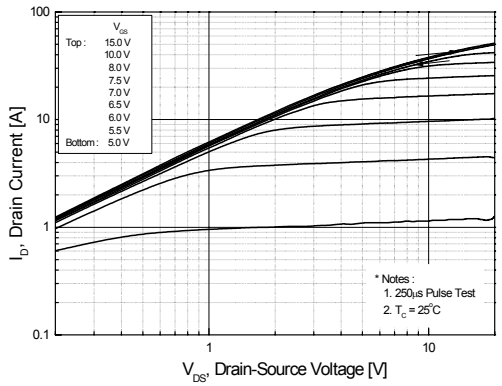


Figure 2. Transfer Characteristics

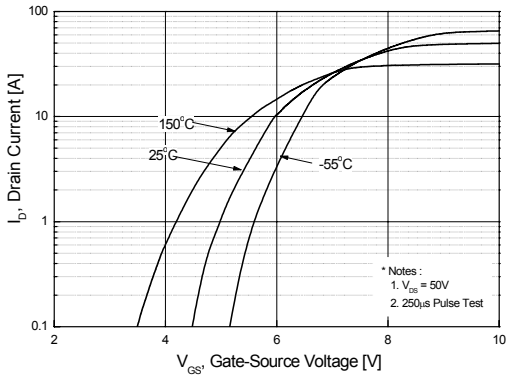


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

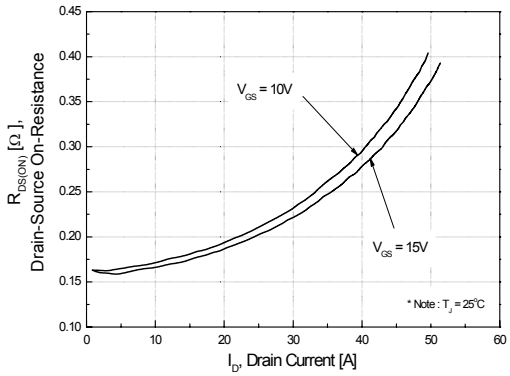


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

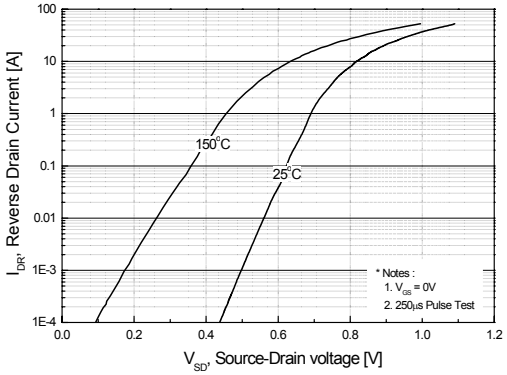


Figure 5. Capacitance Characteristics

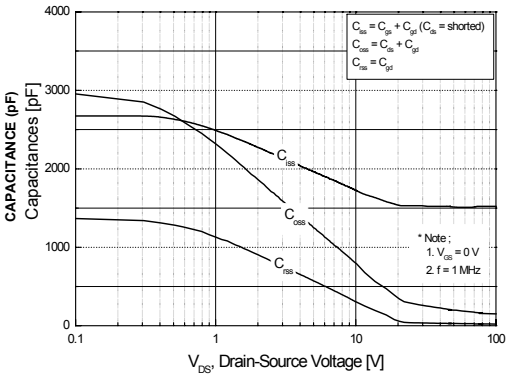
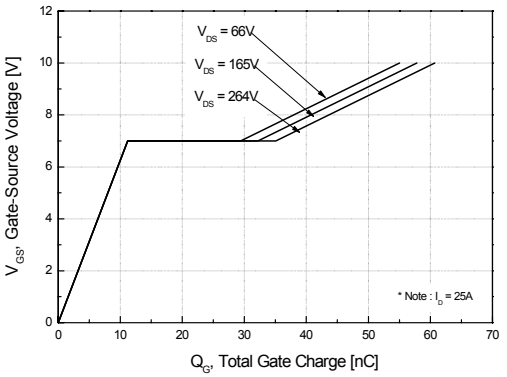


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

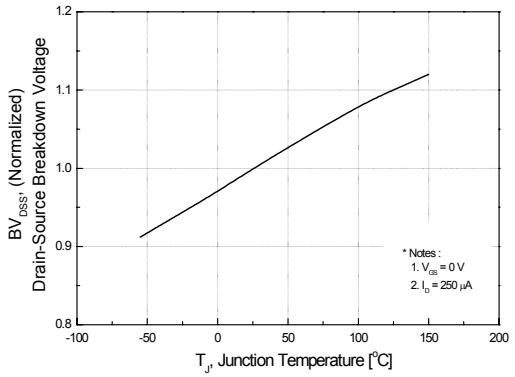


Figure 8. On-Resistance Variation vs. Temperature

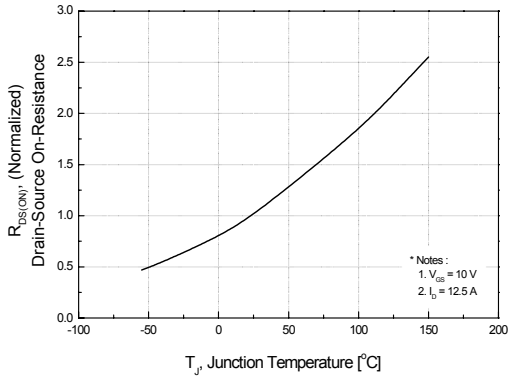


Figure 9. Maximum Safe Operating Area

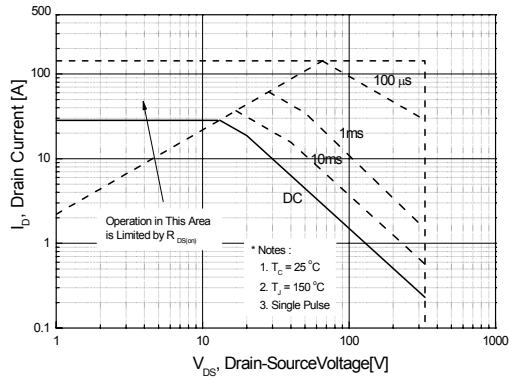


Figure 10. Maximum Drain Current vs. Case Temperature

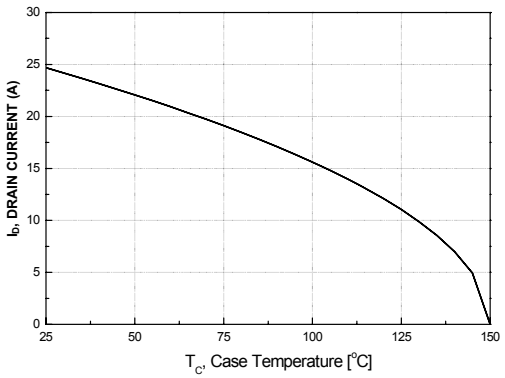
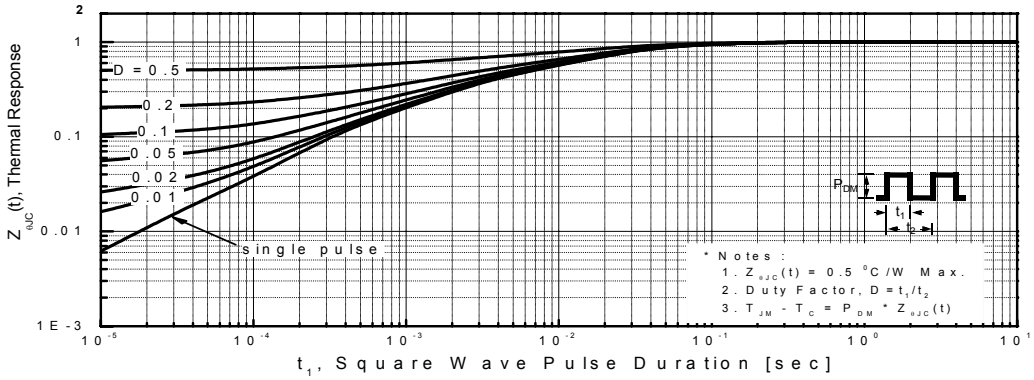
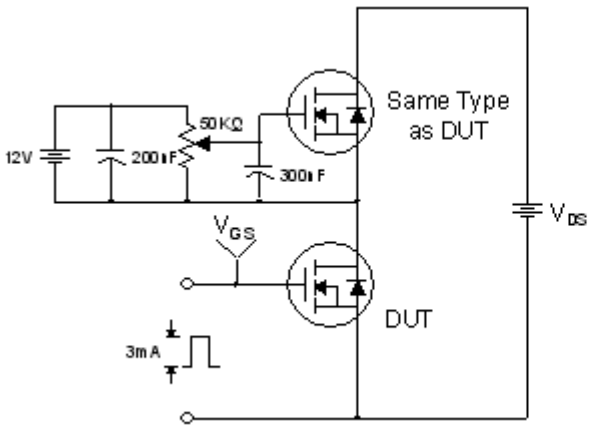
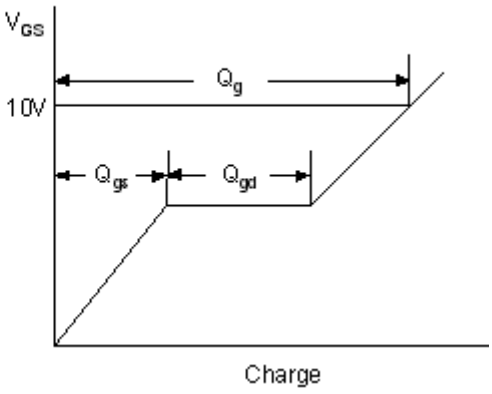


Figure 11. Transient Thermal Response Curve

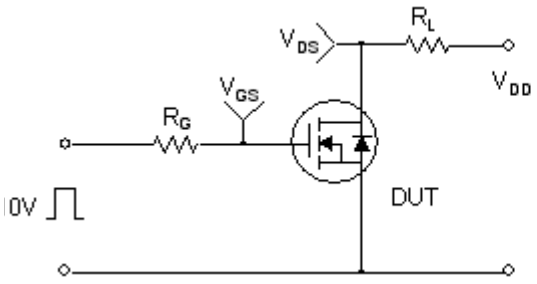


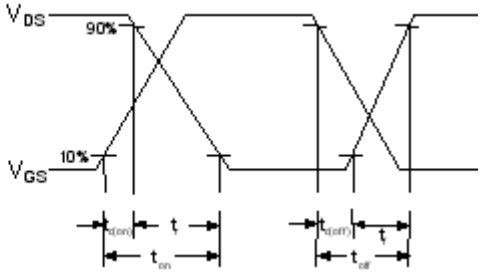
Gate Charge Test Circuit & Waveform



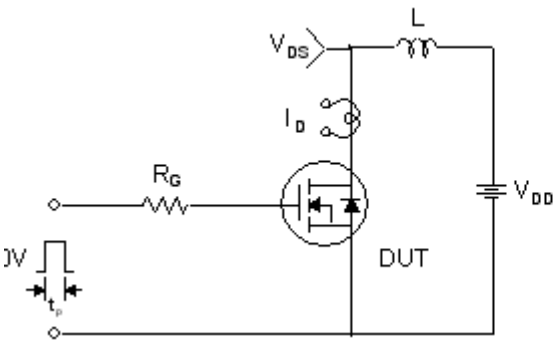


Resistive Switching Test Circuit & Waveforms

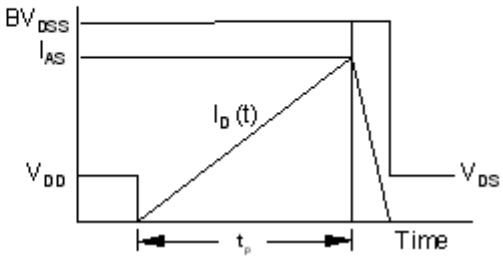




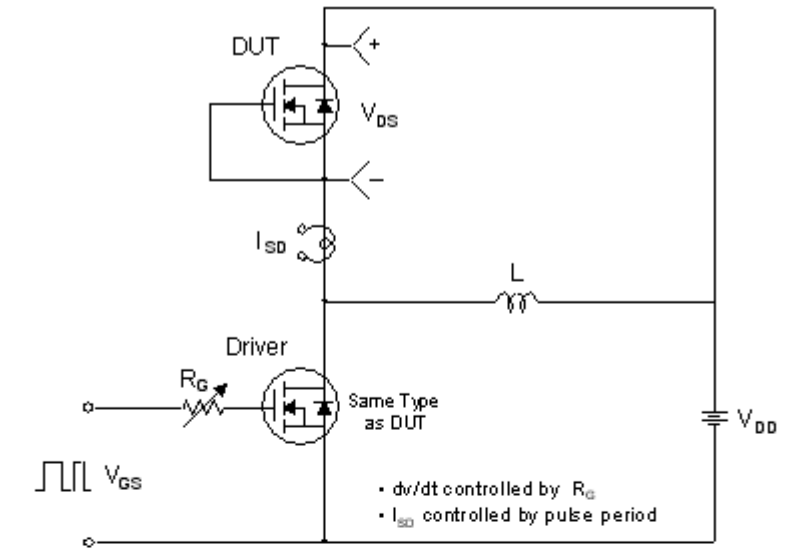
Unclamped Inductive Switching Test Circuit & Waveforms

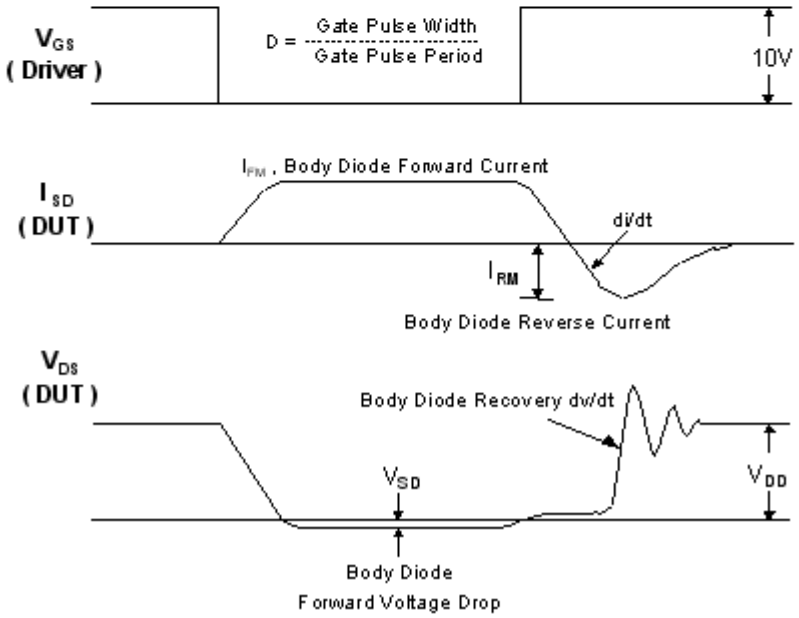


$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I48

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