74HC3G07; 74HCT3G07

Triple buffer with open-drain outputs

Rev. 5 — 24 January 2019 Product data sheet

1. General description

The 74HC3G07; 74HCT3G07 is a triple buffer with open-drain outputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
  - For 74HC3G07: CMOS level
  - For 74HCT3G07: TTL level
- Complies with JEDEC standard no. 7 A
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC3G07DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HCT3G07DP				
74HC3G07DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HCT3G07DC				

4. Marking

Table 2. Marking code

Type number	Marking code [1]
74HC3G07DP	H07
74HCT3G07DP	T07
74HC3G07DC	H07
74HCT3G07DC	T07

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

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5. Functional diagram

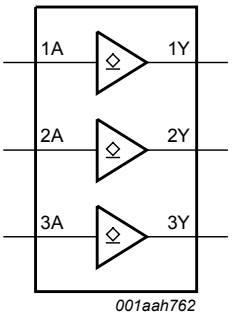

Fig. 1. Logic symbol

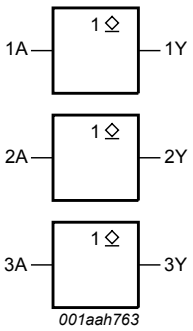

Fig. 2. IEC logic symbol

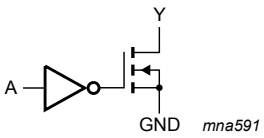

Fig. 3. Logic diagram (one buffer)

6. Pinning information

6.1. Pinning

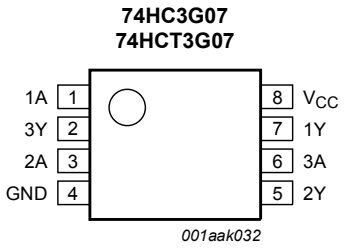

Fig. 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V_{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input nA	Output nY
L	L
H	Z

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V	[1]	-20	-	mA
V_O	output voltage	active mode	[1]	-0.5	$V_{CC} + 0.5$	V
		high-impedance mode	[1]	-0.5	7.0	V
I_O	output current	V_O = -0.5 V to 7.0 V	[1]	-25	-	mA
I_{CC}	supply current		[1]	-	50	mA
I_{GND}	ground current		[1]	-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_D	dynamic power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC3G07			74HCT3G07			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	6.0	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

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10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
74HC3G07								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	μA
I_{LO}	output leakage current	V_I = V_{IH}; V_O = V_{CC} or GND	-	-	±5.0	-	±10	μA
I_{CC}	supply current	per input pin; V_{CC} = 6.0 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	10	-	20	μA
C_I	input capacitance		-	1.5	-	-	-	pF
74HCT3G07								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	-	±1.0	μA
I_{LO}	output leakage current	V_I = V_{IH}; V_O = V_{CC} or GND	-	-	±5.0	-	±10	μA
I_{CC}	supply current	per input pin; V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	10	-	20	μA
ΔI_{CC}	additional supply current	per input; V_{CC} = 4.5 V to 5.5 V; V_I = V_{CC} - 2.1 V; I_O = 0 A	-	-	375	-	410	μA
C_I	input capacitance		-	1.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

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11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
74HC3G07								
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 5						
		V_{CC} = 2.0 V	-	25	95	-	125	ns
		V_{CC} = 4.5 V	-	9	19	-	25	ns
		V_{CC} = 6.0 V	-	7	16	-	20	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 5						
		V_{CC} = 2.0 V	-	25	95	-	125	ns
		V_{CC} = 4.5 V	-	11	23	-	30	ns
		V_{CC} = 6.0 V	-	10	23	-	26	ns
t_{THL}	HIGH to LOW output transition time	nY; see Fig. 5						
		V_{CC} = 2.0 V	-	18	95	-	125	ns
		V_{CC} = 4.5 V	-	6	19	-	25	ns
		V_{CC} = 6.0 V	-	5	16	-	20	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [2]	-	4	-	-	-	pF
74HCT3G07								
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; V_{CC} = 4.5 V; see Fig. 5	-	11	27	-	32	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; V_{CC} = 4.5 V; see Fig. 5	-	10	26	-	31	ns
t_{THL}	HIGH to LOW output transition time	nY; V_{CC} = 4.5 V; see Fig. 5	-	6	19	-	22	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} - 1.5 V [2]	-	4		-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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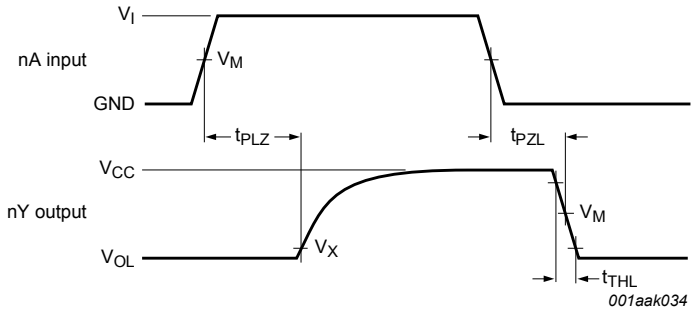
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} is the typical output voltage level that occurs with the output load.

Fig. 5. The input (nA) to output (nY) propagation delays

Table 9. Measurement points

Type	Input	Output	
	V_M	V_M	V_X
74HC3G07	0.5 × V_{CC}	0.5 × V_{CC}	0.1 × V_{CC}
74HCT3G07	1.3 V	1.3 V	0.1 × V_{CC}

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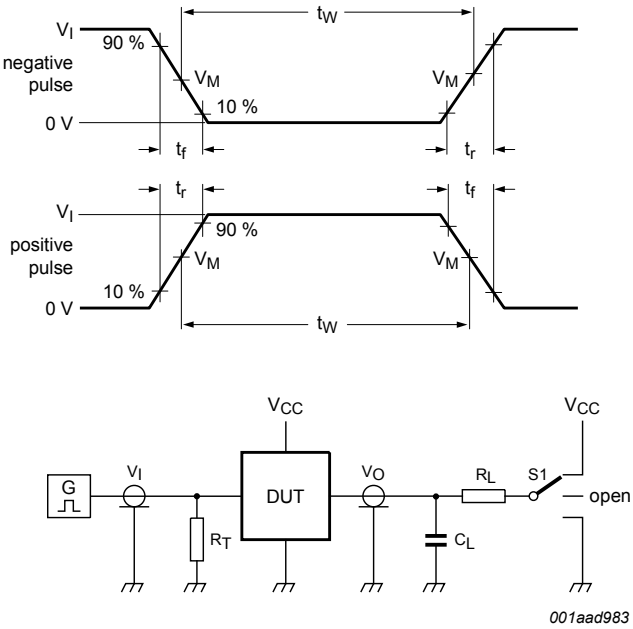

Test data is given in Table 10.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PZL}, t_{PLZ}
74HC3G07	GND to V_{CC}	≤ 6 ns	50 pF	1 kΩ	V_{CC}
74HCT3G07	GND to 3 V	≤ 6 ns	50 pF	1 kΩ	V_{CC}

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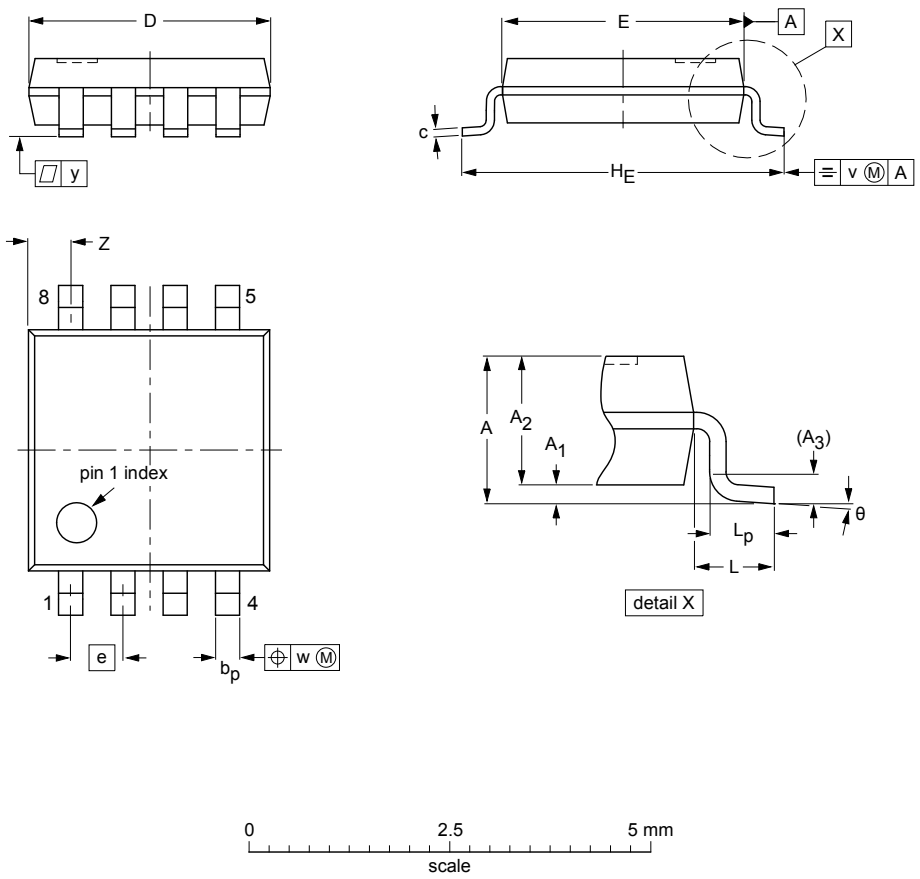
12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig. 7. Package outline SOT505-2 (TSSOP8)

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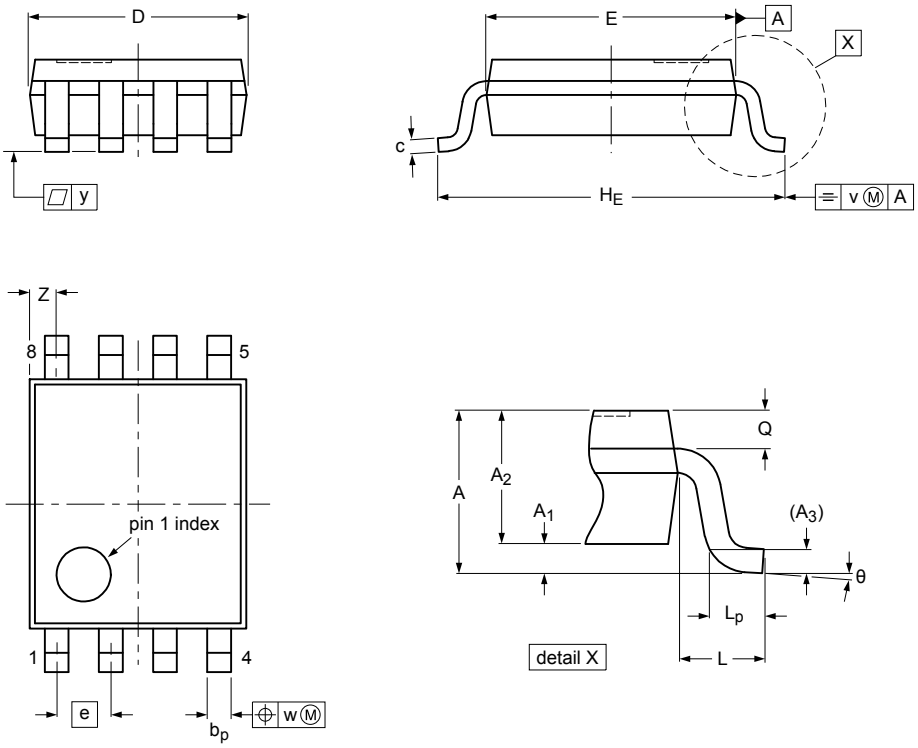
VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
mm nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 8. Package outline SOT765-1 (VSSOP8)

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13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT3G07 v.5	20190124	Product data sheet	-	74HC_HCT3G07 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC3G07GD and 74HCT3G07GD (SOT996-2) removed. • Package outline drawing SOT765-1 (VSSOP8) updated.			
74HC_HCT3G07 v.4	20131216	Product data sheet	-	74HC_HCT3G07 v.3
Modifications:	• Features and benefits updated (errata).			
74HC_HCT3G07 v.3	20130814	Product data sheet	-	74HC_HCT3G07 v.2
Modifications:	• For type numbers 74HC3G07GD and 74HCT3G07GD XSON8U has changed to XSON8.			
74HC_HCT3G07 v.2	20090512	Product data sheet	-	74HC_HCT3G07 v.1
74HC_HCT3G07 v.1	20031015	Product specification	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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