

Advanced HD AVC processor with integrated low power standby controller for entry market

Data brief

Features

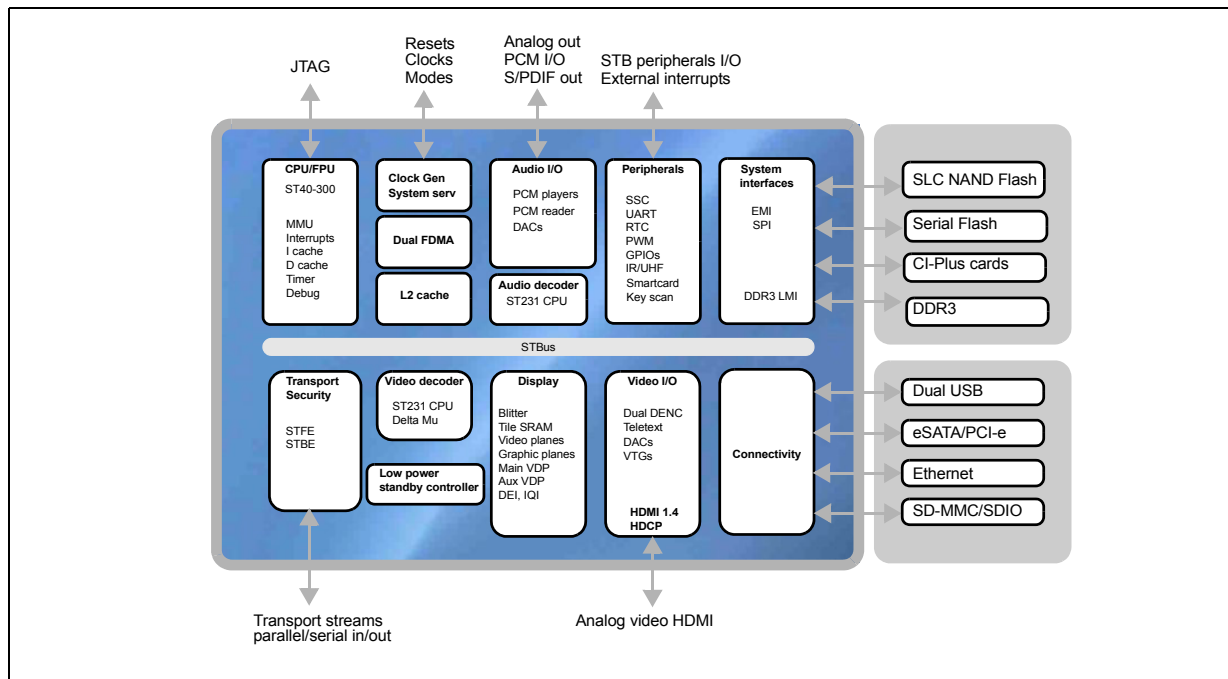
- ST40 applications CPU with 256 Kbyte L2 cache
- 16-bit LMI supporting DDR3 up to 667 MHz
- Decoding of H.264, MPEG2, VC-1 and AVS HD video streams
- 3DTV decoding and display compatible with HDMI 1.4b
- Extensive connectivity (two USB 2.0 ports; Ethernet MII/RMII/TMII port; SD/MMC card port; eSATA port; PCIe)
- Secure booting from SLC NAND Flash or Serial NOR Flash
- Low-power process and architecture
- Integrated low power standby controller
- High-quality video resizing and de-interlacing
- Integrated Ethernet PHY

- Targets two layer PCB designs for low-end zapper STB applications
- Package: PBGA 27 × 27 × 2.19

Description

The STiH206 uses the latest process technology to provide a cost-effective, feature rich, highly integrated SoC for set-top boxes (STBs). It is targeted at the advanced decoding STB market across all networks (cable/satellite/DTT/x-DSL/IP) worldwide, and is suitable both for operator markets (with advanced security) and retail markets.

The STiH206 provides a solution for operators and manufacturers to specify a range of cost-effective, high-performance STBs including basic zappers, interactive STBs, IP clients, and DVR STBs with content delivery possible using broadcast or broadband networks or both (Hybrid STBs).



1 Introduction

The STiH206 offers current users of ST's growing family of advanced decoding ICs enhancements in performance and features, enabling operators to offer consumers new multimedia-rich services and viewing experiences, including new 3DTV features. Faster DDR3 memory is also supported, and the applications CPU benefits from an L2 cache. The STiH206 keeps pace with the latest advanced security requirements of the main CA vendors, and an integrated standby controller enables the STiH206 to target stringent low power regulations.

Features	Benefits
ST40 applications CPU, with 32 Kbyte I and 32 Kbyte D L1 caches and 256 Kbyte L2 cache.	High performance processing for applications and middleware.
Integrated low power standby controller within its own power island.	Secure hibernation to, and fast resume from, very low power passive standby mode, targeting STB standby power < 0.5 W.
Latest generation of ST's Delta video decoder with an ST231-based multi-codec capable controller, coupled with a High Quality Video Display Pipeline (HQVDP).	Decoding of advanced high definition standards (MPEG2, H264, VC-1, AVS) plus the performance and flexibility for web-based content decoding such as Flash [®] , DivX [™] , MJPEG and Real [®] , without impacting applications CPU performance.
Dual USB 2.0 hosts, eSATA, Ethernet MAC with MII/RMII/TMII interfaces, PCI-e, SD-MMC/SDIO interface.	Extensive high speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, Ethernet, home network controllers (such as MoCA [®] , Wi-Fi), DOCSIS [®] modem and memory cards.
NOCS3.0, NSK2.0 and DVB-CSA3 ready.	Fully compliant with the latest advanced security requirements of CA vendors.

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
06-Jun-2013	1	Initial release.

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