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November 2013

FAN8060
1.2 MHz, 1 A Synchronous Step-Down DC/DC Regulator

Features

- Current Mode Control
- Over 96% Efficient
- Selectable Continuous Output Current: 500 mA/1 A
- 2.5 V to 5.5 V Input Voltage Range
- Output Voltage as Low as 1.2 V
- 1.2 MHz Operating Frequency
- Less than 1 µA Shutdown Current
- External Synchronization from 500 kHz to 2 MHz
- 100% Duty Cycle
- Synchronous Switching FET; no Schottky Diode Required
- Stable with Ceramic Capacitors
- Light Load Mode with Pulse Skipping
- External Compensation
- External Soft-Start
- Overload / Short-Circuit Protection
- Under-Voltage Lockout
- Thermal Shutdown
- 10-Lead 3x3 mm Green MLP Package

Applications

- PDAs
- GPS Devices
- MP3 Players
- Mini PCI
- Digital Cameras
- Peripheral Ports
- DSP Core
- USB Devices
- PCMCIA
- Cable Modem
- Data Cards

Description

The FAN8060 is a highly efficient, monolithic, current-mode, step-down synchronous regulator. It can provide 1 A continuous current from 2.5 V to 5.5 V input voltage. The output voltage can be adjusted from 1.2 V up to the input voltage with an external voltage divider.

External compensation and soft-start allow for design optimization and flexibility. High-frequency operation allows for all-ceramic solutions and small footprints. In addition, a user-selectable current limit provides protection against output overload and short circuit.

FAN8060 features pulse skipping to achieve higher efficiency during light load operation. 100% duty cycle capability enables power solutions to extend the drop out voltage.

Provision for external synchronization allows users to minimize input capacitors and manage EMI in solutions.

FAN8060 is available in a green, low profile, 10-Lead 3x3 mm MLP package.

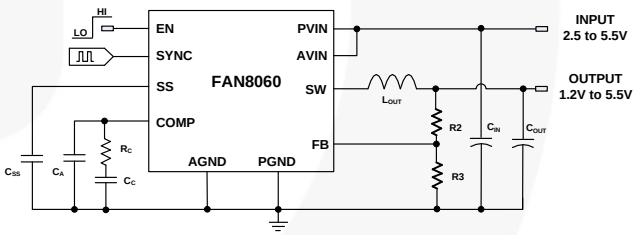


Figure 1. Typical Application Circuit

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN8060EMPX	-40 to +85°C	10-Pin, 3x3 mm Molded Leadless Package (MLP)	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Pin Configuration

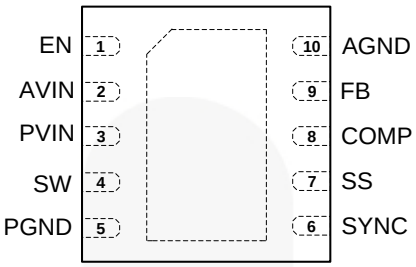


Figure 2. Pin Configuration (Top View)

Note:
1. Connect exposed PAD to AGND

Pin Definitions

Pin	Name	Function
1	EN	**Enable**. Enables operation when pulled to logic HIGH.
2	AVIN	**Analog Input Voltage**. All internal control circuits are connected to this supply.
3	PVIN	**Power Input Voltage**. Power stage supply voltage.
4	SW	**Switching Node**. The drains of both PMOS and NMOS.
5	PGND	**Power Ground**. Power return and source of the power NMOS
6	SYNC	**Synchronization**. Use this pin to synchronize the part to an external clock. This pin also controls current limit threshold. Tie to ground for 1.0 A or tie to V_{IN} for 0.5 A continuous load current. When an external clock is applied, the default current setting is 1 A. This pin has a pull-down resistor of 450 KΩ.
7	SS	**Soft-Start.** A capacitor connected between this pin and AGND can set soft-start time.
8	COMP	**Compensation**. Error amplifier output. Connect the external compensation network between this pin and AGND.
9	FB	**Output Voltage Feedback**. Connect through a resistor divider to set the output voltage.
10	AGND	**Analog Ground**. Ground return for all internal control circuits.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to the network ground terminal. Stress beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Symbols	Parameter		Min.	Max.	Unit
V_{PVIN}	PVIN (AGND=PGND)		-0.3	6.0	V
V_{AVIN}	AVIN (AGND=PGND)		-0.3	6.0	V
V_{SW}	Switch Voltage, SW to GND		-0.3	V_{IN} + 0.3 or 6.0	V
	All other pins except COMP		-0.3	6.0	V
T_{STG}	Storage Temperature		-65	+150	°C
T_J	Junction Temperature		-40	+125	°C
ESD	Electrostatic Discharge Protection	Human Body Model, JESD22-A114	2.0		kV
		Charged Device Model, JESD22-C101	2.5		

Note:
2. COMP pin has an internal clamp to 1.5 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

Thermal Information

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{STG}	Storage Temperature	-65		+150	°C
T_L	Lead Soldering Temperature, 30 Seconds			+300	°C
θ_{JA}	Thermal Resistance: Junction-to-Ambient		49		°C/W
θ_{Jc}	Thermal Resistance: Junction-to-Case[3]		8		°C/W
P_D	Total Power Dissipation in the package, T_A=25°C[3]			1.3	W

Note:
3. Typical thermal resistance when mounted on a four-layer PCB. Actual results are dependent upon mounting method and surface related to the design.

Electrical Characteristics

V_{IN}=5.0 V, V_{OUT}=2.5 V, C_{OUT}=10 µF, C_{IN}=10 µF, over operating range, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Basic Operation						
V_{IN}	V_{IN} Operating Voltage	AVIN=PVIN	2.5		5.5	V
I_Q	Quiescent Current	V_{EN}=5 V, V_{SS}=0 V	250	371	500	µA
I_{SD}	Shutdown Current	V_{EN}=0 V		0.34	0.60	µA
V_{UVLO}	V_{IN} Under-Voltage Lockout	Rising V_{IN}	2.10	2.19	2.25	V
$V_{UVLOHYS}$	V_{IN} Under-Voltage Lockout Hysteresis			70		mV
V_{ENH}	Enable High Input Voltage			1.70	2.00	V
V_{ENL}	Enable Low Input Voltage		0.80	1.22		V
R_{ONPMOS}	PMOS On Resistance(4)	V_{IN}=5 V		200		mΩ
		V_{IN}=3.3 V		300		
R_{ONNMOS}	NMOS On Resistance(4)	V_{IN}=5 V		200		mΩ
		V_{IN}=3.3 V		300		
I_{LIM}	P-Channel Current Limit V_{FB}=0.7 V, V_{IN}=5 V, 100% Duty Cycle	V_{SYNC}=0 V		1.2		A
		V_{SYNC}=V_{IN}		0.6		
f_{OSC}	Oscillator Frequency	T_A=25°C	1.105	1.210	1.350	MHz
V_{SYNC}	SYNC Threshold	Rising Edge		V_{IN}/2		V
f_{SYNC}	Synchronization Frequency	V_{SYNC}=Square Wave	500		2000	KHz
t_{SYNC}	Minimum SYNC Pulse Width	V_{SYNC} On Time		100		ns
I_{AMP}	Error Amplifier	Sink/Source Current	30	45	60	µA
		G_{EA}(4)	700	1000	1400	µA/V
		A_{VEA}(4)		550		V/V
G_{CS}	Current Sense Gain(4)			3		A/V
V_{REF}	Reference Voltage for Temperature Co-efficient, *see Figure 12*	Measured at FB Pin T_A=25°C	1.181	1.205	1.229	V
I_{FB}	FB Bias Current	T_A=25°C	-0.10	-0.06	0	µA
I_{SS}	Soft-Start Current		-5.5	-4.5	-3.5	µA
Protections						
T_{OTP}	Over-Temperature Threshold(4)			+165		°C
T_{HYS}	Over-Temperature Hysteresis			+20		°C

Note:

4. Guaranteed by design and characterization; not production tested.

Functional Block Diagram

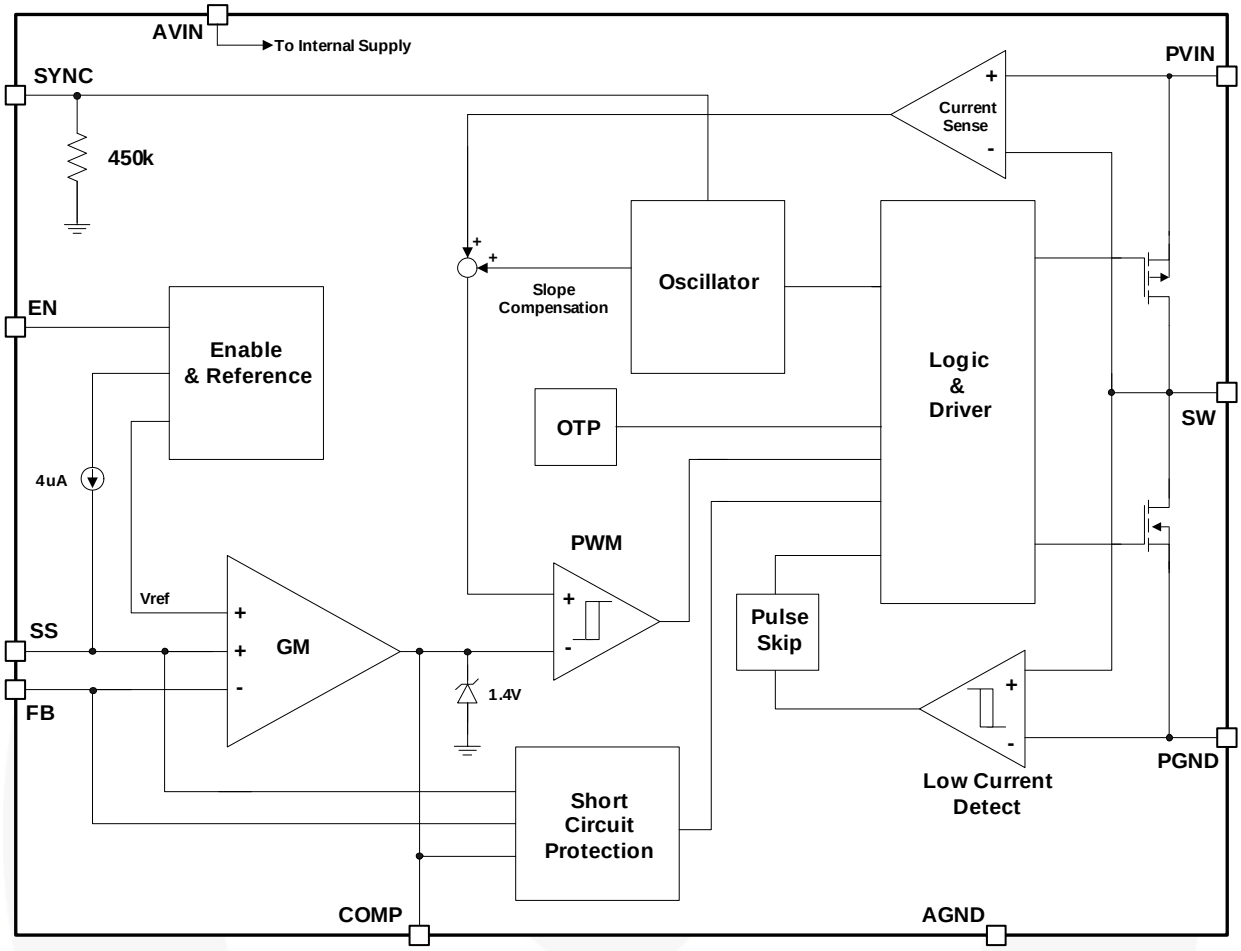


Figure 3. Functional Block Diagram

Operation Description

The FAN8060 is a step-down converter operating in current-mode PWM architecture with a typical switching frequency of 1.2 MHz. At the beginning of each clock cycle, the P-channel transistor is turned on. The current in the inductor ramps up and is sensed via an internal circuit. The P-channel switch is turned off when the sensed current causes the PWM comparator to trip, which is when the output voltage is in regulation or when the inductor current reaches the current limit (set internally to 1.2 A, typically). After a minimum dead time to prevent shoot-through current, the N-channel transistor is turned on and the current ramps down. As the clock cycle is completed, the N-channel switch is turned off and the next clock cycle starts.

Light Load Operation

As the output load reduces, the current in the inductor during off time is sensed across the low side MOSFET. When the current reverses direction, the low-side MOSFET is turned off and the high-side MOSFET is not turned on until the output is out of regulation.

100% Duty Cycle Operation

As the input voltage approaches the output voltage, the controller starts to increase the duty cycle to maintain output regulation until duty cycle reaches 85%. The controller then transitions to a 100% duty cycle mode over several cycles to support the load. When the dropout condition is met, the converter turns the P-channel high side continuously on. In this mode, the output voltage is equal to the input voltage, minus the voltage drop across the P-channel MOSFET.

Soft Start

When the input voltage on AVIN exceeds the UVLO threshold and EN is high, the circuit releases SS and enables the PWM regulator. A capacitor connected to the SS pin and AGND is charged by a 4 µA internal current source, causing the voltage on the capacitor to rise. When this voltage reaches 1.2 V, the output is in regulation. The SS voltage continues to rise to AVIN. The time for the output to reach regulation is given by the following equation:

$$t(ms) = \frac{C_{SS}(nF)}{(4\mu A / 1.2V)} \quad (1)$$

Output overload and short-circuit protection is active during soft-start. When the part is disabled, SS pin is pulled low internally.

Overload & Short-Circuit Protection

FAN8060 employs cycle-by-cycle current limiting, which limits current by reducing duty cycle during overload. As the load increases beyond the limit, the output voltage starts to reduce, thereby reducing the FB voltage. When the FB node is half the reference voltage and the COMP node has reached maximum value, short-circuit protection is detected. At that time, both the SS pin and the COMP pin are pulled to ground until the inductor current crosses zero. At that point, both SS and COMP are released for the current to ramp up again. This continues until the short-circuit condition is released.

Typical Performance Characteristics

V_{IN}=5 V, V_{OUT}=2.4 V, L=3.3 µH, C_{IN}=10 µF, C_{OUT}=10 µF, f_S=1.2 MHz, T_A=25°C, unless otherwise noted.

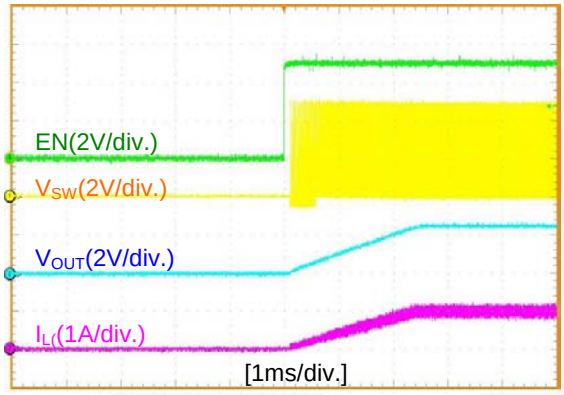


Figure 4. EN Startup with 1 A Load

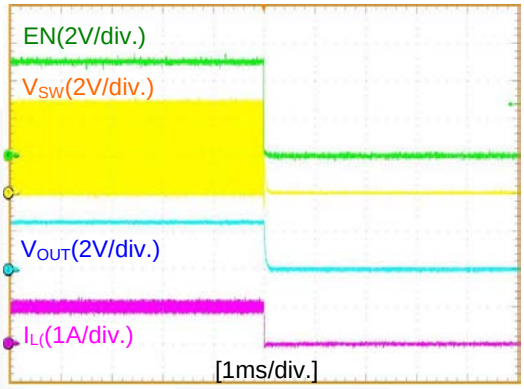


Figure 5. EN Turn off with 1 A Load

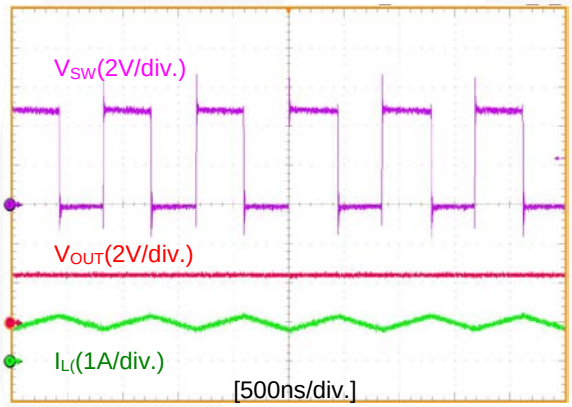


Figure 6. PWM Operation with 1 A Load

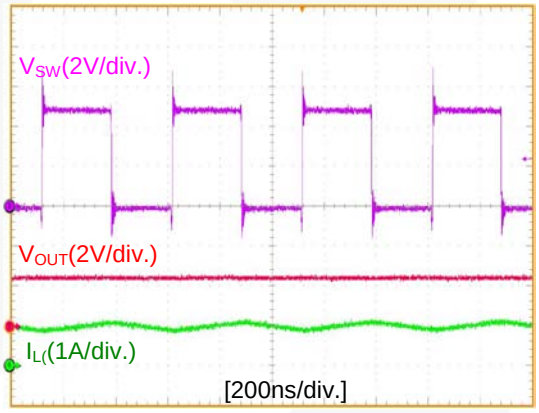


Figure 7. 2 MHz Sync Operation with 1 A Load

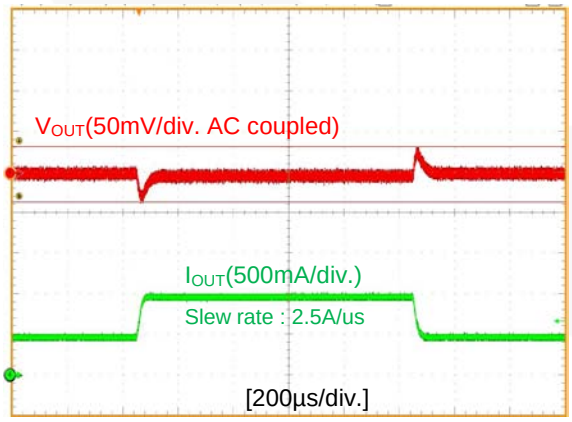


Figure 8. Load Transient Response(Step-up/down)

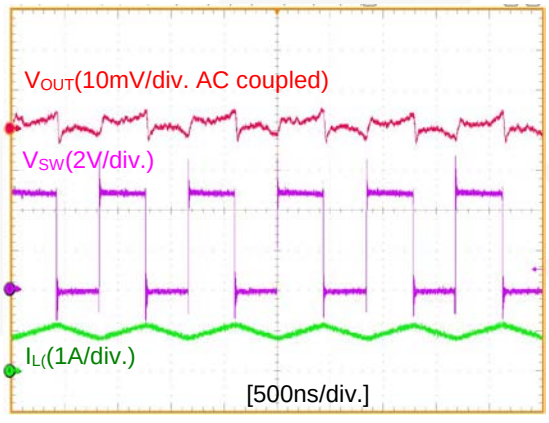


Figure 9. Output Voltage Ripple with 1 A Load

Typical Performance Characteristics (Continued)

V_{IN}=5 V, V_{OUT}=2.4 V, L=3.3 µH, C_{IN}=10 µF, C_{OUT}=10 µF, f_S=1.2 MHz, T_A=25°C, unless otherwise noted.

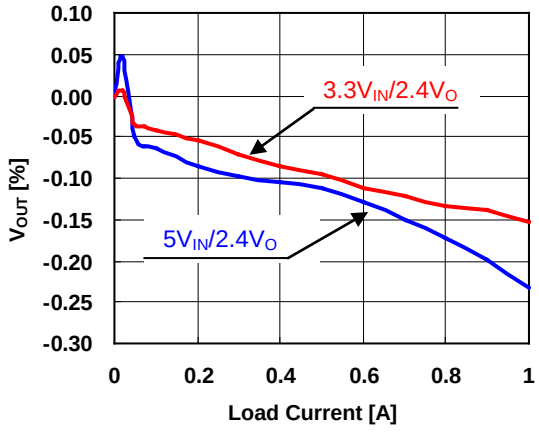


Figure 10. Normalized V_{OUT} vs. Load Current

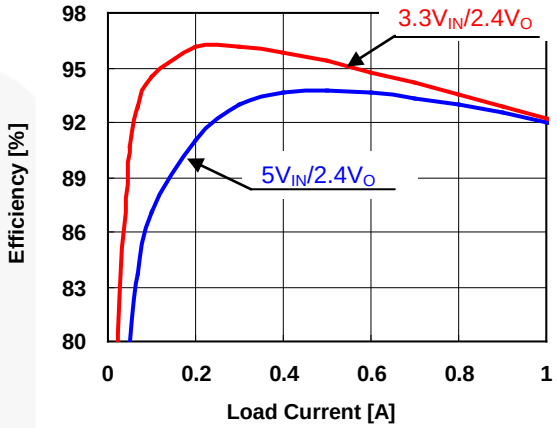


Figure 11. Efficiency vs. Load Current

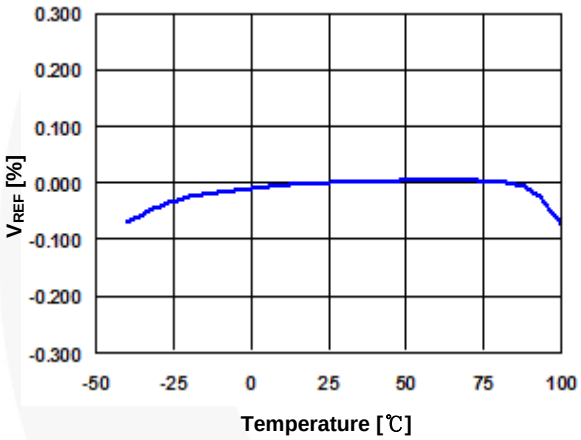


Figure 12. Normalized V_{REF} vs. Temperature

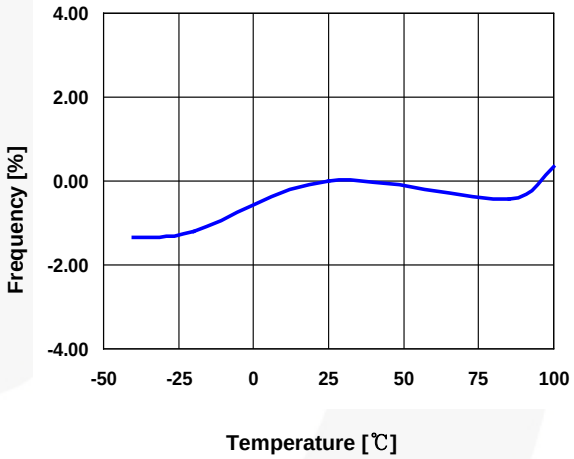


Figure 13. Normalized Oscillation Frequency vs. Temperature

Applications Information

Refer to Figure 1 for reference designators.

Output Voltage Setting

The output voltage of the FAN8060 can be set from 1.2 V to V_{IN} by an external resistor divider, given by the following equation:

$$V_{OUT} = 1.2(1+\frac{R_2}{R_3}) \quad (2)$$

where, V_{OUT} equals the output voltage.

Inductor Selection

Typically, the inductor value is chosen based on ripple current (ΔI_L), which is chosen between 10% and 35% of the maximum DC load. Regulator designs that require fast transient response use a higher ripple-current setting, while regulator designs that require higher efficiency keep ripple current on the low side and operate at a lower switching frequency.

For a given output voltage ripple requirement, L can be calculated by the following equation:

$$L \geq \frac{V_{OUT} \cdot (1-D)}{\Delta I_L \cdot f_S} \quad (3)$$

where;

D = Duty ratio (V_O/V_{IN});

f_S = Switching frequency; and

ΔI_L = Inductor ripple value, typically set to 10% - 35% of the maximum steady-state load current.

The inductor should have a low DCR to minimize the conduction losses and maximize efficiency. Some recommended inductors are suggested in Table 1:

Table 1. Recommended Inductors (3.3 µH)

Size[mm2]	DCR	Part Number	Vendor
7x7x3	23 mΩ	SLF7032T-3R3	TDK
5x5x2	60 mΩ	LTF5022T-3R3	TDK
4x4x2	78 mΩ	VLCF4020T-3R3	TDK
2.6x2.8x1.2	130 mΩ	VLF3012AT-3R3	TDK

Output Capacitor Selection

The output capacitor is selected based on the needs of the final application and its output ripple requirements. A larger output capacitor value reduces the output ripple voltage. The formula of output ripple ΔV_{OUT} is:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \cdot C_{OUT} \cdot f_S} \right) \quad (4)$$

where C_{OUT} is the output capacitor.

ESR is the equivalent series resistance of the output capacitor.

Input Capacitor Selection

The input capacitor reduces the RMS current drawn from the input and switching noise from the device. The combined RMS current rating for the input capacitor should be greater than the value calculated by the following equation:

$$I_{RMS} = I_{OUTMAX} \cdot (\sqrt{D - D^2}) \quad (5)$$

where:

I_{RMS} = RMS current of the input capacitor; and

I_{OUTMAX} = Maximum output current.

Small, high value, inexpensive, lower-ESR ceramic capacitors are recommended; 10 µF ceramic capacitors with X7R or X5R should be adequate for 1 A applications.

Loop Compensation

The loop is compensated using a feedback network connected between COMP and AGND. Figure 14 shows a Type-2 compensation network used to stabilize the FAN8060.

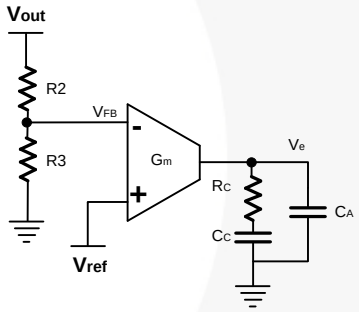


Figure 14. Compensation Network

The goal of the compensation design is to shape the frequency response of the converter to achieve high DC gain and fast transient, while maintaining loop stability. FAN8060 employs peak-current-mode control for easy use and fast transient response. Current mode control helps simplify the loop to a one-pole and one zero system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_L \cdot G_{CS} \cdot A_{VEA} \cdot \frac{V_{FB}}{V_{OUT}} \quad (6)$$

where:

A_{VDC} = DC gain of the feedback loop;

R_L = Load resistor value (V_{OUT}/I_{OUT});

G_{CS} = Current sense gain (3 A/V);

A_{VEA} = Error amplifier voltage gain (550 V/V); and

V_{FB} = Feedback threshold voltage (1.2 V).

The system pole is calculated by the equation:

$$f_{P1} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_L} \quad (7)$$

The system zero is due to the output capacitor and its ESR. System zero is calculated by the equation:

$$f_{z1} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR} \quad (8)$$

The output characteristics of the error (Gm) amplifier are controlled by a series capacitor and resistor network connected at the COMP pin to GND.

The pole is calculated by the following equation:

$$f_{p2} = \frac{G_{EA}}{2\pi \cdot C_C \cdot A_{VEA}} \quad (9)$$

where:

G_{EA} = Error Amplifier Transconductance (1000 µA/V); and

C_C = compensation capacitor.

Zero is due to the compensation capacitor (C_C) and resistor (R_C) calculated by the following equation:

$$f_{z2} = \frac{1}{2\pi \cdot C_C \cdot R_C} \quad (10)$$

where R_C is compensation resistor.

The system crossover frequency (f_C), where the control loop has unity gain, is recommended to be set at 1/10th of switching frequency. Generally, higher f_C means faster response to load transients, but can result in instability if not properly compensated.

The first step in compensation design is choosing the compensation resistor (R_C) to set the crossover frequency by the following equation:

$$R_C = \frac{2\pi \cdot C_{OUT} \cdot f_C \cdot V_{OUT}}{G_{CS} \cdot G_{EA} \cdot V_{FB}} \quad (11)$$

where V_{FB} is reference voltage.

The next step is choosing the compensation capacitor (C_C) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z2}, to below one fourth of the crossover frequency provides sufficient phase margin. Determine the (C_C) value by the following equation:

$$C_C = \frac{2}{\pi \cdot R_C \cdot f_C} \quad (12)$$

Then determine if the second compensation capacitor (C_A) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency.

$$\frac{1}{2\pi \cdot C_{OUT} \cdot ESR} < \frac{f_S}{2} \quad (13)$$

If required, add the second compensation capacitor (C_A) to set the pole f_{P3} at the location of the ESR zero. Determine (C_A) value by the equation:

$$C_A = \frac{C_{OUT} \cdot ESR}{R_C} \quad (14)$$

Design Example

Table 2 provides component values for delivering various output voltages with loads up to 1 A with V_{IN} at 5 V (±10% tolerance).

Table 2. Recommended Feedback and Compensation Values (V_{IN}=5 V)

V_O	C_4	L_1	R_2	R_3	R_1	C_5	C_2
1.2 V	10 µF	3.3 µH	Short	Open	4.7 kΩ	1.5 nF	150 pF
1.5 V			2.55 kΩ	10.2 kΩ			
1.8 V			5.9 kΩ	11.8 kΩ			
2.5 V			16.2 kΩ	15 kΩ			
3.3 V			18.7 kΩ	10.7 kΩ			

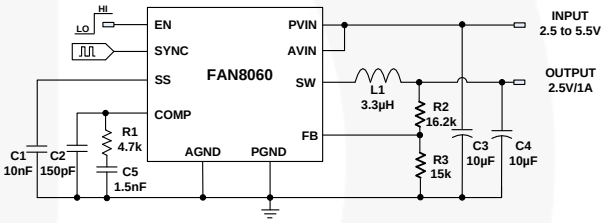


Figure 15. Recommended Schematic (5 V_{IN} to 2.5 V_O)

PCB Layout Recommendations

The switching power supply PCB layout needs careful attention and is critical to achieving low losses and clean and stable operation. Although each design is different, below are some general recommendations for a good PCB layout.

- Keep the high-current traces and load connectors as short and wide as possible. These traces consist of VIN, GND, VOUT, and SW.
- Place the input capacitor, the inductor, and the output capacitor as close as possible to the IC terminals.
- Keep the loop area between SW node, inductor, and output capacitors as small as possible; minimizing ground loops to reduce EMI issues.
- Route high-dV/dt signals, such as SW node, away from the error amplifier input/output pins.
- Keep components connected to the FB and COMP pins close to the pins.

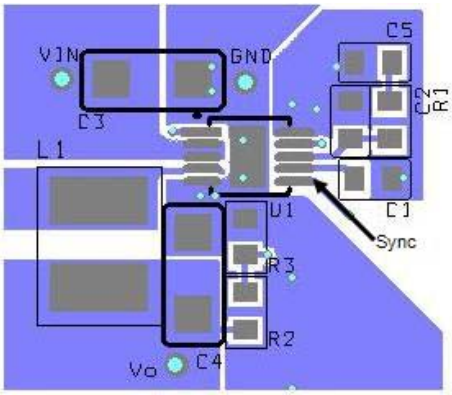
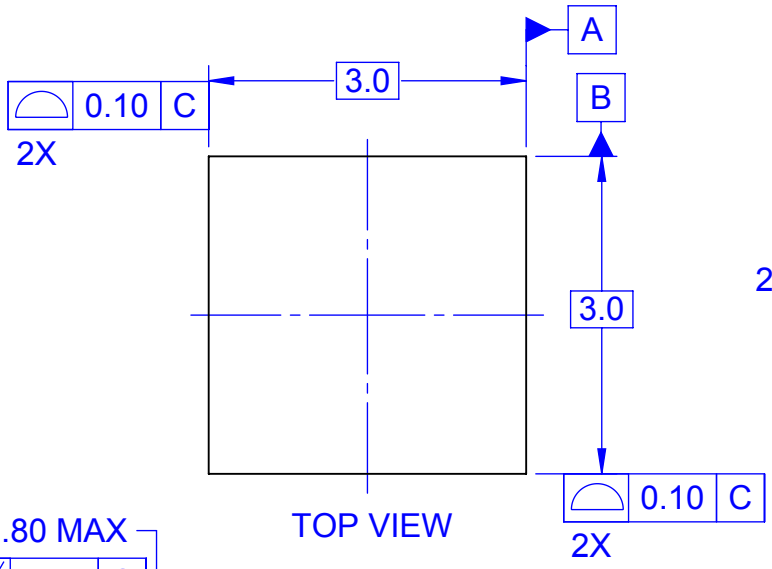
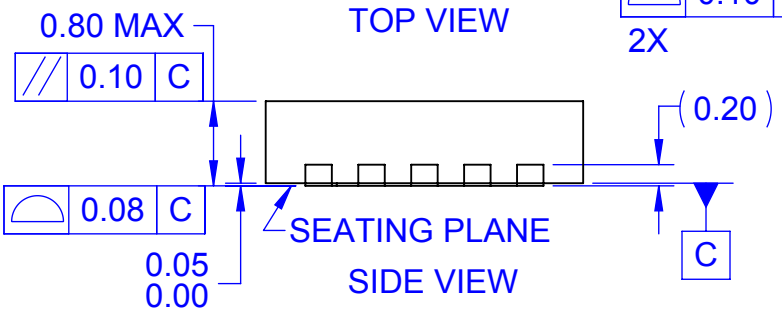
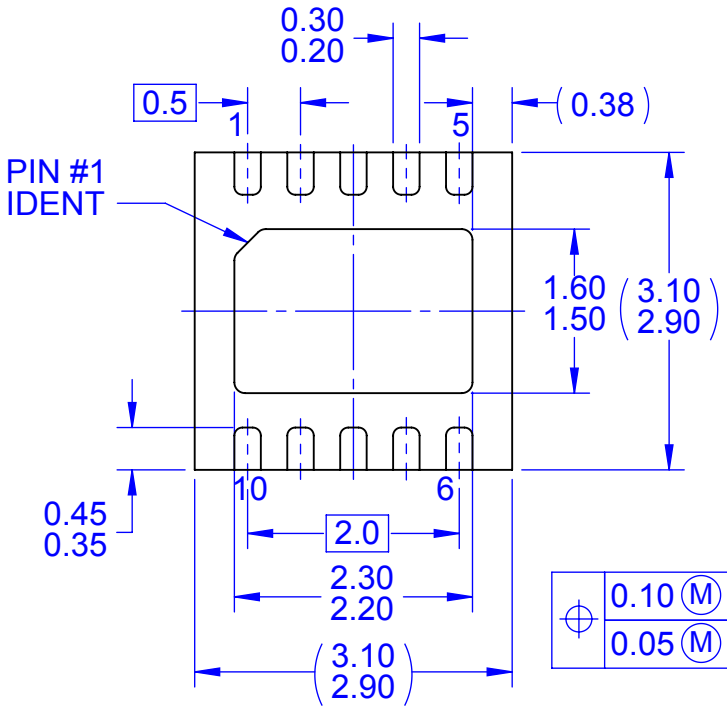
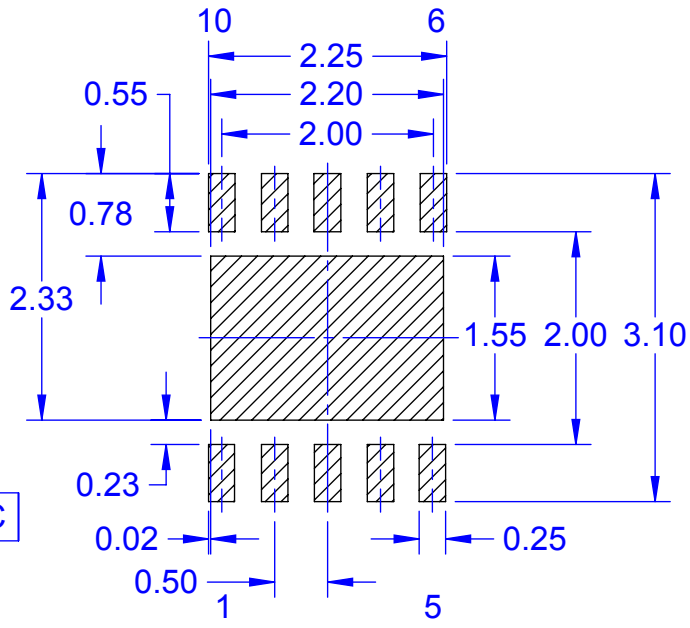


Figure 16. Recommended PCB Layout









NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION WEED-5
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009
D. LAND PATTERN DIMENSIONS ARE NOMINAL REFERENCE VALUES ONLY
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