ESDAVLC6V1-1BM2
ESDAVLC6V1-1BT2

Single line low capacitance Transil™ for ESD protection

Features

- single line bidirectional protection
- breakdown voltage V_{BR} = 6.1 V min.
- very low capacitance (6 pF typ. @ 3 V)
- lead-free package

Benefits

- very low capacitance for optimized data integrity
- very low reverse current < 0.1 µA
- low PCB space consumption 0.6 mm^2 max
- high reliability offered by monolithic integration

Complies with the following standards:

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7: class 3 B:
  - Human body model

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- computers
- printers
- communication systems
- cellular phone handsets and accessories
- video equipment

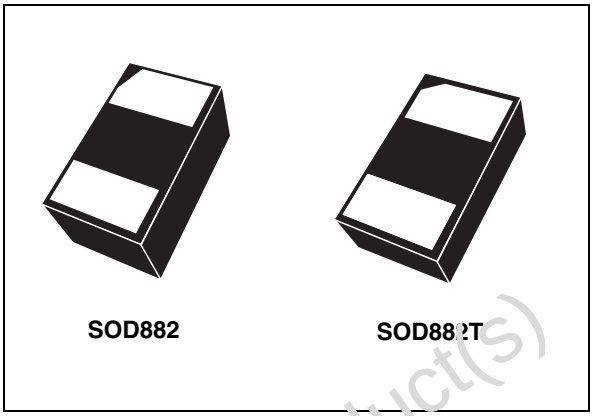
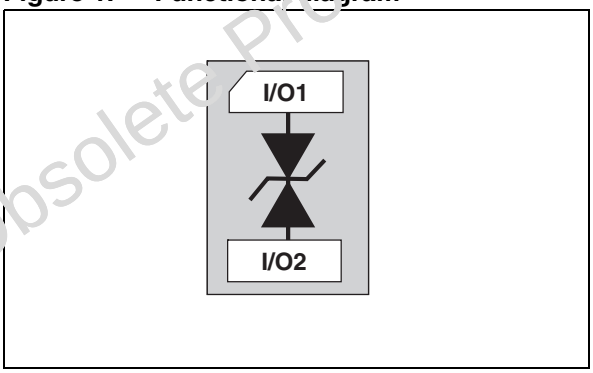


Figure 1. Functional diagram



Description

The ESDAVLC6V1-1BM2 and ESDAVLC6V1-1BT2 are monolithic application specific devices dedicated to ESD protection of high speed serial interfaces such as USB 2.0, display and camera interfaces.

The devices are ideal for applications where both printed circuit board space and power absorption capability are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25° C)

Symbol	Parameter		Value	Unit
V_{PP}(1)	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge MIL STD 883G - Method 3015-7: class 3B	15 15 25	kV
P_{PP}(1)	Peak pulse power dissipation (8/20 µs)	T_j initial = T_{amb}	30	W
I_{PP}	Peak pulse current (8/20 µs)		2.5	A
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		- 55 to + 150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C
T_{OP}	Operating temperature range		- 40 to + 125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

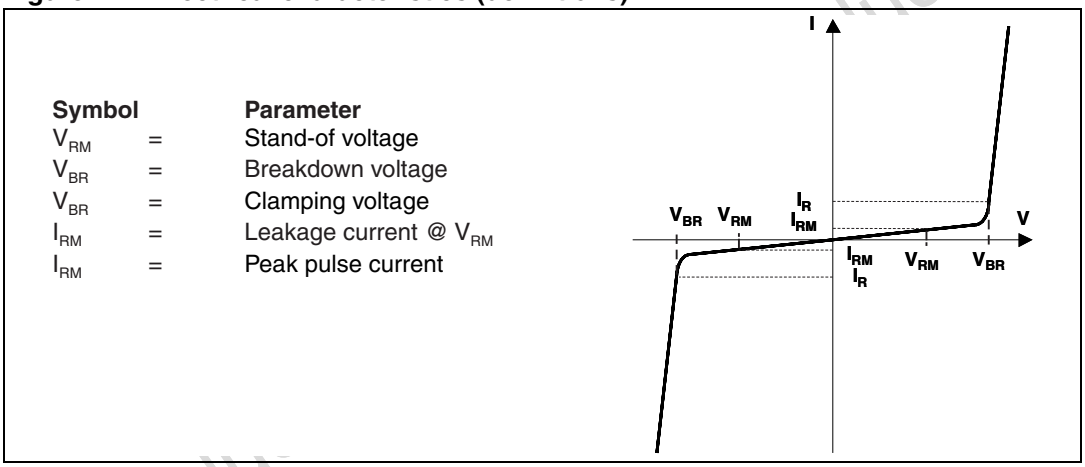


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6.1			V
I_{RM}	V_{RM} = 3 V			100	nA
R_d			1.6		Ω
αT				2.5	10^{-4}/°C
C	F = 1 MHz, V_R = 0 V		7	8	pF
	F = 1 MHz, V_R = 3 V		6	7	

Figure 3. Relative variation of peak pulse power versus initial junction temperature

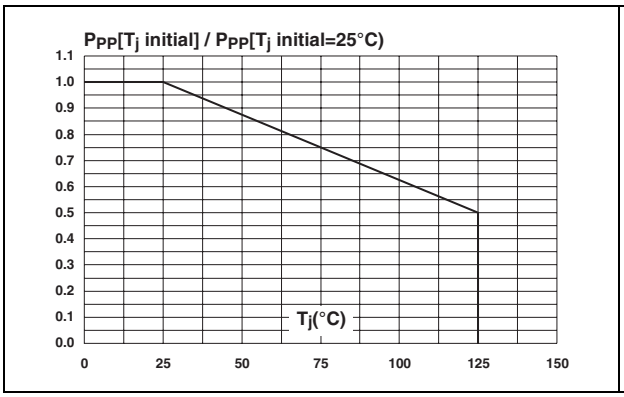


Figure 4. Peak pulse power versus exponential pulse duration

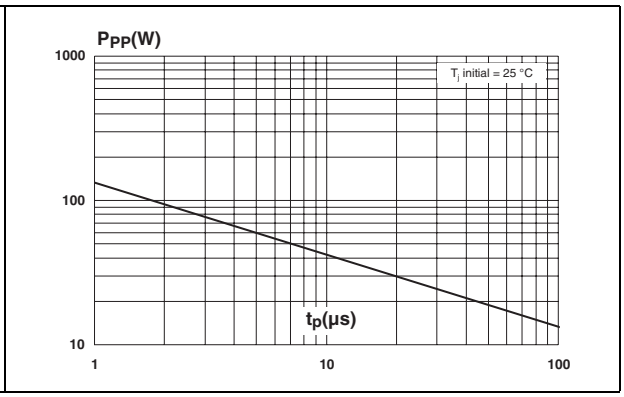


Figure 5. Clamping voltage versus peak pulse current (typical values)

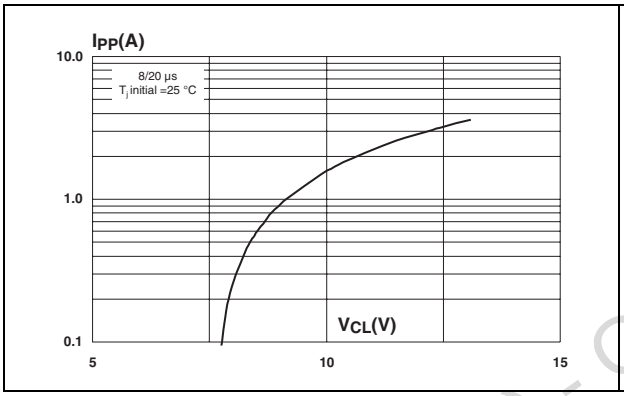


Figure 6. Junction capacitance versus reverse voltage applied (typical values)

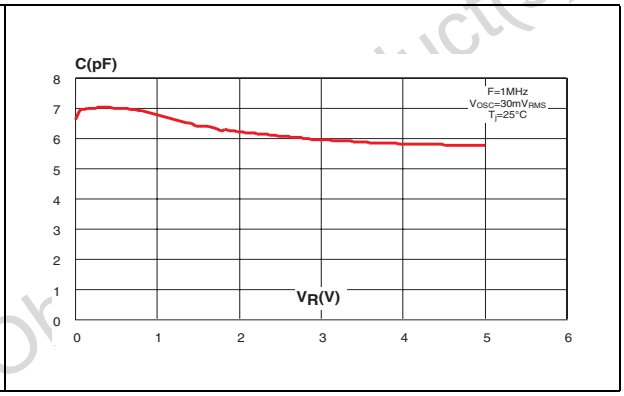


Figure 7. Relative variation of leakage current versus junction temperature (typical values)

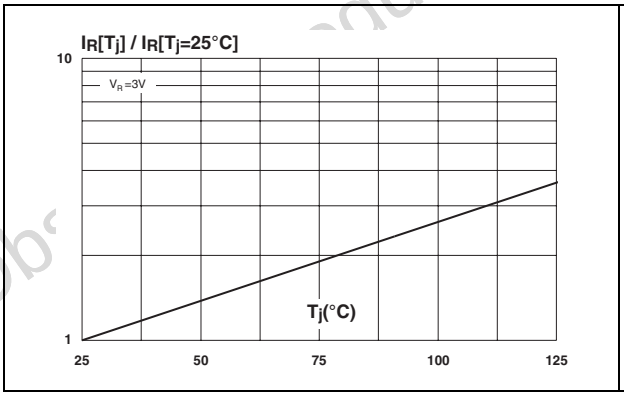


Figure 8. S21 attenuation measurement result

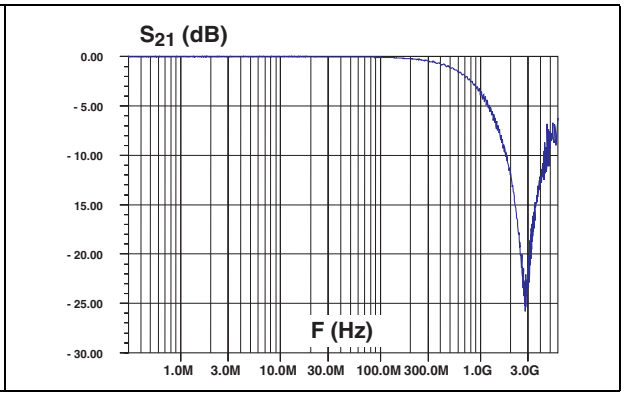


Figure 9. ESD response to IEC 61000-4-2 (+2 kV air discharge)

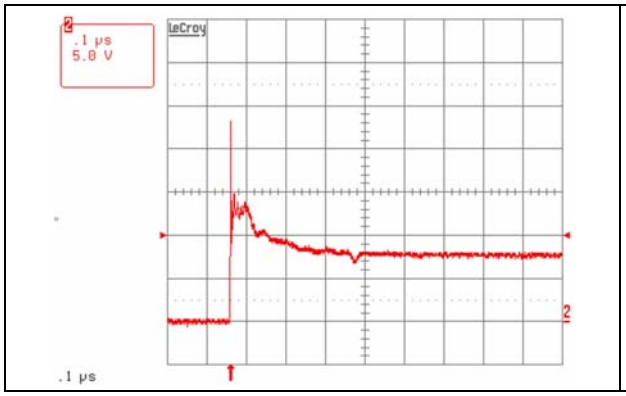


Figure 10. ESD response to IEC 61000-4-2 (-2 kV air discharge)

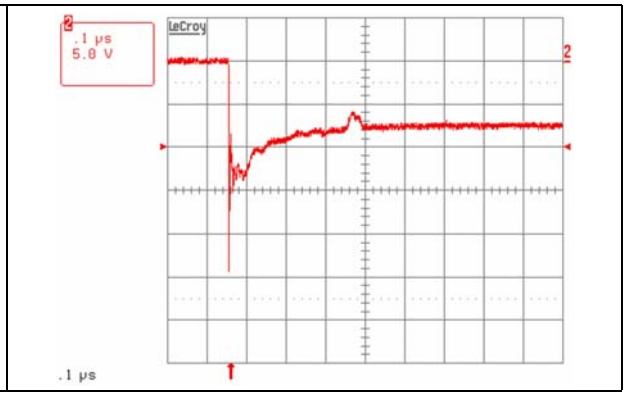


Figure 11. ESD response to IEC 61000-4-2 (+8 kV air discharge)

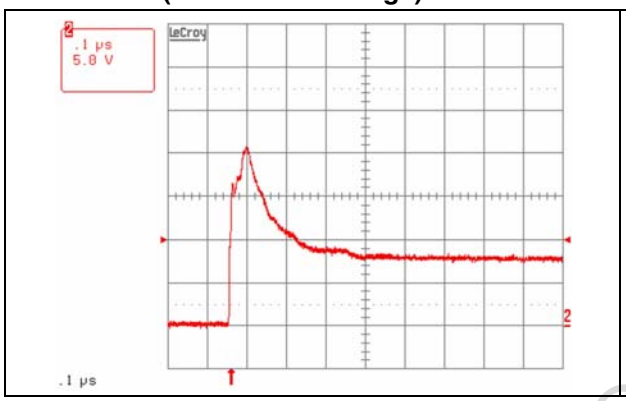


Figure 12. ESD response to IEC 61000-4-2 (-8 kV air discharge)

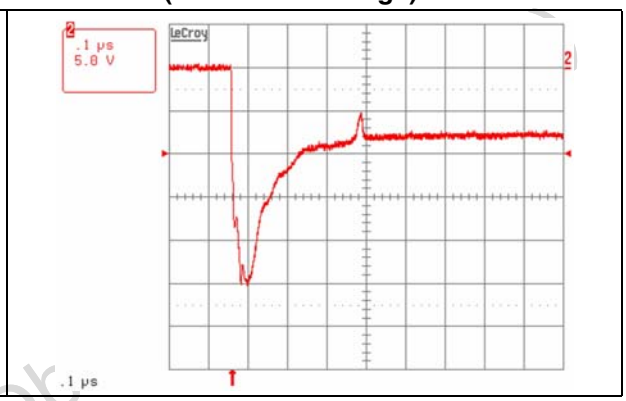


Figure 13. ESD response to IEC 61000-4-2 (+15 kV air discharge)

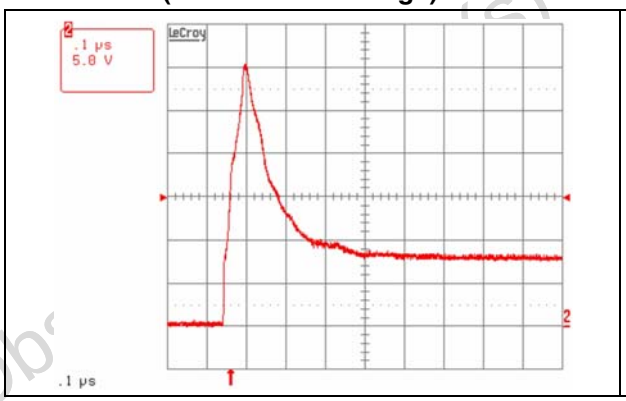


Figure 14. ESD response to IEC 61000-4-2 (-15 kV air discharge)

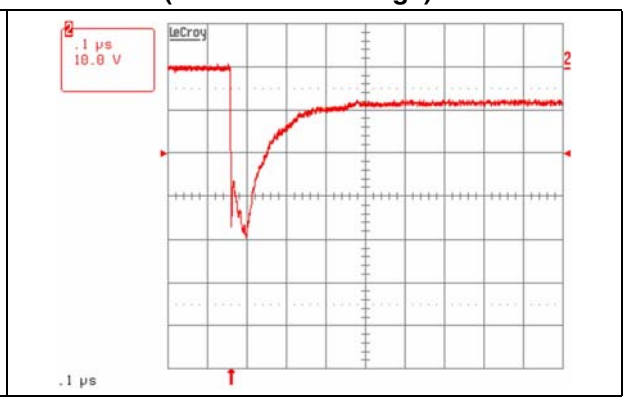


Figure 15. ESD response to IEC 61000-4-2 (+2 kV contact discharge)

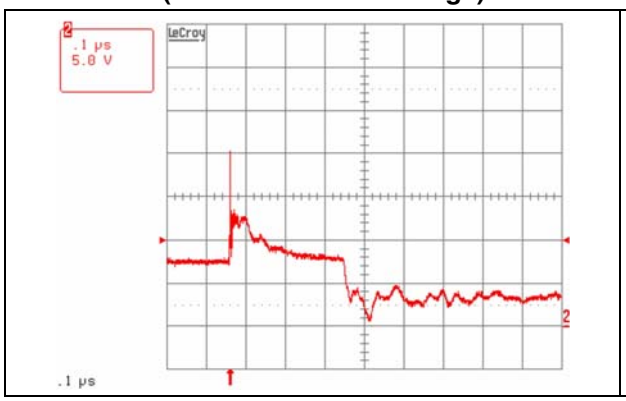


Figure 16. ESD response to IEC 61000-4-2 (-2 kV contact discharge)

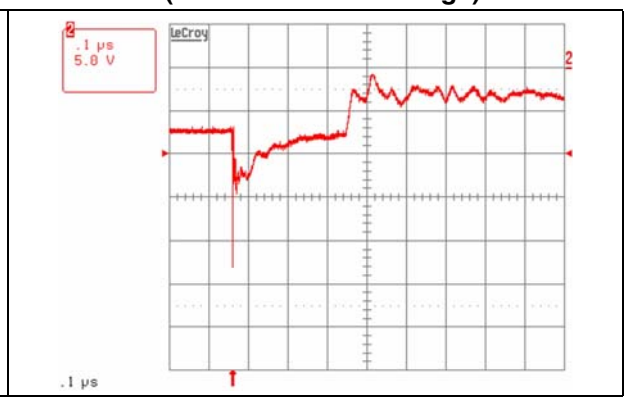


Figure 17. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

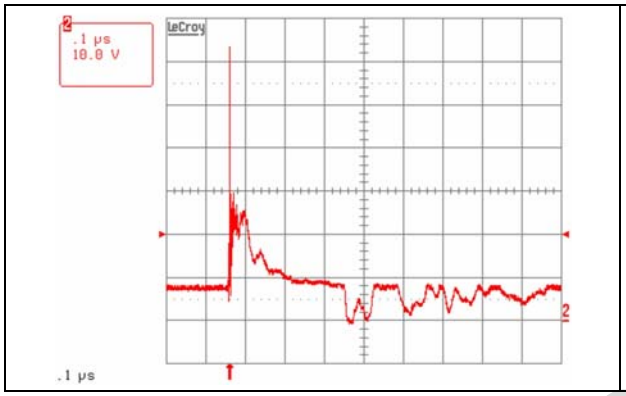


Figure 18. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

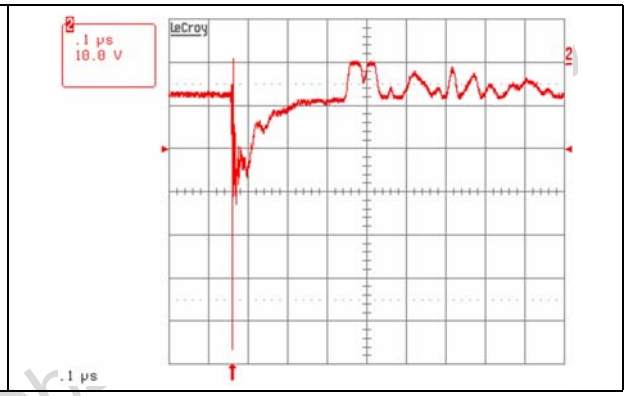


Figure 19. ESD response to IEC 61000-4-2 (+15 kV contact discharge)

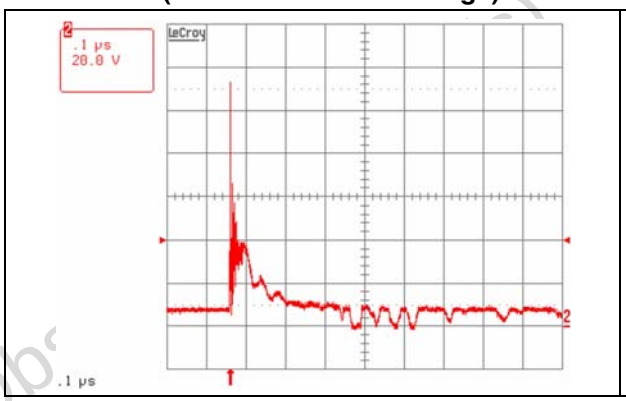
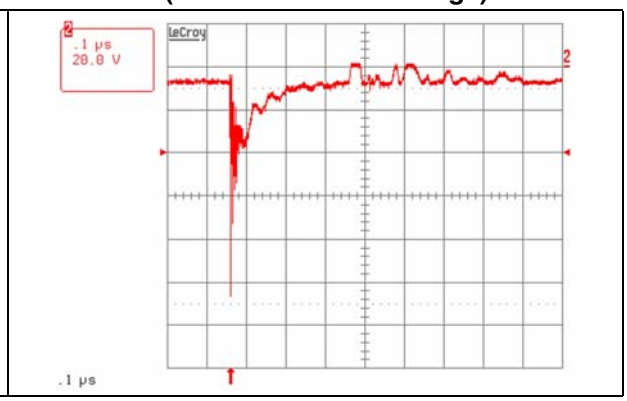
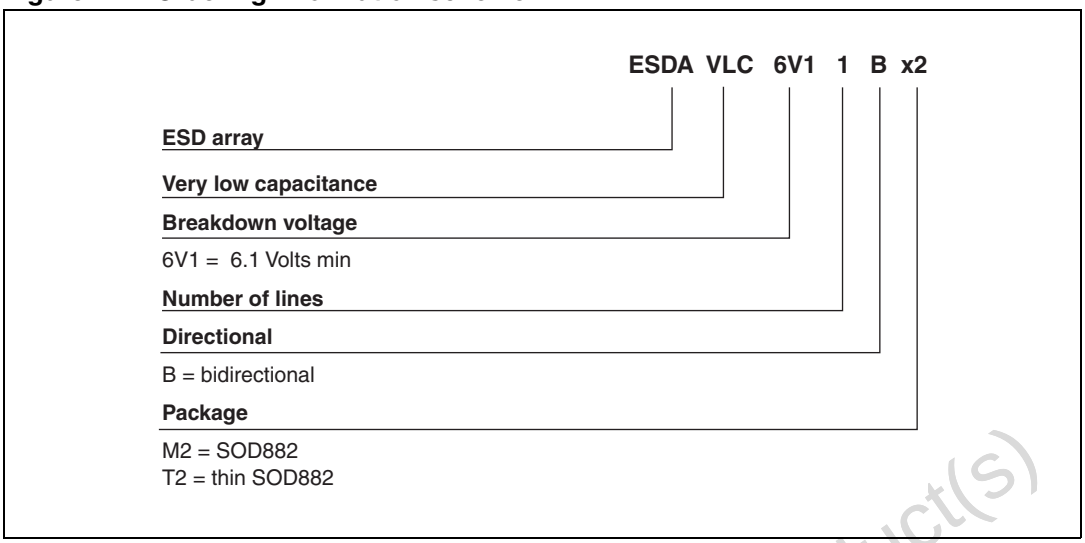


Figure 20. ESD response to IEC 61000-4-2 (-15kV contact discharge)



2 Ordering information

Figure 21. Ordering information scheme

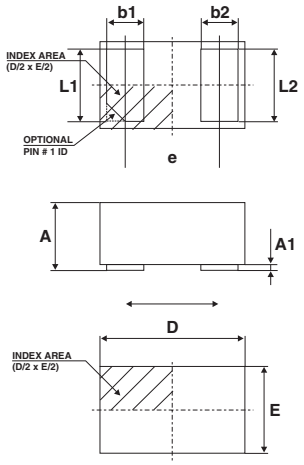


3 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. SOD882 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.016	0.019	0.020
A1	0.00		0.05	0.000		0.002
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	0.20	0.25	0.30	0.008	0.010	0.012
D		1.00			0.039	
E		0.60			0.024	
e		0.65			0.026	
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.45	0.50	0.55	0.018	0.020	0.022

Figure 22. Footprint

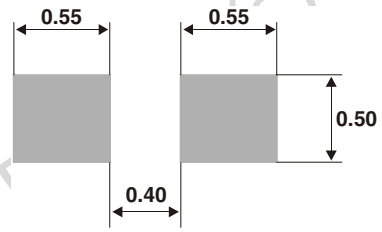
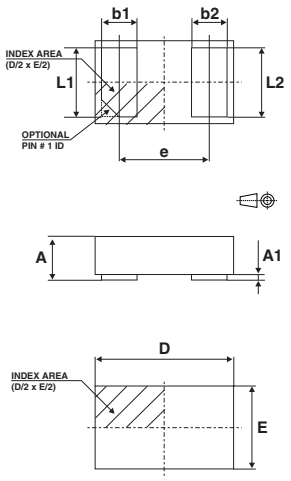


Figure 23. Marking

Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Table 4. Thin SOD882 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.30		0.40	0.012		0.016
A1	0.00		0.05	0.000		0.002
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	0.20	0.25	0.30	0.008	0.010	0.012
D		1.00			0.039	
E		0.60			0.024	
e		0.65			0.026	
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.45	0.50	0.55	0.018	0.020	0.022

Figure 24. Footprint

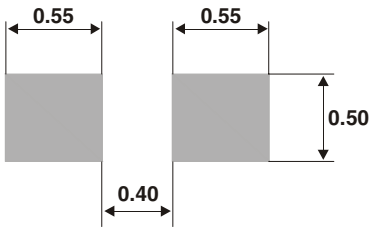
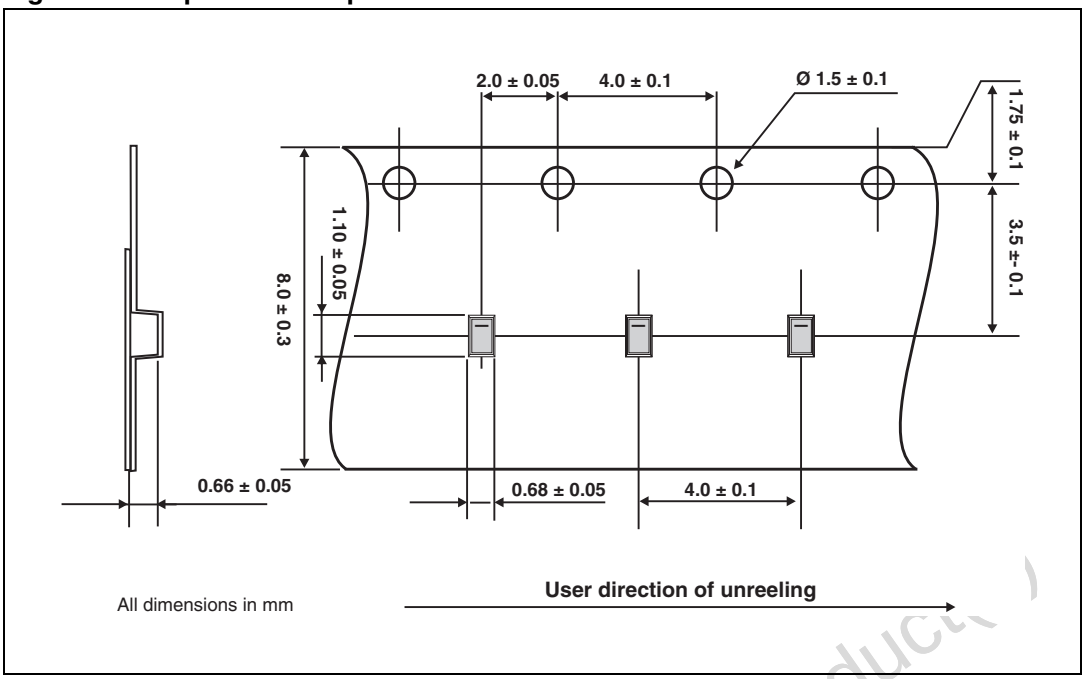


Figure 25. Marking

Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 26. Tape and reel specifications

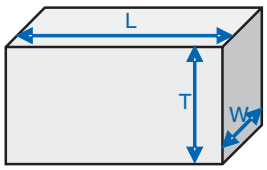


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 27. Stencil opening dimensions



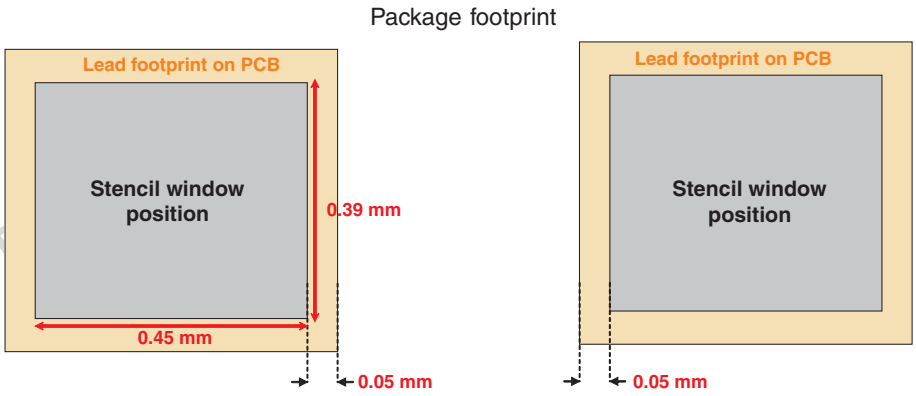
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio - between 60% and 65%.

Figure 28. Recommended stencil windows position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

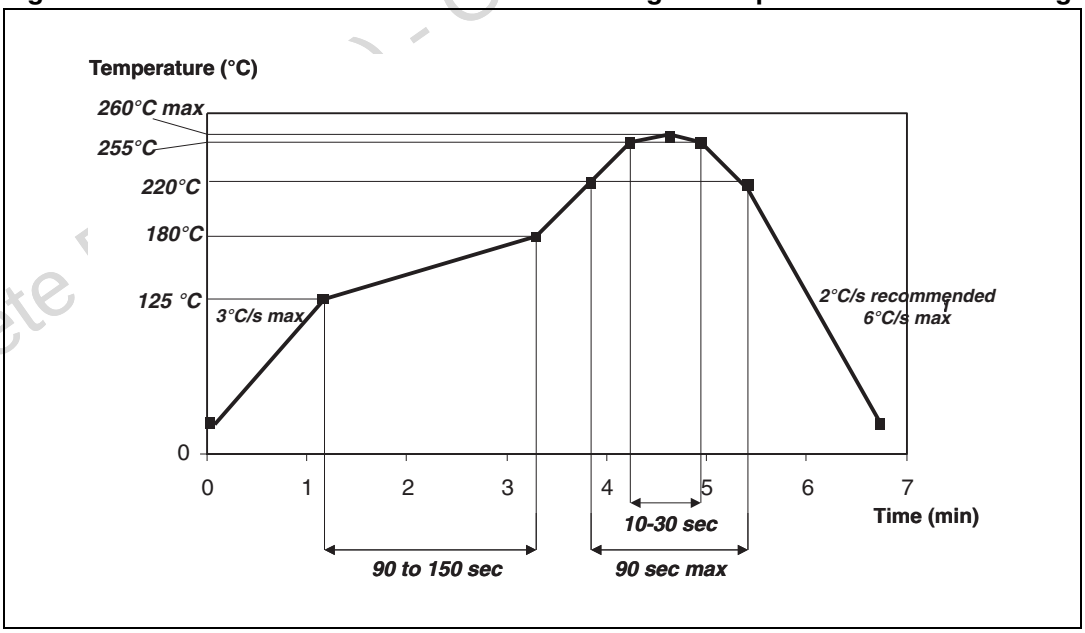
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 29. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDAVLC6V1-1BM2	C(1)	SOD882	0.92 mg	12000	Tape and reel
ESDAVLC6V1-1BT2	T(1)	Thin SOD882	0.76 mg	12000	Tape and reel

1. The marking can be rotated by 90° to diferentiate assembly location

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
16-Apr-2008	1	Initial release.
02-Dec-2010	2	Updated base quantity in *Table 5.*