ESDAXLC4-1BF3

Single line extra low capacitance TVS

Features

- Stand-off voltage 3 V
- Ultra low capacitance 0.3 pF on a wide frequency spectrum, 200 to 3000 MHz
- Bidirectional device
- Low clamping factor V_{CL}/V_{BR}
- Fast response time
- Very thin package: 0.36 mm max
- Low leakage current

Complies with the following standards

- IEC 61000-4-2 level 4

Applications

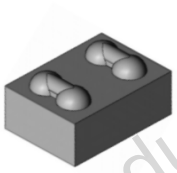
Where transient over voltage protection and electrical overstress protection in sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment Portable equipment

Description

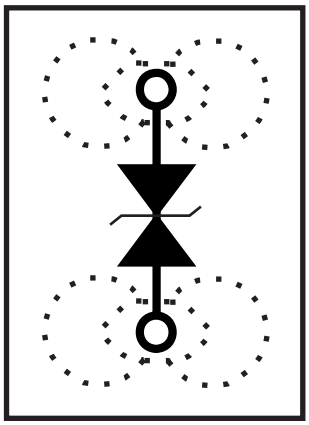
The ESDAXLC4-1BF3 is a single line Transil™ diode designed specifically for the protection of integrated circuits into portable equipment and miniaturized electronics devices subject to ESD and EOS transient over voltages.

Packaged in WLCSP, it minimizes PCB consumption.



Flip Chip
(2 bumps)

Figure 1. Schematic diagram (top view)



TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage: IEC61000-4-2 contact discharge		8	kV
P_{PP}	Peak pulse power dissipation (8/20 µs) (1)	$T_{j\ initial} = T_{amb}$	55	W
I_{PP}	Repetitive peak pulse current (8/20 µs)	$T_{j\ initial} = T_{amb}$	3	A
T_j	Junction temperature		- 55 to +125	°C
T_{stg}	Storage temperature range		- 65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 2. Electrical characteristics (definitions)

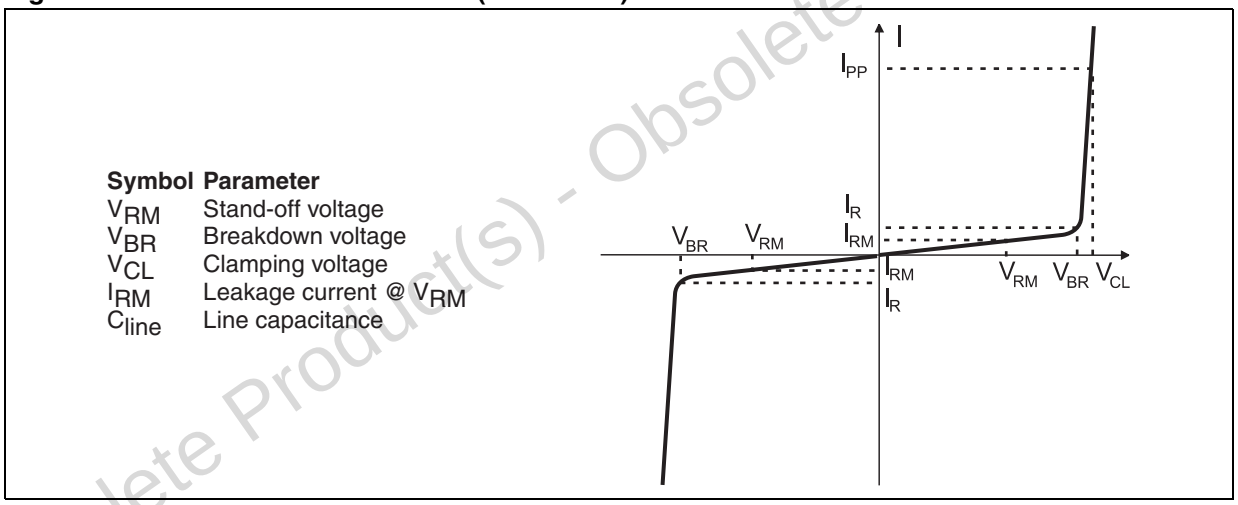


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	4	5.5	-	V
I_{RM}	V_{RM} = 3 V	-	-	50	nA
V_{CL}	I_{PP} (8/20 µs) = 1 A	-	-	10	V
C_{line}	F = [200 MHz -3000] MHz, V_R = 0 V DC, V_{osc} = 30 m V_{RMS}	-	0.3	0.4	pF

Figure 3. Junction capacitance versus reverse applied voltage (typical values)

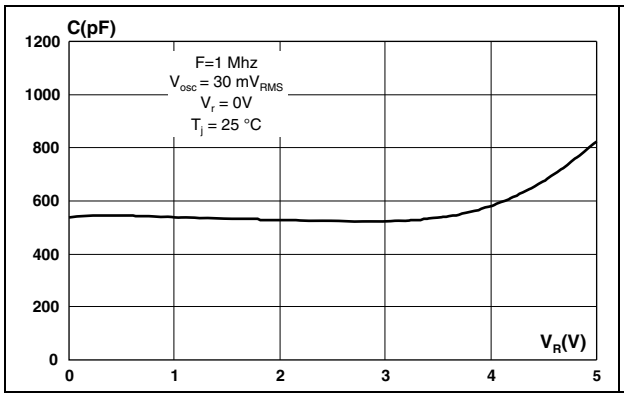


Figure 4. Junction capacitance versus frequencies (typical values)

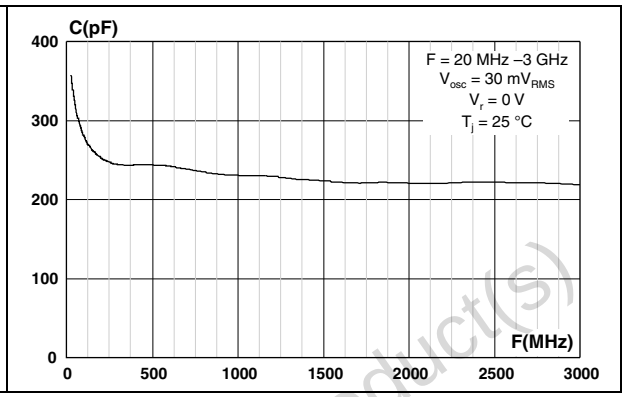


Figure 5. S_{21} attenuation measurement result

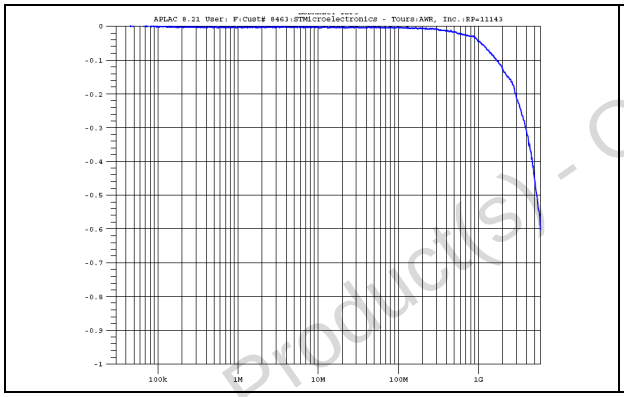


Figure 6. Variation of leakage current versus junction temperature (typical values)

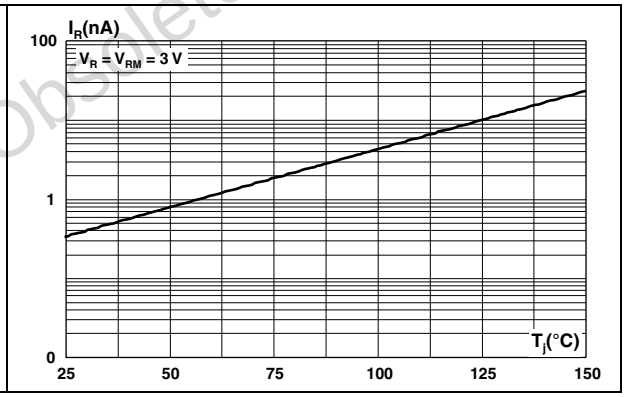


Figure 7. ESD response to IEC61000-4-2 (+8 kV contact discharge)

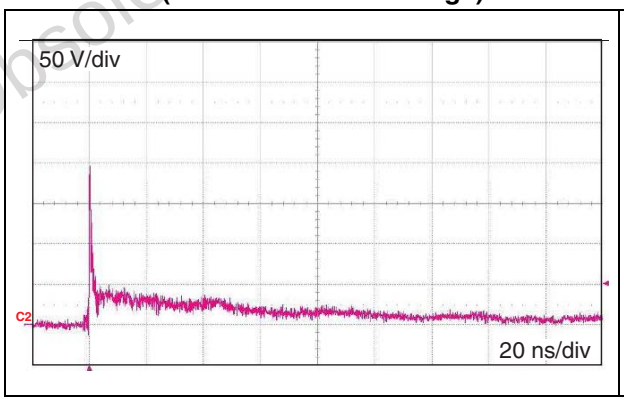
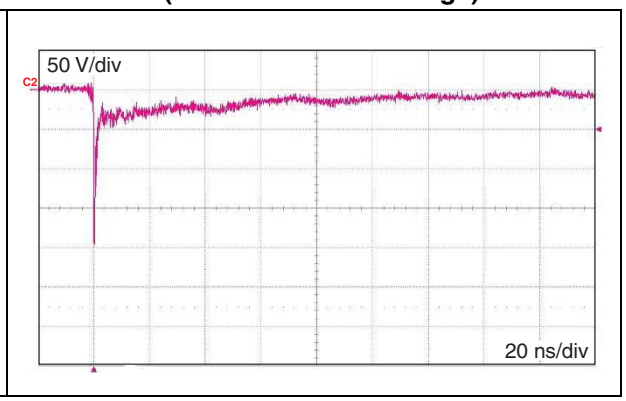
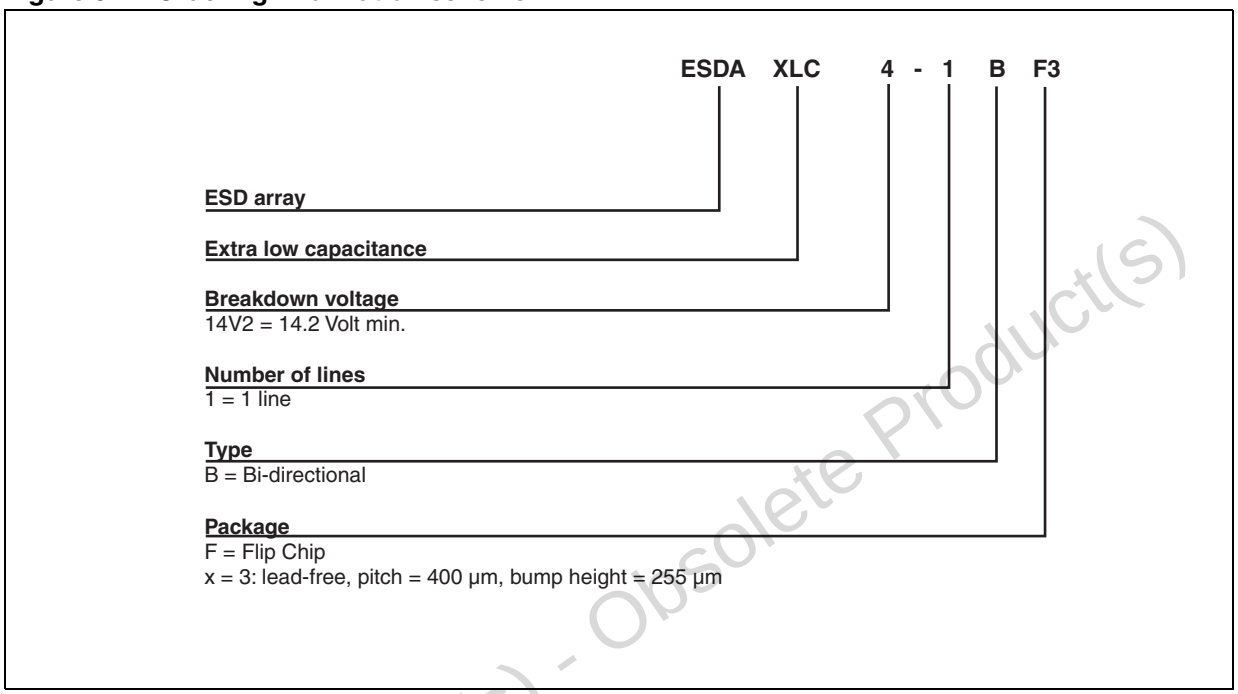


Figure 8. ESD response to IEC61000-4-2 (-8 kV contact discharge)



2 Ordering information scheme

Figure 9. Ordering information scheme



3 Package information

- Epoxy meets UL94,V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 10. Package dimensions

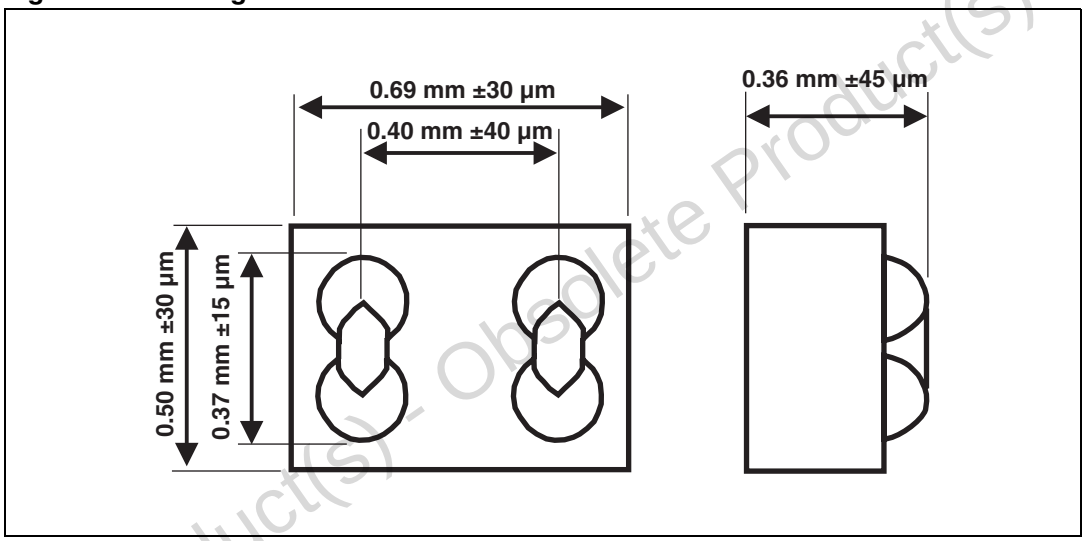


Figure 11. Marking

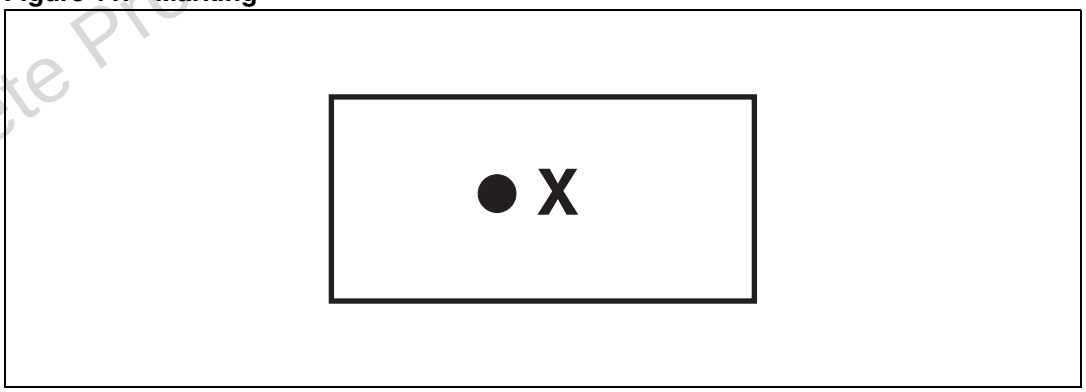
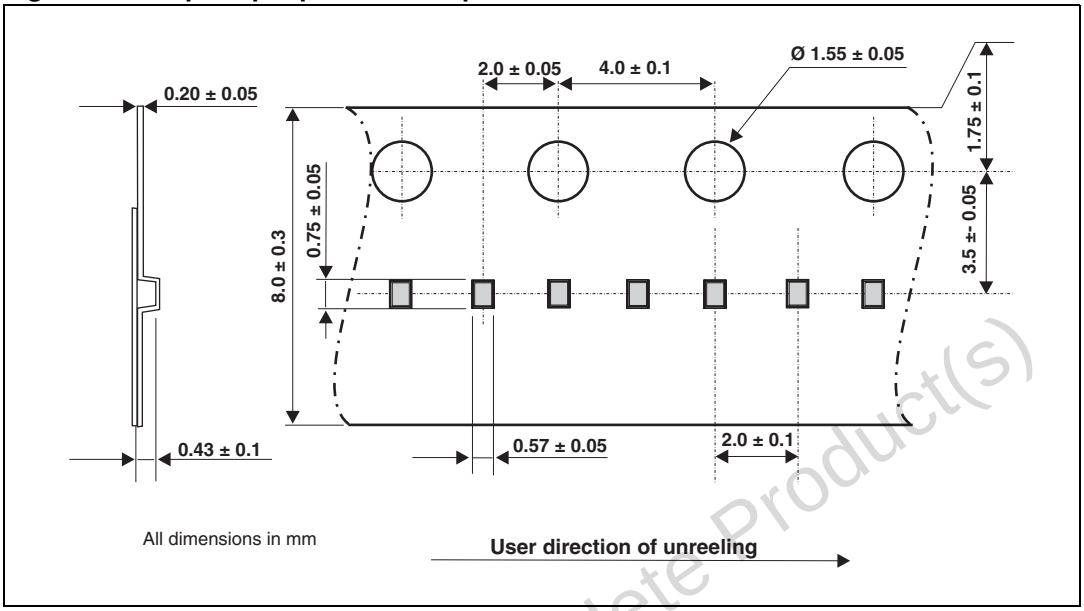


Figure 12. Flip Chip tape and reel specification



4 PCB recommendations

4.1 Design

For optimum electrical performance and highly reliable solder joints, STMicroelectronics recommends the PCB design recommendations listed in *Table 3*.

Table 3. PCB design recommendations for solder bar pitch 400 µm

For NSMD PCB non solder mask defined	Oblong pad: 370 x 180 µm – Micro via SSBU allowed – Micro via SBU to be avoided – Micro via SBU filled (under qualification)
	Track: – Only one track per pad – Maximum track width = 100 µm Track layout must be symmetrical to the die axis (to homogenize stress and welding attraction during reflow assembly)
For SMD PCB solder mask defined	Oblong pad: – Micro via SSBU allowed – Micro via SBU to be avoided – Micro via SBU filled (under qualification)
PCB Pad Finishing	Cu – Ni (2-6 µm) - Au (0.2 µm max)

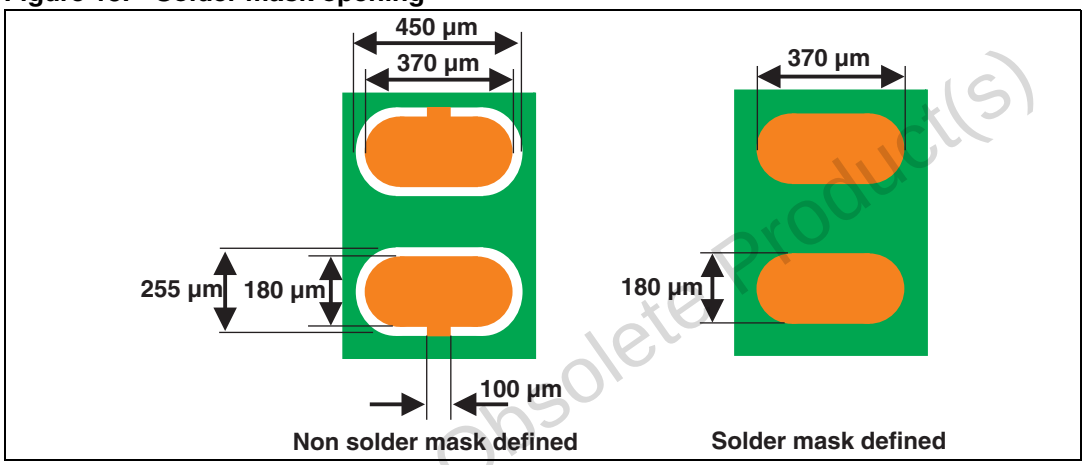
Note: A gold layer finishing on the PCB pad that is too thick (0.2 µm maximum) is not recommended (low joint reliability).

To optimize the natural self centering effect of CSP on the PCB, PCB pad positioning and size have to be properly designed (see *Figure 13*)

Micro vias

An alternative to routing on the top surface is to route out on buried layers. To achieve this, the pads are connected to the lower layers using micro vias. Only SSBU via technology is approved.

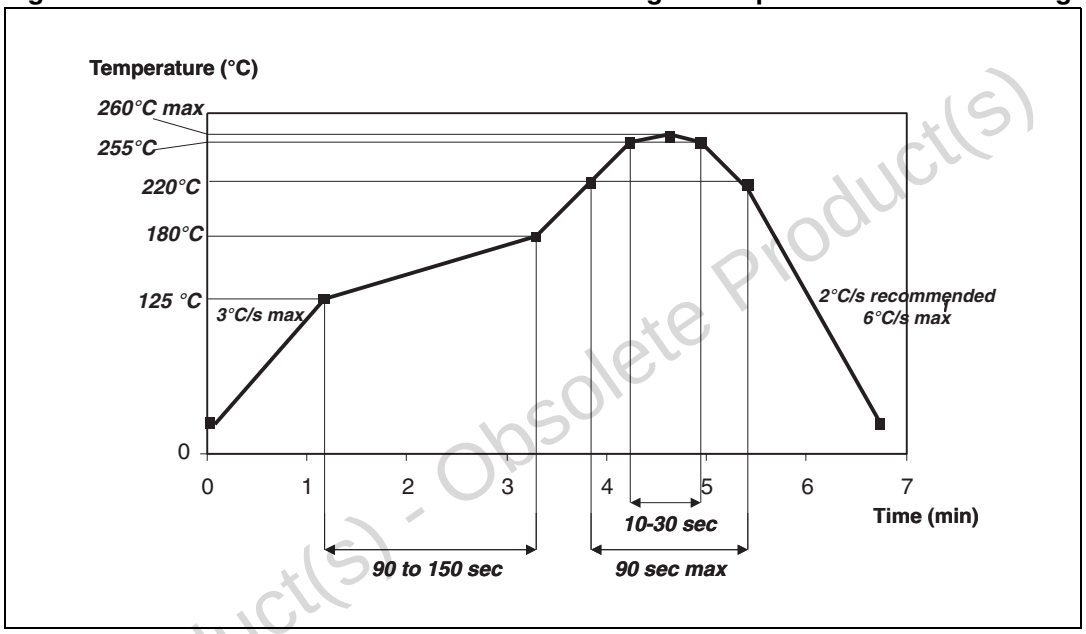
Figure 13. Solder mask opening



4.2 Assembly

For chip scale package mounting on the PCB, STMicroelectronics recommends the use of a solder stencil aperture of 330 x 330 µm² maximum and a typical stencil thickness of 75 or 80 µm. Chip scale packages are fully compatible with the use of near eutectic 95.5 Sn, 4 Ag, 0.5 Cu solder paste with no-clean flux. ST's recommendations for chip scale package board mounting are illustrated on the soldering reflow profile shown in *Figure 14*.

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Dwell time in the soldering zone (with temperature higher than 220 °C) has to be kept as short as possible to prevent component and substrate damages. Peak temperature must not exceed 260 °C. Controlled atmosphere (N2 or N2H2) is recommended during the whole reflow, especially above 150 °C.

Chip scale packages are able to withstand three times the previous recommended reflow profile in order to be compatible with a double reflow when SMDs are mounted on both sides of the PCB and one additional repair.

A maximum of three soldering reflows are allowed for these lead-free packages (with repair step included).

The use of a no-clean flux is highly recommended to avoid any cleaning operation. To prevent any bump cracks, ultrasonic cleaning methods are not recommended.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDAXLC4-1BF3	L	Flip Chip	0.37 mg	15 000	Tape and reel 7”

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
03-Mar-2011	1	Initial release.
12-May-2011	2	Updated features, *Table 1*, *Figure 9* and *Figure 11.*

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