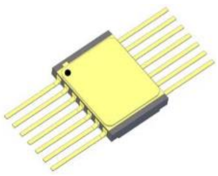
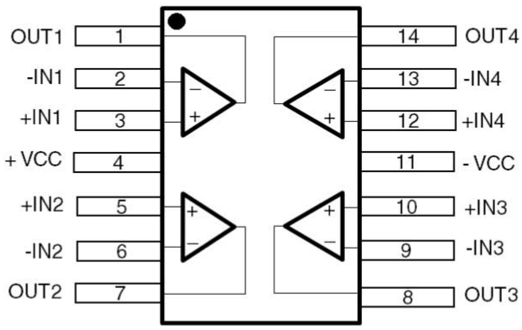
RHF484

Rad-hard precision quad operational amplifier

Datasheet - production data

Ceramic Flat-14W





The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package

Features

- Bandwidth: 8 MHz gain bandwidth product
- Rail-to-rail input/output
- Low input offset voltage: 60 µV typ
- Supply current: 2.2 mA typ per amplifier
- Operating from 4 to 14 V
- Input bias current: 6 nA typ
- ELDRS free up to 100 krad
- SEL immune at LET = 120 MEV.cm^2/mg at 125 °C
- SET characterized
- High radiation immunity: 300 krad TID at high-dose rate

Applications

- Space probes and satellites
- Harsh environments

Description

The RHF484 is a rail-to-rail, precision, bipolar, quad, operational amplifier featuring a low input offset voltage and a wide supply voltage. Designed to increase tolerance to radiation, the RHF484 is housed in a hermetic 14-pin flat package, making it an ideal product for space applications and harsh environments.

Table 1: Device summary

Parameter	RHF484K1	RHF484K-01V
SMD (1)	—	5962F08222
Quality level	Engineering model	QML-V flight
Package Mass	Flat-14W 0.7 g	
EPPL (2)	—	Yes
Temp. range	-55 °C to 125 °C	

Notes:

(1)SMD: standard microcircuit drawing

(2)EPPL = ESA preferred part list

Contact your ST sales office for information on the specific conditions for products in die form and QML-Q versions.

This is information on a product in full production. www.st.com

Contents

1 Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (voltage difference between -V_{CC} and V_{CC} pins)	18	V
V_{id}	Differential input voltage [(1)]	±1.2	
V_{in}	Input voltage [(2) (3)]	-V_{CC} - 0.3 V to V_{CC} + 0.3 V	
I_{in}	Input current	45	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction to ambient area [(4)]	TBD	°C/W
R_{thjc}	Thermal resistance junction to case [(4)]	TBD	
ESD	HBM: human body model [(5)]	2	kV
T_{Lead}	Lead temperature (soldering, 10 s)	260	°C

Notes:

(1)The differential voltage is the voltage difference between the pins +IN and -IN of a channel.

(2)All voltage values except the differential voltage are with respect to the network ground terminal.

(3)The voltage on either input must never exceed V_{CC} + 0.3 V nor 16 V.

(4)Short circuits can cause excessive heating and destructive dissipation. Values are typical.

(5)Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

Table 3: Operating conditions

Symbol	Parameter	Value	Unit
(V_{CC}) - (-V_{CC})	Supply voltage	4 to 14 [(1)]	V
V_{icm}	Common-mode input voltage	-V_{CC} to V_{CC}	
T_{oper}	Operating free-air temperature range	-55 to 125	°C

Notes:

(1)SEL-free up to 120 MeV.cm^2/mg

2 Electrical characteristics

Table 4: VCC = 7 V, -VCC = -7 V, Vicm = 0 V, Tamb = 25 °C, loads (RL, CL) connected to GND (unless otherwise specified)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
DC performance							
V_{io}	Offset voltage	Vicm = 7 V	-55 °C			700	µV
			25 °C			500	
			125 °C			700	
		Vicm = 0 V	-55 °C			500	
			25 °C		60	300	
			125 °C			500	
		Vicm = -7 V	-55 °C			700	
			25 °C			500	
			125 °C			700	
DV_{io}	Input offset voltage drift	No load			1		µV/°C
I_{ib}	Input bias current	No load	-55 °C			100	nA
			25 °C		6	60	
			125 °C			100	
DI_{ib}	Input offset current temperature drift	No load			100		pA/°C
I_{io}	Input offset current	No load, Vout = 0 V	-55 °C			35	nA
			25 °C		2	15	
			125 °C			35	
C_{in}	Differential input capacitance between IN and -IN		25°C		8		pF
	Input capacitance between IN (or -IN) and GND				2		
I_{CC}	Supply current per amplifier	No load	-55 °C			2.9	mA
			25 °C		2.2	2.9	
			125 °C			2.9	
CMR	Common mode rejection ratio	No load, -Vcc < Vicm < Vcc	-55 °C	72			dB
			25 °C	72	105		
			125 °C	72			
SVR	Supply voltage rejection ratio	No load, from Vcc = 2 V and -Vcc = -2 V to Vcc = 7 V and -Vcc = -7 V	-55 °C	80			
			25 °C	90	120		
			125 °C	80			
AC performance							
GBP	Gain bandwidth product	Vout = 200 mVpp, f = 100 kHz, RL = 1 kΩ, CL = 100 pF	-55 °C	3.5			MHz
			25 °C	6	8		
			125 °C	3.5			

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
F_u	Unity gain frequency	RL = 1 kΩ, CL = 100 pF	25 °C		5		
ϕm	Phase margin	RL = 1 kΩ, CL = 100 pF, G = 5	25 °C		50		Degrees
A_{VD}	Large signal voltage gain	RL = 10 kΩ, Vout = -6.5 V to 6 V	-55 °C	60			dB
			25 °C	74	85		
			125 °C	60			
SR	Slew rate	RL = 1 kΩ, Vout = -4.8 V to 4.8 V, Vout = 4.8 V to -4.8 V	-55 °C	1.7			V/µs
			25 °C	2	3.5		
			125 °C	1.7			
e_n	Equivalent input noise voltage	No load, f = 1 kHz	25 °C		7		nV/√Hz
i_n	Equivalent input noise current	No load, f = 1 kHz	25 °C		0.8		pA/√Hz
THD+e_n	Total harmonic distortion + noise	Vout = 13 Vpp, RL = 1 kΩ, CL = 100 pF, G = -5.1	25 °C		0.01		%
Output characteristics							
V_{OH}	High level output voltage	Vcc = 14 V, -Vcc = 0 V, RL = 1 kΩ	-55 °C	13.5			V
			25 °C	13.6	13.8		
			125 °C	13.5			
		Vcc = 14 V, -Vcc = 0 V, RL = 10 kΩ	-55 °C	13.6			
			25 °C	13.8	13.9		
			125 °C	13.6			
V_{OL}	Low level output voltage	Vcc = 14 V, -Vcc = 0 V, RL = 1 kΩ	-55 °C			0.3	
			25 °C		0.12	0.2	
			125 °C			0.3	
		Vcc = 14 V, -Vcc = 0 V, RL = 10 kΩ	-55 °C			0.2	
			25 °C		0.04	0.08	
			125 °C			0.2	
I_{out} [(1)]	Output sink current	Vout = Vcc, no load, Vid = -1 V	-55 °C	15			mA
			25 °C	20	35		
			125 °C	15			
	Output source current	Vout = -Vcc, no load, Vid = 1 V	-55 °C	10			
			25 °C	15	30		
			125 °C	10			

Notes:

[(1)]These tests are performed during a very short period of time. Excessive heating can damage the device. In the application, the junction temperature must never exceed 150 °C.

Table 5: VCC = 2 V, -VCC = -2 V, Vicm = 0 V, Tamb = 25 °C, loads (RL, CL) connected to GND (unless otherwise specified)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
DC performance							
V_{io}	Offset voltage	Vicm = 2 V	-55 °C			700	µV
			25 °C			500	
			125 °C			700	
		Vicm = 0 V	-55 °C			500	
			25 °C		60	300	
			125 °C			500	
		Vicm = -2 V	-55 °C			700	
			25 °C			500	
			125 °C			700	
DV_{io}	Input offset voltage drift	No load			1		µV/°C
I_{ib}	Input bias current	No load	-55 °C			100	nA
			25 °C		11	60	
			125 °C			100	
DI_{ib}	Input offset current temperature drift	No load			100		pA/°C
I_{io}	Input offset current	No load, Vout = 0 V	-55 °C			35	nA
			25 °C		2	15	
			125 °C			35	
C_{in}	Differential input capacitance between IN and -IN		25°C		8		pF
	Input capacitance between IN (or -IN) and GND				2		
I_{CC}	Supply current per amplifier	No load	-55 °C			2.6	mA
			25 °C		2	2.6	
			125 °C			2.6	
CMR	Common mode rejection ratio	No load, -Vcc < Vicm < Vcc	-55 °C	72			dB
			25 °C	72	95		
			125 °C	72			
AC performance							
GBP	Gain bandwidth product	Vout = 200 mVpp, f = 100 kHz, RL = 1 kΩ, CL = 100 pF	-55 °C	3.5			MHz
			25 °C	6	8		
			125 °C	3.5			
F_u	Unity gain frequency	RL = 1 kΩ, CL = 100 pF	25 °C		5		
ϕm	Phase margin	RL = 1 kΩ, CL = 100 pF, G = 5	25 °C		50		Degrees
A_{VD}	Large signal voltage gain	RL = 10 kΩ, Vout = -1.5 V to 0.5 V	-55 °C	60			dB
			25 °C	70	80		

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
A_{VD}	Large signal voltage gain	RL = 10 kΩ, Vout = -1.5 V to 0.5 V	125 °C	60			dB
SR	Slew rate	RL = 1 kΩ, Vout = -1.28 V to 1.28 V, Vout = 1.28 V to -1.28 V	-55 °C	1.7			V/µs
			25 °C	2	3.1		
			125 °C	1.7			
e_n	Equivalent input noise voltage	No load, f = 1 kHz	25 °C		7.5		nV/√Hz
i_n	Equivalent input noise current	No load, f = 1 kHz	25 °C		0.8		pA/√Hz
THD+e_n	Total harmonic distortion + noise	Vout = 3 Vpp, RL = 1 kΩ, CL = 100 pF, G = -5.1	25 °C		0.01		%
Output characteristics							
V_{OH}	High level output voltage	Vcc = 4 V, -Vcc = 0 V, RL = 1 kΩ	-55 °C	3.75			V
			25 °C	3.8	3.9		
			125 °C	3.75			
		Vcc = 4 V, -Vcc = 0 V, RL = 10 kΩ	-55 °C	3.75			
			25 °C	3.85	3.95		
			125 °C	3.75			
V_{OL}	Low level output voltage	Vcc = 4 V, -Vcc = 0 V, RL = 1 kΩ	-55 °C			0.2	
			25 °C		0.05	0.1	
			125 °C			0.2	
		Vcc = 4 V, -Vcc = 0 V, RL = 10 kΩ	-55 °C			0.1	
			25 °C		0.03	0.07	
			125 °C			0.1	
I_{out} (1)	Output sink current	Vout = Vcc, no load, Vid = -1 V	-55 °C	15			mA
			25 °C	20	35		
			125 °C	15			
	Output source current	Vout = -Vcc, no load, Vid = 1 V	-55 °C	10			
			25 °C	15	30		
			125 °C	10			

Notes:

(1)These tests are performed during a very short period of time. Excessive heating can damage the device. In the application, the junction temperature must never exceed 150 °C.

3 Electrical characteristic curves

Figure 1: Input offset voltage distribution

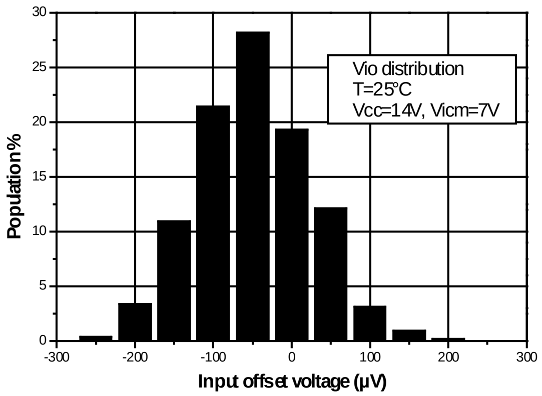


Figure 2: Input bias current vs. supply voltage

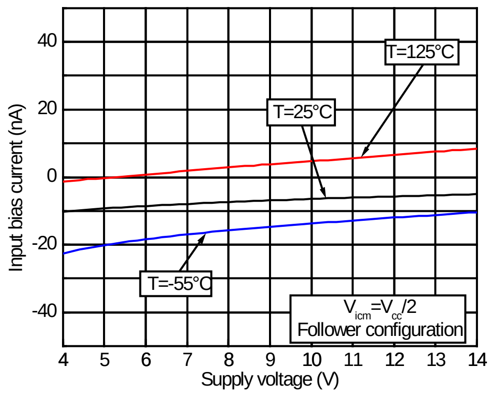


Figure 3: Input bias current vs Vicm at VCC = 4 V

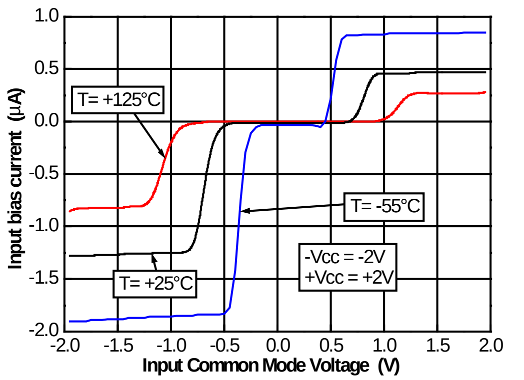


Figure 4: Input bias current vs Vicm at VCC = 14 V

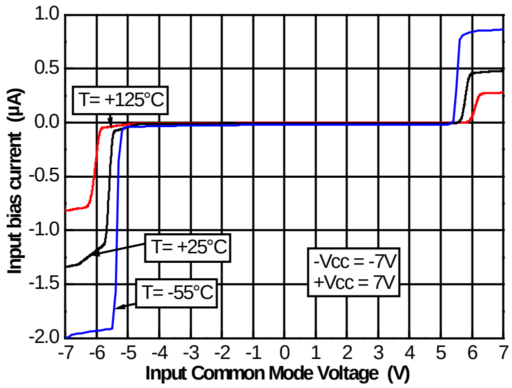


Figure 5: Supply current vs. Vicm in follower configuration at VCC = 4 V

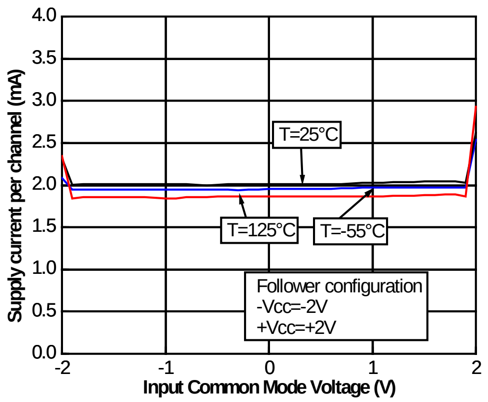


Figure 6: Supply current vs. Vicm in follower configuration at VCC = 14 V

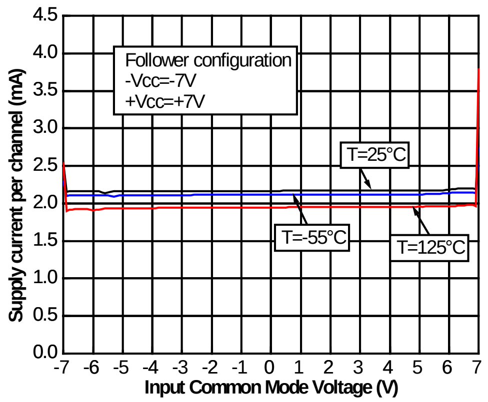


Figure 7: Supply current vs. supply voltage at Vicm = VCC/2

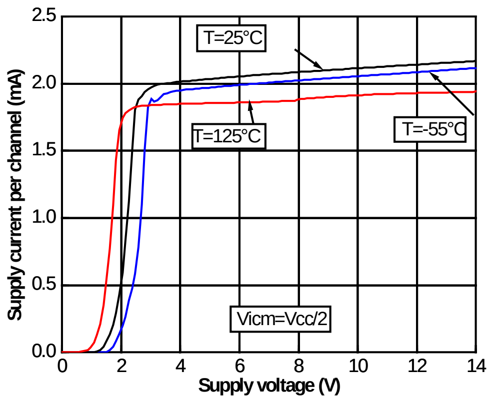


Figure 8: Output current vs. supply voltage at Vicm = VCC/2

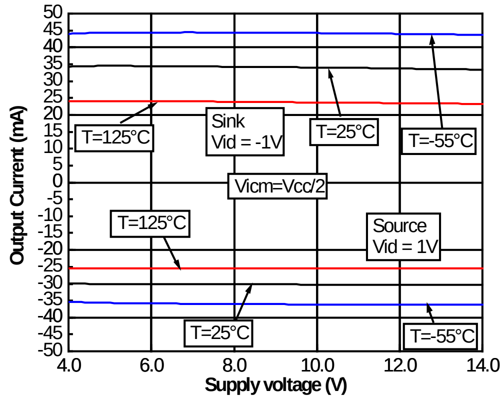


Figure 9: Output current vs. output voltage at VCC = 4 V

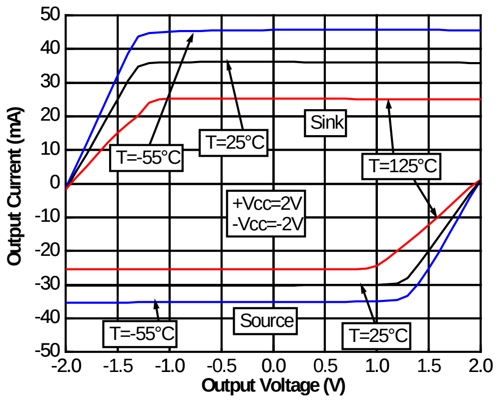


Figure 10: Output current vs. output voltage at VCC = 14 V

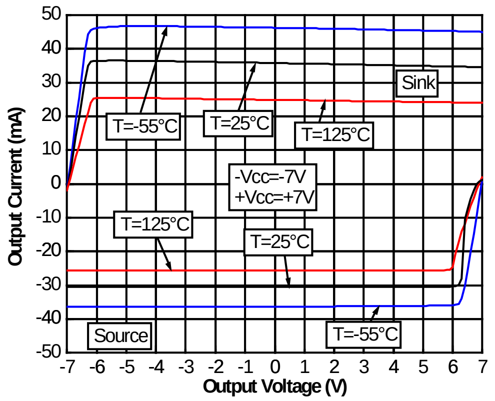


Figure 11: Differential input voltage vs. output voltage at VCC = 4 V

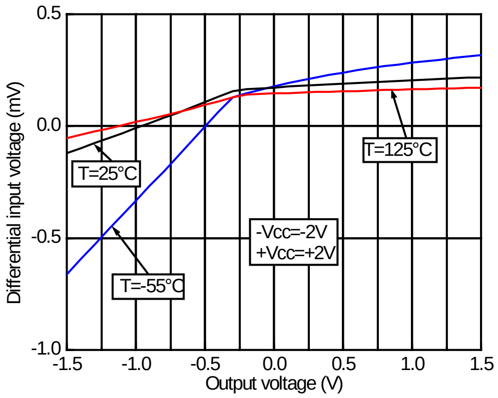


Figure 12: Differential input voltage vs. output voltage at VCC = 14 V

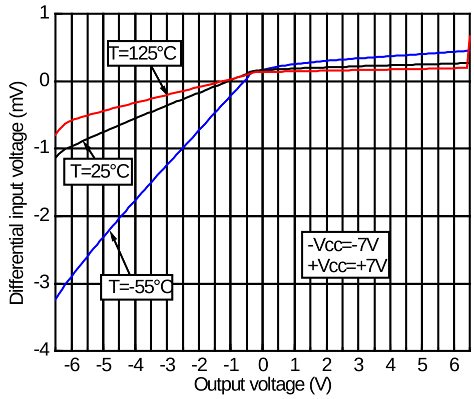


Figure 13: Noise vs. frequency at VCC = 4 V and VCC = 14 V

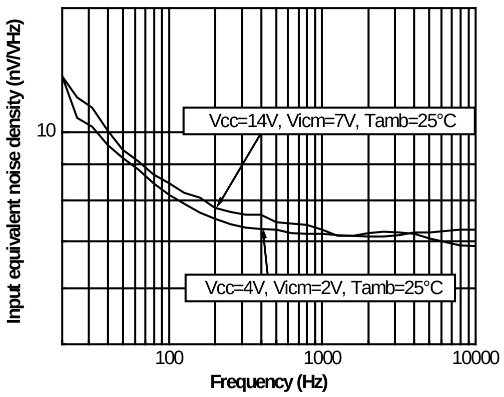


Figure 14: Voltage gain and phase vs. frequency at VCC = 4 V, Vicm = 2 V

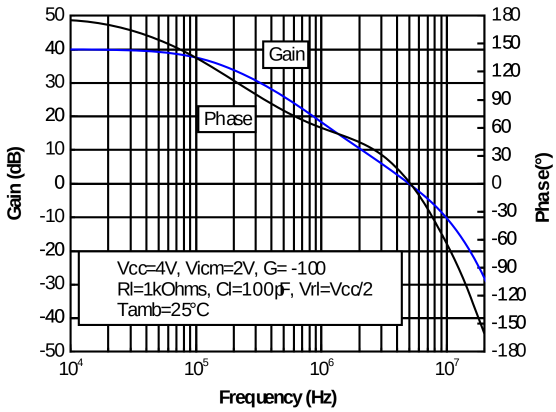


Figure 15: Voltage gain and phase vs. frequency at VCC = 4 V, Vicm = 3.5 V

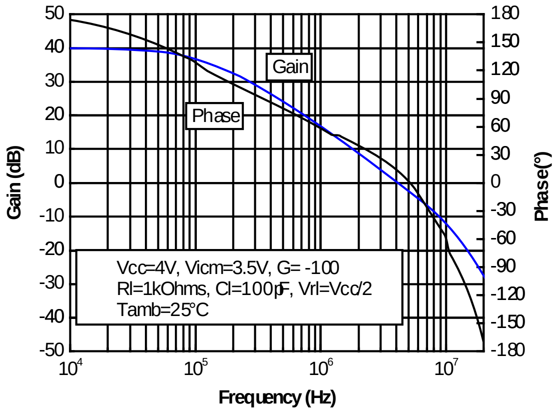


Figure 16: Voltage gain and phase vs. frequency at VCC = 4 V, Vicm = 0.5 V

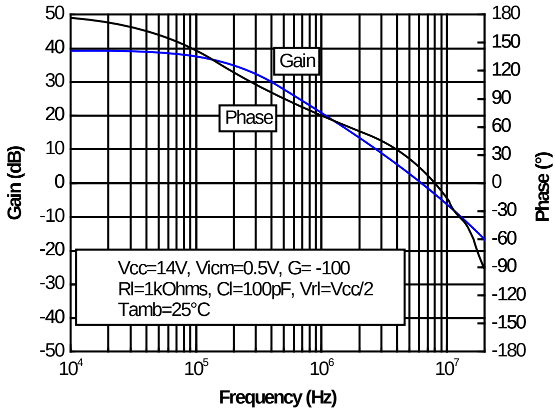


Figure 17: Voltage gain and phase vs. frequency at VCC = 14 V, Vicm = 7 V

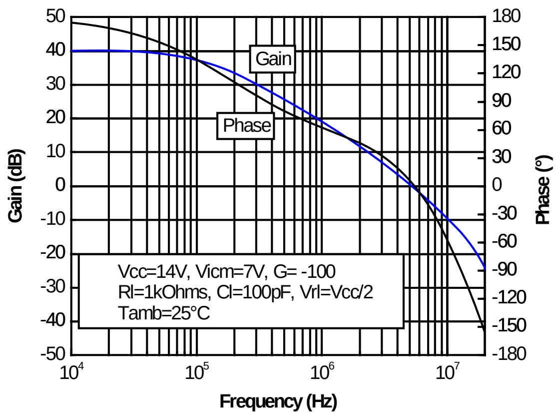


Figure 18: Voltage gain and phase vs. frequency at VCC = 14 V, Vicm = 13.5 V

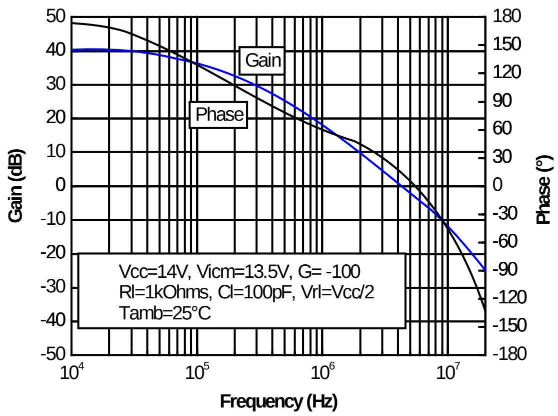


Figure 19: Voltage gain and phase vs. frequency at VCC = 14 V, Vicm = 0.5 V

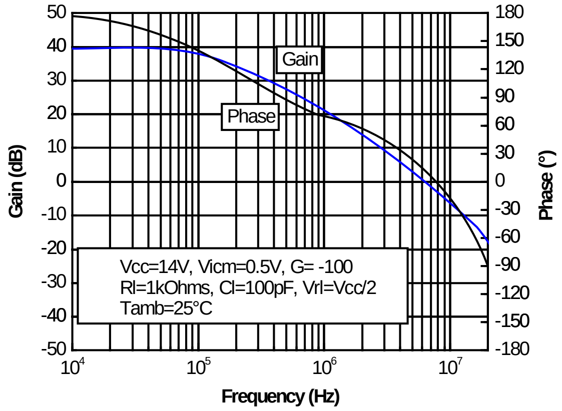


Figure 20: Positive slew rate at VCC = 4 V

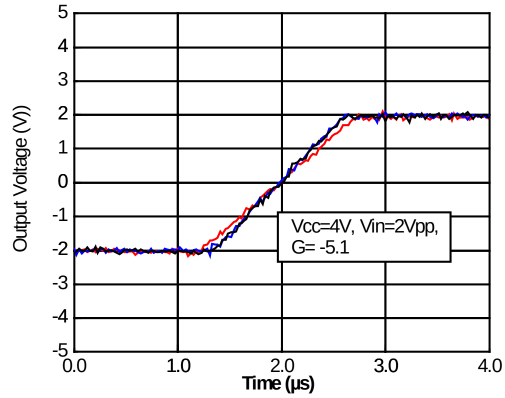


Figure 21: Negative slew rate at VCC = 4 V

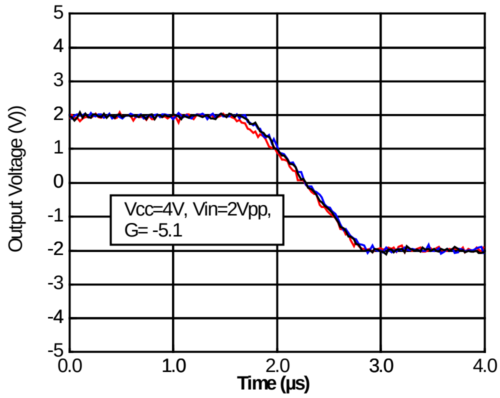


Figure 22: Positive slew rate at VCC = 14 V

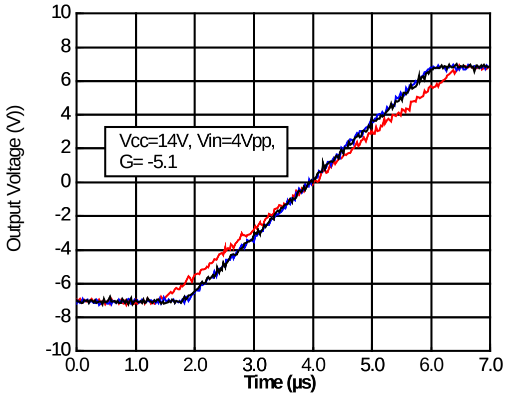
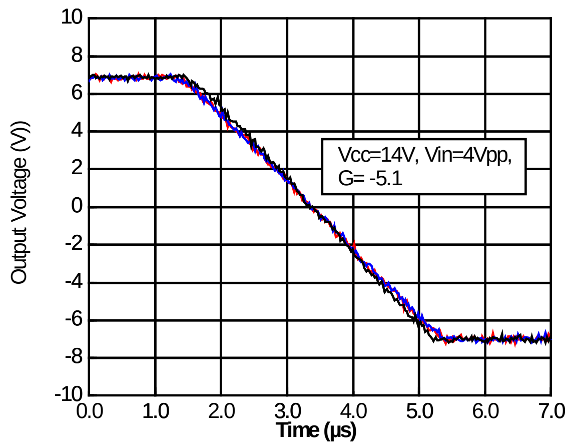


Figure 23: Negative slew rate at VCC = 14 V



4 Radiations

4.1 Introduction

Table 6 summarizes the radiation performance of the RHF484.

Table 6: Radiations

Type	Features		Value	Unit
TID	High-dose rate		300	krad
	Low-dose rate		300	
	ELDRS		300	
Heavy ions	SEL immunity (at 125 °C) up to:		110	MeV.cm²/mg
	SET characterized	Inverting	LET_{th} = 1	MeV.cm²/mg
			σ = 3.10E-03	cm²/device
		Non-inverting	LET_{th} = 1	MeV.cm²/mg
			σ = 3.20E-03	cm²/device
		Subtracting	LET_{th} = 1	MeV.cm²/mg
			σ = 2.80E-03	cm²/device

4.2 Total ionizing dose (TID)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MILSTD-883 test method 1019 specification.

The RHF484 is RHA QML-V qualified, and is tested and characterized in full compliance with the MIL-STD-883 specification. It using a mixed bipolar and CMOS technology and is tested both below 10 mrad/s (low dose rate) and between 50 and 300 rad/s (high dose rate).

- The ELDRS characterization is performed in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.
- Each wafer lot is tested at high-dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

4.3 Heavy ions

The heavy ion trials are performed on qualification lots only. No additional test is performed.

5 Achieving good stability at low gain

At low frequencies, the RHF484 can be used in a low gain configuration as shown in *Figure 24*. At lower frequencies, the stability is not affected by the value of the gain, which can be set close to 1 V/V (0 dB), and is reduced to its simplest expression G1 = 1+Rfb/Rg. Therefore, an R-C cell is added in the gain network so that the gain is increased (up to 5) at higher frequencies (where the stability of the amplifier could be affected). At higher frequencies, the gain becomes G2 = 1+Rfb/(Rg//R).

Figure 24: Low gain configuration

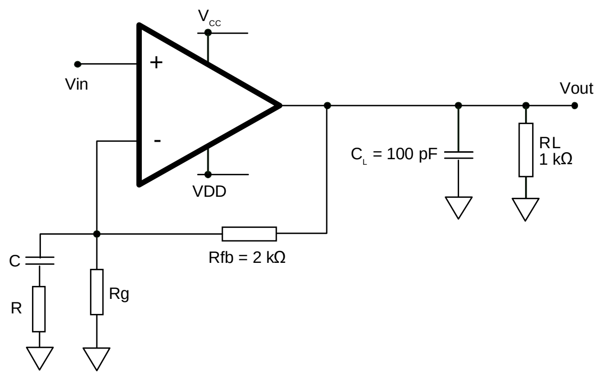
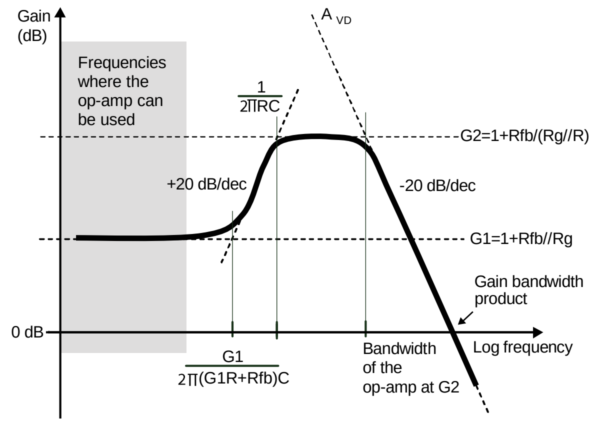


Figure 25: Closed-loop gain



Rg becomes a complex impedance. The closed-loop gain features a variation in frequency and can be expressed as *Equation 1*.

Equation 1

$$\text{Gain} = G1\frac{1 + jC\omega \times \left(\frac{G1R + Rfb}{G1}\right)}{1 + jCR\omega}$$

Where a pole appears at 1/2πRC and a zero at G1/2π(G1R+Rfb)C. The frequency can be plotted as shown in *Figure 25*.

Table 7: External components versus low-frequency gain

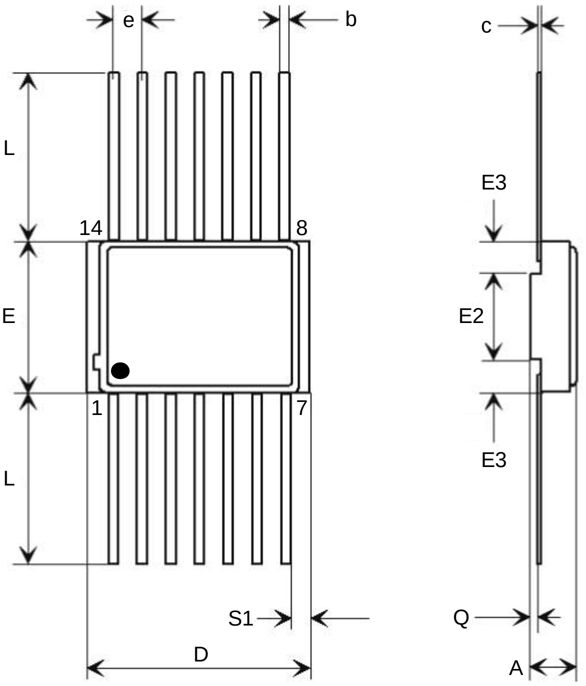
<table>
<tr><th>G1 (v/V)</th><th>R (Ω)</th><th>C (nF)</th><th>Rg (Ω)</th><th>Rfb (Ω)</th></tr>
<tr><td>1.1</td><td rowspan="4">510</td><td rowspan="4">1</td><td>20 k</td><td rowspan="3">2 k</td></tr>
<tr><td>2</td><td>2 k</td></tr>
<tr><td>3</td><td>1 k</td></tr>
<tr><td>4</td><td>750</td><td>2.4 k</td></tr>
<tr><td>5</td><td>Not connected</td><td>Not connected</td><td>820</td><td>3.3 k</td></tr>
</table>

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 Wide ceramic Flat-14W package information

Figure 26: Wide ceramic Flat-14W package outline



The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or VCC will not affect the electrical characteristics.

Table 8: Wide ceramic Flat-14W mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.93	2.11	2.29	0.076	0.083	0.090
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.18	0.004	0.005	0.007
D	9.71	9.91	10.11	0.382	0.390	0.398
E	7.27	7.42	7.57	0.286	0.292	0.298
E2		5.4			0.213	
E3	0.76			0.030		
e		1.27			0.050	
L	6.3		6.6	0.248		0.260
Q	0.20		0.28	0.008		0.011
S1	0.13			0.005		

7 Ordering information

Table 9: Ordering information

Order code	SMD pin	EPPL [(1)]	Quality level	Package	Lead finish	Marking [(2)]	Packing
RHF484K1	-	-	Engineering model	Flat-14W	Gold	RHF484K1	Strip pack
RHF484K-01V	5962F0822201VXC	Yes	QML-V flight			5962F0822201VXC	

Notes:

[(1)]EPPL = ESA preferred part list

[(2)]Specific marking only. Complete marking includes the following:
- SMD pin (as indicated in above table)
- ST logo
- Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
- QML logo (Q or V)
- Country of origin (FR = France).

Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

8 Other information

8.1 Date code

The date code is structured as shown below:

- EM xyywwz
- QML-V yywwz
  where:
  - x (EM only) = 3 and the assembly location is Rennes, France
  - yy = last two digits of the year
  - ww = week digits
  - z = lot index in the week

8.2 Documentation

Table 10: Documentation provided for each type of product

Quality level	Documentation
Engineering model	—
QML-V flight	Certificate of conformance
	QCI (groups A, B, C, D, and E) (1)
	Screening electrical data
	Precap report
	PIND test (2)
	SEM inspection report (3)
	X-ray report

Notes:

(1)QCI = quality conformance inspection

(2)PIND = particle impact noise detection

(3)SEM = scanning electron microscope

9 Revision history

Table 11: Document revision history

Date	Revision	Changes
26-Apr-2011	1	Initial release
06-Feb-2015	2	Replaced package silhouette and added marker to show position of pin 1 on the silhouette, pinout, and package drawing. Updated Features Updated Table 1: Device summary Table 2: Absolute maximum ratings: transferred radiation information to Section 3. Added Section 3: Radiations Section 5.1: Wide ceramic Flat14W package information: added "W" to package information. Updated Section 6: Ordering information Added Section 7: Other information
06-Apr-2016	3	Updated document layout *Table 1: "Device summary"*: updated footnote 1, SMD = standard microcircuit drawing.

IMPORTANT NOTICE – PLEASE READ CAREFULLY