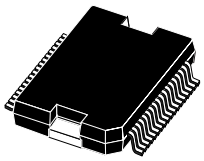
L9347

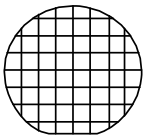
Intelligent quad (2x5A/2x2.5A) low-side switch

Features

- Quad low-side switch
- 2 x 5A designed as conventional switch
- 2 x 2.5A designed as switched current-regulator
- Low ON resistance 2 x 0.2Ω, 2 x 0.35Ω (typ.)
- Power SO-36 package with integrated cooling area
- Integrated free wheeling and clamping Z diodes
- Output slope control
- Short circuit protection
- Selective overtemperature shutdown
- Open load detection
- Ground and supply loss detection
- External clock control
- Recirculation control
- Regulator drift detection
- Regulator error control
- Regulator resolution 5mA
- Status monitoring
- Status push-pull stages
- Electrostatic discharge (ESD) protection



PowerSO-36



Bare Die

Description

The L9347 is an integrated quad low-side power switch to drive inductive loads like valves used in ABS systems. Two of the four channels are current regulators with current range from 250mA to 2.25A and an accuracy of 10%.

All channels are protected against fail functions. They are monitored by a status output.

Table 1. Device summary

Part number	Package	Packing
L9347LF	PowerSO-36	Tray
L9347LF-TR	PowerSO-36	Tape and reel
L9347DIE1	Bare die	Bare die

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Figure 1. Block diagram

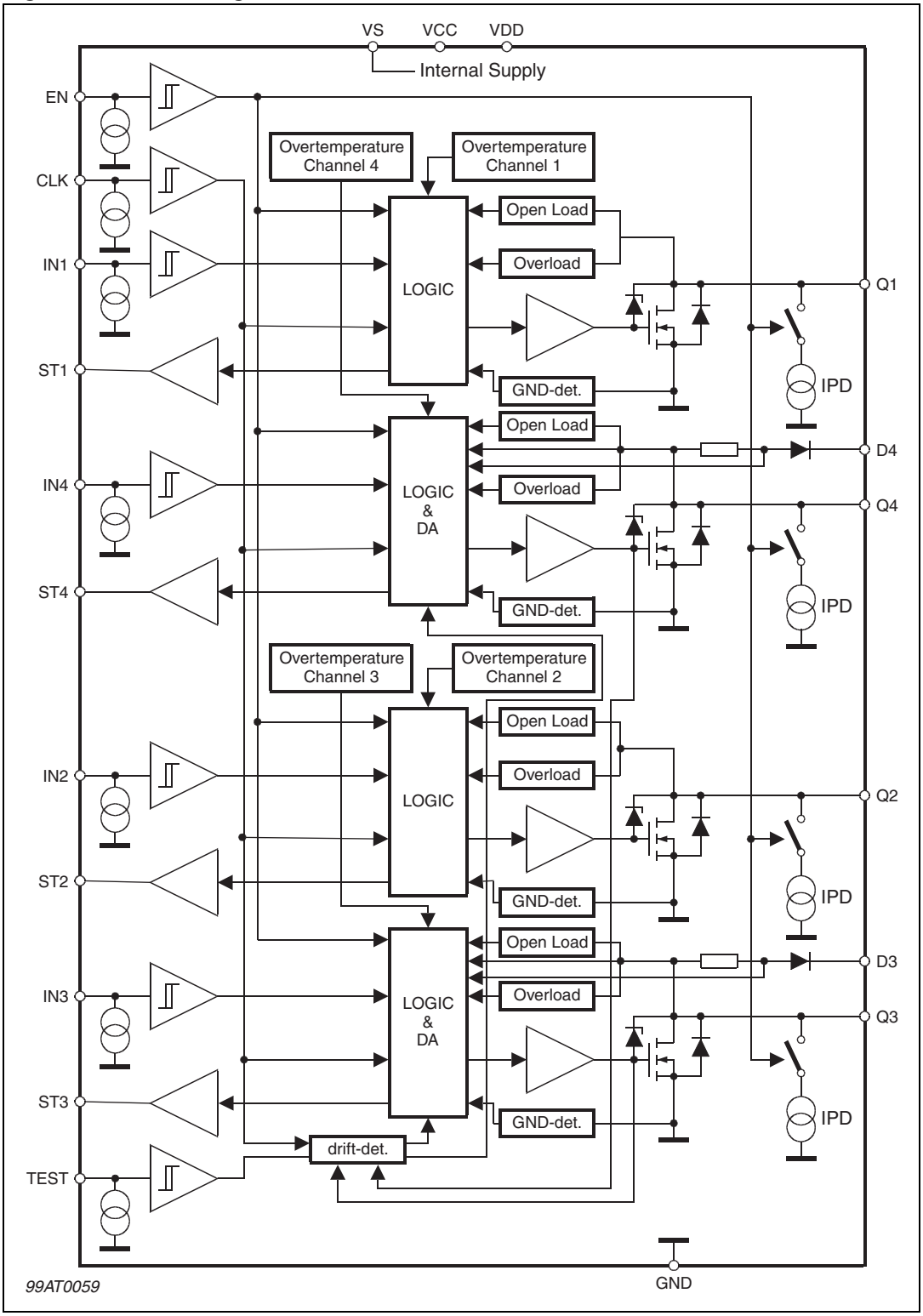


Figure 2. Pin connections

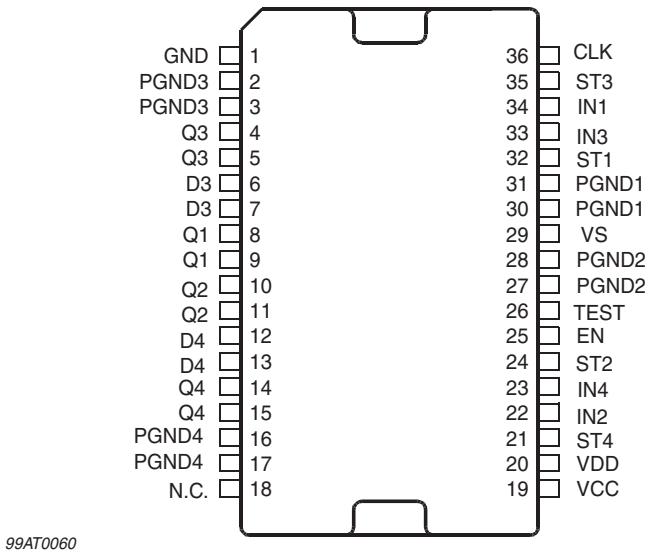


Table 2. Pin description

N°	Pin	Function
1	GND	Logic Ground
2, 3	PGND 3	Power Ground Channel 3
4, 5	Q 3	Power Output Channel 3
6, 7	D 3	Free-Wheeling Diode Channel 3
8, 9	Q 1	Power Output Channel 1
10, 11	Q 2	Power Output Channel 2
12, 13	D 4	Free-Wheeling Diode Channel 4
14, 15	Q 4	Power Output Channel 4
16, 17	PGND 4	Power Ground Channel 4
18	NC	Not Connected
19	VCC	5V Supply
20	VDD	5V Supply
21	ST 4	Status Output Channel 4
22	IN 2	Control Input Channel 2
23	IN 4	Control Input Channel 4
24	ST 2	Status Output Channel 2
25	EN	Enable Input for all four Channels
26	TEST	Enable Input for Drift detection
27, 28	PGND 2	Power Ground Channel 2
29	VS	Supply Voltage

Table 2. Pin description (continued)

N°	Pin	Function
30, 31	PGND 1	Power Ground Channel 1
32	ST 1	Status Output Channel 1
33	IN 3	Control Input Channel 3
34	IN 1	Control Input Channel 1
35	ST 3	Status Output Channel 3
36	CLK	Clock Input

2 Electrical specifications

Table 3. Electrical characteristcs:
(Vs = 4.8 to 18V; T_j = -40 to 150°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power supply						
I_{SON}	Supply current	$V_S \leq 18V$ (outputs ON)			5	mA
I_{SOFF}	Quiescent current	$V_S \leq 18V$ (outputs OFF)			5	mA
I_{cc}	Supply current VCC (analog supply)	VCC =5V			5	mA
I_{dd}	Supply current VDD (digital supply)	VDD =5V f_{CLK}=0Hz			5	uA
I_{dd}	Supply current VDD (digital supply)	VDD =5V f_{CLK}=250kHz			5	mA
General diagnostic functions						
V_{QU}	Open load voltage	$V_S \geq 6.5V$ (outputs OFF)	0.3	0.33	0.36	x V_Q
V_{thGND}	Signal-GND-loss threshold	VCC= 5V	0.1		1	V
V_{thPGL}	Power-GND-loss threshold	VCC= 5V	1.5	2.5	3.5	V
$f_{CLK,min}$	Clock frequency error		10		100	kHz
DC_{CLKe_low}	Clock duty cycle error detection low	f_{CLK}= 250 kHz		33,3	45	%
DC_{CLKe_high}	Clock duty cycle error detection high	f_{CLK}= 250 kHz	55	66,6		%
VS_{loss}	Supply detection	VCC = VDD = 5V	2		4.5	V
Additional diagnostic functions channel 1 and channel 2 (non regulated channels)						
$I_{QU1,2}$	Open-load current channel 1, 2	$V_S \geq 6.5V$	50		140	mA
$I_{QO1,2}$	Over-load current channel 1, 2	$V_S \geq 6.5V$	5	7.5	9	A
Additional diagnostic functions channel 3 and channel 4 (regulated channels)						
DC_{OUT}	Output duty cycle range	filtered with 10ms	10		90	%
$I_{QO3,4}$	Overload current channel 3,4	$V_S \geq 6.5V$	2.5	5	8	A
V_{rerr}	Recirculation error shutdown threshold (open D3/D4)	Iout > 50mA	45	50	60	V
PWM_{dOUT}	Output PWM ratio during drift comparison	$V_{IN3} = V_{IN4} = PWM_{IN}$ V_{TEST} = H	-14.3		+14.3	%
Digital inputs (IN1 to IN4, ENA, CLK, TEST). The valid PWM-Ratio for IN3/IN4 is 10% to 90%						
V_{IL}	Input low voltage		-0.3		1	V
V_{IH}	Input high voltage		2		6	V
V_{IHy}	Input voltage hysteresis (1)		20		500	mV

Table 3. Electrical characteristcs: (continued)
(Vs = 4.8 to 18V; T_j = -40 to 150°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_I	Input pull down current	V_{IN} = 5V, $V_S \geq$ 6.5V	8	20	40	µA
Digital outputs (ST1 to ST4)						
V_{STL}	Status output voltage in low state (2)	$I_{ST} \leq$ 40µA	0		0.4	V
V_{STH}	Status output voltage in high state (2)	$I_{ST} \geq$ -40µA	2.5		3.45	V
		$I_{ST} \geq$ -120µA	2		3.45	V
R_{DIAGL}	R_{OUT} + R_{DSON} in low state		0.3	0.64	1.5	kΩ
R_{DIAGH}	R_{OUT} + R_{DSON} in high state		1.5	3.2	7.0	kΩ
Power outputs (Q1 to Q4)						
$R_{DSON1,2}$	Static drain-source ON-resistance Q1 and Q2 (non-reg. channels)	I_Q = 1A; $V_S \geq$ 9.5V T_j = 25°C T_j = 125°C(3) T_j = 150°C(4)		 0.2	 0.5 0.5	 W W W
$R_{DSON3,4}$	Static drain-source ON-resistance Q3 and Q4 (reg. channels)	I_Q = 1A; $V_S \geq$ 9.5V T_j = 25°C T_j = 125°C (3) T_j = 150°C (4)		 0.35	 0.75 0.75	 Ω Ω Ω
V_{F_250mA}	Forward voltage of free wheeling path D3, D4 @250mA	$I_{D3/4}$ = -250mA	0.5		1.5	V
$V_{F\_2.25A}$	Forward voltage of free wheeling path D3, D4 @2.25A	$I_{D3/4}$ = -2.25A	2.0		4.5	V
R_{sens}	Sense resistor = ($V_{F\_2.25A}$-V_{F_250mA})/2A			1		Ω
V_Z	Z-diode clamping voltage	$I_Q \geq$ 100mA	45		60	V
I_{PD}	Output pull down current	V_{EN} = H, V_{IN} = L	10		150	µA
I_{Qlk}	Output leakage current	V_{EN} = L; V_Q = 20V			5	µA
Timing						
t_{ON}	Output ON delay time	I_Q = 1A	0	5	20	µs
t_{OFF}	Output OFF delay time channel	I_Q = 1A	0	10	30	µs
t_{OFFREG}	Output OFF delay time regulator	(5)		528		µs
t_r	Output rise time	I_Q = 1A	0.5	1.5	8	µs
t_f	Output fall time	I_Q = 1A	0.5	1.5	8	µs
t_{sf}	Short error detection filter time	f_{CLK} = 250kHz DC = 50%(5)	4		8	µs
t_{lf}	Long error detection filter time	f_{CLK} = 250kHz DC = 50%(5)	16		32	µs
t_{SCP}	Short circuit switch-OFF delay time	(5)	4		30	µs

Table 3. Electrical characteristcs: (continued)
(Vs = 4.8 to 18V; T_j = -40 to 150°C unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_D	Status delay time	(5)	896		1024	us
t_{RE}	Regulation error status delay time	(5) (reg. channels only)		10		ms
t_{Dreg}	Output off status delay time	(5) (reg. channels only		528		µs
Reg. current accuracy (reg. channels only)						
$I_{Q3/Q4}$	Minimum current	DC = 10%	200	250	300	mA
$I_{Q3/Q4}$	Maximum current	DC = 90%	2	2.25	2.5	A
I_{REG}	Max. regulation deviation @ DC 10% - 90%	250mA < $I_{Q3/Q4}$ < 400mA 400mA ≤ $I_{Q3/Q4}$ ≤ 800mA 800mA < $I_{Q3/Q4}$ < 2.25A			±10 ±6 ±10	% % %
$\Delta I_{Q3/Q4}$	Min. quant. step			5		mA
Frequencies						
	CLK frequency	crystal-controlled		250		kHz
	Input PWM frequency	(reg. channels only)		2		kHz

1. This parameter will not be tested but assured by design
2. Short circuit between two digital outputs (one in high the other in low state) will lead to the defined result "LOW"
3. Measured chip, bond wires not included
4. Measured on Power SO-36 devices
5. Digital filtered with external clock, only functional test

Table 4. Absolute maximum ratings
The absolute maximum ratings are the limiting values for this device. Damage may occur if this device is subjected to conditions which are beyond these values

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
E_Q	Switch off energy for inductive loads				50	mJ
Voltages						
V_S	Supply voltage		-0.3		40	V
V_{CC}, V_{DD}	Supply voltage		-0.3		6	V
V_Q	Output voltage static				40	V
V_Q	Output voltage during clamping	t < 1ms			60	V
V_{IN}, V_{EN}	Input voltage IN1 to IN4, EN	I_I < |10|mA	-1.5		6	V
V_{CLK}	Input Voltage CLK		-1.5		6	V
V_{ST}	Output voltage status		-0.3		6	V
V_D	Recirculation circuits D3, D4				40	V
V_{DRmax}	max. reverse breakdown voltage of free wheeling diodes D3, D4				55	V

Table 4. Absolute maximum ratings (continued)

The absolute maximum ratings are the limiting values for this device. Damage may occur if this device is subjected to conditions which are beyond these values

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Currents						
$I_{Q1/2}$	Output current for Q1 and Q2		>5		internal limited	A
$I_{Q3/4}$	Output current for Q3 and Q4		>3		internal limited	A
$I_{Q1/2}$, $I_{PGND1/2}$	Output current at reversal supply for Q1 and Q2		-4			A
$I_{Q3/4}$, $I_{PGND3/4}$	Output current at reversal supply for Q3 and Q4		-2			A
I_{ST}	Output current status pin		-5		5	mA
ESD Protection						
ESD	Electrostatical Discharging	MIL883C	±2			kV
ESD	Output Pins (Qx, Dx)	vs. Common GND (PGND1-4 + GND)	±4			kV

Table 5. Thermal data

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_j	Junction temperature	T_j	-40		150	°C
T_{jc}	Junction temperature during clamping (life time)	Σt = 30min Σt = 15min			175 190	°C
T_{stg}	Storage temperature	T_{stg}	-55		150	°C
T_{th}	Overtemperature shutdown threshold	(1)	175		200	°C
T_{hy}	Overtemperature shutdown hysteresis	(1)		10		°C
R_{thJC}	Thermal resistance junction to case	R_{thJC}			2	K/W

1. This parameter will not be tested but assured by design.

Table 6. Operating range

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage		4.8		18	V
V_{CC}, V_{DD}	Supply voltage		4.5		5.5	V
dV_S/dt	Supply voltage transient time		-1		1	V/µs
V_Q	Output voltage static		-0.3		40	V
V_Q	Output voltage induced by inductive switching	Voltage will be limited by internal Z-diode clamping			60	V
V_{ST}	Output voltage status		-0.3		6	V

Table 6. Operating range (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ST}	Output current status		-1		1	mA
T_j	Junction temperature		-40		150	°C
T_{jc}	Junction temperature during clamping	Σ = 30min Σ = 15min			175 190	°C

3 Functional Description

3.1 Overview

The L9347 is designed to drive inductive loads (relays, electromagnetic valves) in low side configuration. Integrated active Zener-clamp (for channel1 and 2) or free wheeling diodes (for channel 3 and 4) allow the recirculation of the inductive loads. All four channels are monitored with a status output. All wiring to the loads and supply pins of the device are controlled. The device is self-protected against short circuit at the outputs and overtemperature. For each channel one independent push-pull status output is used for a parallel diagnostic function.

Channel 3 and 4 work as current regulator. A PWM signal on the input defines the target output current. The output current is controlled through the output PWM of the power stage. The regulator limits of 10% or 90% are detected and monitored with the status signal. The current is measured during recirculation phase of the load.

A test mode compares the differences between the two regulators. This “drift” test compares the output PWM of the regulators. By this feature a drift of the load during lifetime can be detected.

3.2 Input circuits

The INput, CLK, TEST and ENable inputs, are active high, consist of Schmidt triggers with hysteresis. All inputs are connected to pull-down current sources.

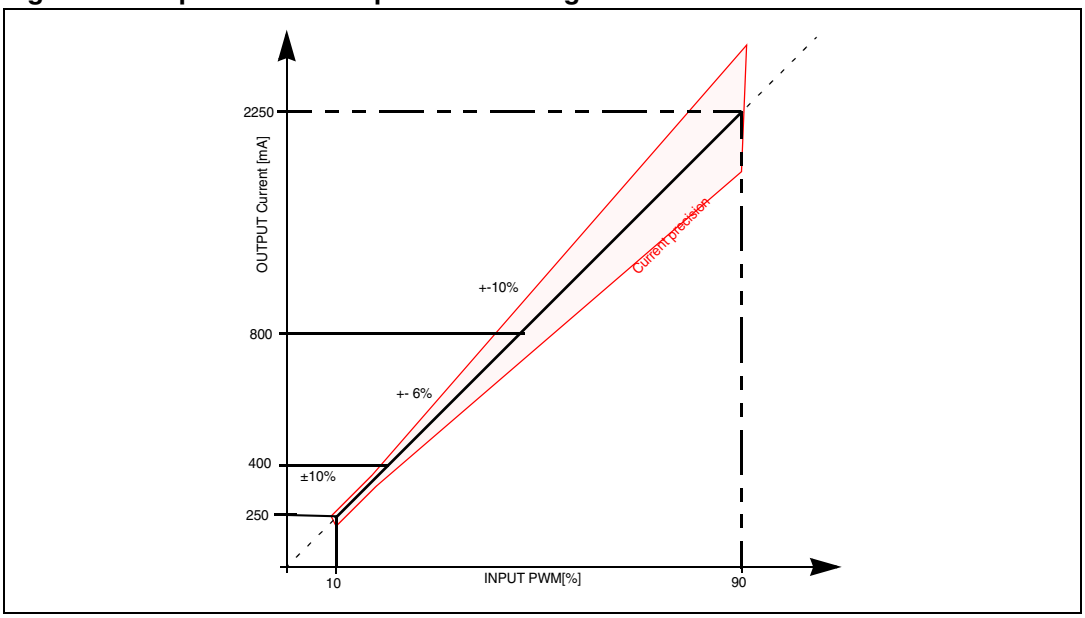
3.3 Output stages (not regulated) Channel 1 and 2

The two power outputs (5A) consist of DMOS power transistors with open drain output. The output stages are protected against short circuit. Via integrated Zener clamp diodes the overvoltage of the inductive loads due to recirculation are clamped to typ. 52V for fast shut off of the valves. Parallel to the DMOS transistors there are internal pull-down current sources. They are provided to assure an open load condition in the OFF state. With EN=low this current source is switched off, but the open load comparator is still active.

3.4 Current regulator stages Channel 3 and 4

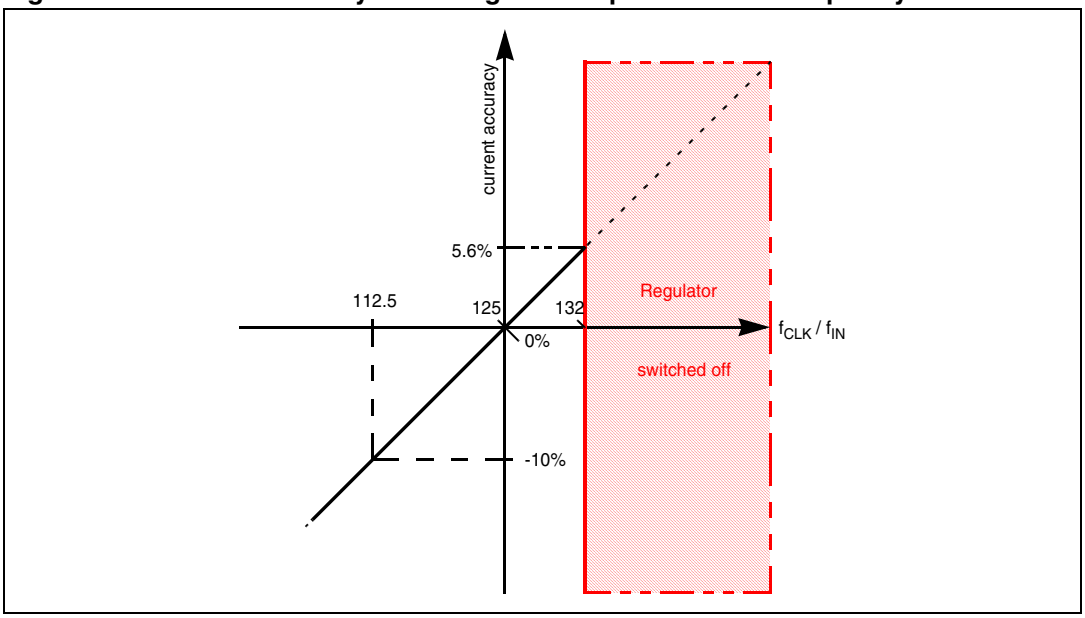
The current-regulator channels are designed to drive inductive loads. The target value of the current is given by the duty cycle (DC) of the 2kHz PWM input signal. The following figure shows the relation between the input PWM and the output current and the specified accuracy.

Figure 3. Input PWM to output current range



The ON period of the input signal is measured with a 1MHz clock, synchronized with the external 250kHz clock. For requested precision of the output current the ratio between the frequencies of the input signal and the external 250kHz clock has to be fixed according to the graph shown in *Figure 3*.

Figure 4. Current accuracy according to the input and clock frequency ratio



The theoretical error is zero for $f_{CLK} / f_{IN} = 125$.

If the period of the input signal is longer than 132 times the period of the clock the regulator is switched off. For a clock frequency lower than 100kHz the clock control will also disable the regulator. For high precision applications the clock frequency and the input frequency have to be correlated.

The output current is measured during the recirculation of the load. The current sense resistor is in series to the free wheeling diode. If this recirculation path is interrupted the regulator stops immediately and the status output remains low for the rest of the input cycle.

The output period is 64 times the clock period. With a clock frequency of 250kHz the output PWM frequency is 3.9kHz. The output PWM is synchronized with the first negative edge of the input signal. After that the output and the input are asynchronous. The first period is used to measure the current. This means the first turn-on of the power is 256µs after the first negative edge of the input signal.

As regulator a digital PI-regulator with the Transfer function for:

KI: $\frac{0.126}{z-1}$ and KP: 0.96

for a sampling time of 256µs is realised.

To speed up the current settling time the regulator output is locked to 90% output PWM untill the target current value is reached. This happens alsowhen the target current value changes and the output PWM reaches 90% during the regulation. The status output gets low if the target current value is not reached within the regulation error delay time of t_{RE}=10ms. The output PWM is than out of the regulation range from 10% to 90%.

3.5 Protective circuits

The outputs are protected against current overload, overtemperature, and power-GND-loss. The external clock is monitored by a clock watchdog. This clock watchdog detects a minimal frequency $f_{CLK,min}$ and wrong clock duty cycles. The allowed clock duty cycle range is 45% to 55%. The current-regulator stages are protected against recirculation errors, when D3 or D4 is not connected. All these error conditions shut off the power stage and invert the status output information.

3.6 Error detection

The status outputs indicate the switching state under normal conditions (status LOW = OFF; status HIGH = ON). If an error occurs, the logic level of the status output is inverted, as listed in the diagnostic table below. All external errors, for example open load, are filtered internally. The following table shows the detected errors, the filter times and the detection mode (on/off).

Table 7. Detected errors

	ON State EN &IN = HIGH	OFF State EN &IN = LOW	Filter time	Reset done by
Short circuit of the load	X		t_{sf}	EN & IN = “LOW” for T_D or T_{Dreg}
Open load (under voltage detection)		X	t_{lf}	timer T_D
Open load (under current detection)	X		t_{sf}	timer T_D
Over temperature	X		t_{sf}	EN & IN = “LOW” for T_D or T_{Dreg}
Power-GND-loss	X	X	t_{lf}	in on: EN & IN = “LOW” for T_D or T_{Dreg} in off: timer T_D
Signal-GND-loss	X	X	t_{lf}	timer T_D
Supply-VS-loss	X	X	t_{lf}	timer T_D
Clock control	X	X	no	in on: EN & IN = “LOW” for T_D or T_{Dreg} in off: timer T_D
Output voltage clamp active	X (regulated channels)		no	in on: EN & IN = “LOW” for T_D or T_{Dreg} in off: timer T_D

EN&IN=low means that at least one between enable and input is low. For the inputs IN = low means also no input PWM. For the regulator input period longer than T_{Dreg} and for the standard channel input period longer thanT_D.

A detected error is stored in an error register. The reset of this register is made with a timer T_D. With this approach all errors are present at the status output at least for the time T_D.

All protection functions like short circuit of the output, overtemperature, clock failure or power-GND-loss in ON condition are stored into an internal “fail” register. The output is then shut off. The register must be reset with a low signal at the input. A “low signal” means that the input is low for a time longer than T_D or T_{DReg} for the reulated channel, otherwise it is interpreted as a PWM input signal and the register is left in set mode.

Signal-GND-loss and VS-loss are detected in the active on mode, but they do not set the fail register. This type of error is only delayed with the standard timer t_{lf} function.

Open load is detected for all four channels in on and off state.

Open load in off condition detects the voltage on the output pin. If this voltage is below 0.33 * VS the error register is set and delayed with T_D. A sink current stage pull the output down to ground, with EN high. With EN low the output is floating in case of openload and the detection is not assured. In the ON state the load current is monitored by the non-regulated channels. If it drops below the specified threshold value I_{QU} an open load is detected and the error register is set and delayed with T_D. A regulated channel detects the open load in the on state with the current regulator error detection. If the output PWM reaches 90% for a time longer than t_{RE} than an error occurs. This could happen when no load is connected, the

resistivity of the load is too high or the supply voltage too low. The same error is shown if the regulator is not able to reduce the current in the load in the time t_{RE}, so the output PWM falls below 10%.

A clock failure (clock loss) is detected when the frequency becomes lower than $f_{CLK,min}$. All status outputs are set on error and all power outputs are shut off. The status signals remain in their state until the clock signal is present again. A clock failure during power on of VCC is detected only on the regulated channels. The status outputs of the channel 1 and 2 are low in this case.

3.7 Drift detection (regulated channels only)

The drift detection is used to compare the two regulated channels during regulation. This “Drift” test compares the output PWM of the regulators. The resistivity of the load influences the output PWM. The approximated formula for the output current below shows the dependency of the load resistor to the output PWM. In this formula the energy reduction during the recirculation is not taken into account. The real output PWM is higher. The testmode is enabled with IN,EN and TEST high. With an identical 2kHz PWM-Signal connected to the IN-inputs the output PWM must be in a range of +-14.3%. If the difference between the two on-times is more than ±14.3% of the expected value an error is detected and monitored by the status outputs, in the same way as described above, but a drift error will not be registered and also not delayed with T_D as other errors

$$IOUT = \frac{VBAT}{RL + RON} \cdot PWM$$

Drift Definition:

Drift = PWM(1+E) - PWM (1-E) = 2PWM E

Drift * 4 < PWM (1+E)

with E >14.3% a drift is detected

E.. not correlated Error of the channels

%PWM ... Corresponding ideal output PWM to a given input PWM

A 7bit output-PWM-register is used for the comparison. The register with the lower value is subtracted from the higher one. This result is multiplied by four and compared with the higher value.

3.8 Other test modes

The test pin is also used to test the regulated channels in the production. With a special sequence on this pin the power stages of the regulated channels can be controlled direct from the input. No status feedback of the regulated channels is given. The status output is clocked by the regulator logic. The output sequence is a indication of a proper logic functionality. The functionality of this special test mode is shown in *Table 8*.

Table 8. Special test mode functionality

EN	In	Test	Out	Status	Note
1	X	X	X	X	disable test mode
1	1	1	on	1	Drift mode
0	X	⎍	off	test pattern	test condition one
0	X	⎍⎍	off	test pattern	test condition two
0	X	⎍⎍⎍	off	test pattern	test condition three
0	0	⎍⎍⎍⎍	off	test pattern	test condition four
0	1	⎍⎍⎍⎍	on	test pattern	test condition four

For more details about the test conditions see timing diagrams in *Section 4*.

3.9 Diagnostic table

The status follows the input signal in normal operating conditions.
If any error is detected the status is inverted.

Table 9. Diagnostic table

Operating Condition	Test Input TEST	Enable Input ENA	Control Input non-reg./reg. IN	Power Output/Current reg. Q	Status Output ST
Normal function	L	L	L	OFF	L
	L	L	H/PWM	OFF	L
	L	H	L	OFF	L
	L	H	H/PWM	ON	H
Open load or short to ground	L	L	L	OFF	X
	L	L	H/PWM	OFF	X
	L	H	L	OFF	H
	L	H	H/PWM	ON	L
Overload or short to supply	L	H	H/PWM	OFF	L
Latched overload	L	H	H/PWM	OFF	L
Reset latch	L	H –> L	X	OFF	L
Reset latch	L	H	H/PWM –> L	OFF	L
Overtemperature	L	H	H/PWM	OFF	L
Latched overtemperature	L	H	H/PWM	OFF	L
Reset latch	L	H –> L	X	OFF	L
Reset latch	L	H	H/PWM –> L	OFF	L
Recirculation error (reg.chn.)	L	H	PWM	OFF	L
Latched error	L	H	PWM	OFF	L
Reset latch	L	H –> L	X	OFF	L
Reset latch	L	H	PWM –> L	OFF	L

Table 9. Diagnostic table (continued)

Operating Condition	Test Input TEST	Enable Input ENA	Control Input non-reg./reg. IN	Power Output/Current reg. Q	Status Output ST
Clock failure (clock loss) (1)	L	L	L	OFF	H
	L	L	H/PWM	OFF	H
	L	H	L	OFF	H
	L	H	H/PWM	OFF	L
Drift (2)	H	L	L	OFF	X
	H	L	H/PWM	OFF	X
Failure	H	H	H/PWM	ON	L
No failure	H	H	H/PWM	ON	H

1. During power on sequence only detected on channel 3 and 4 (see description).
2. This input combination is also used for an internal chip-test and must not be used.

4 Timing diagrams

4.1 Non regulated channels

Figure 5. Output slope, resistive load

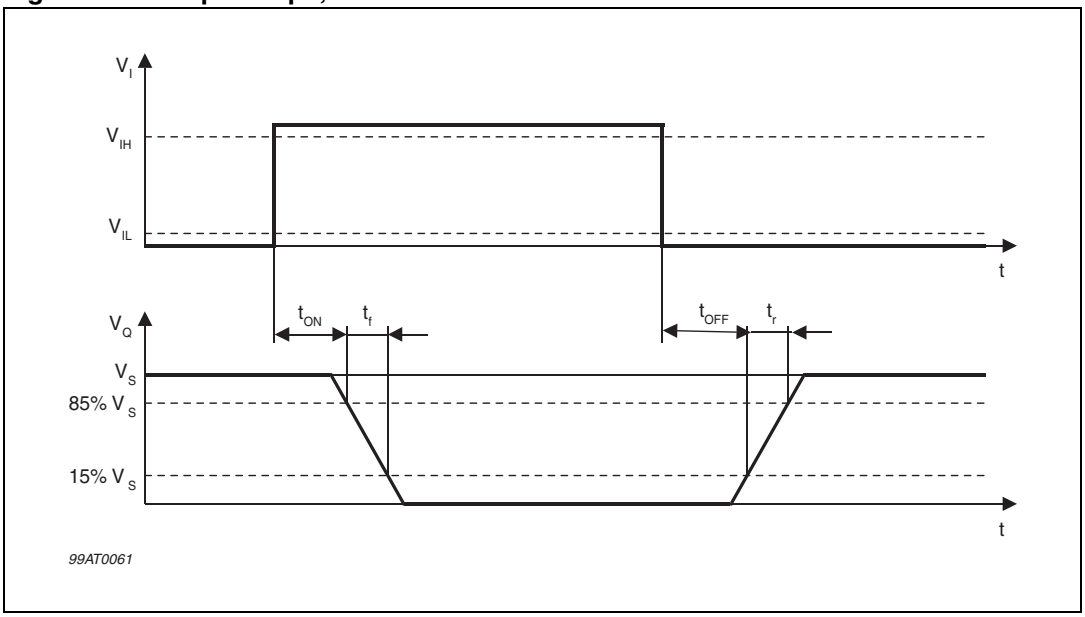


Figure 6. Overload switch OFF delay

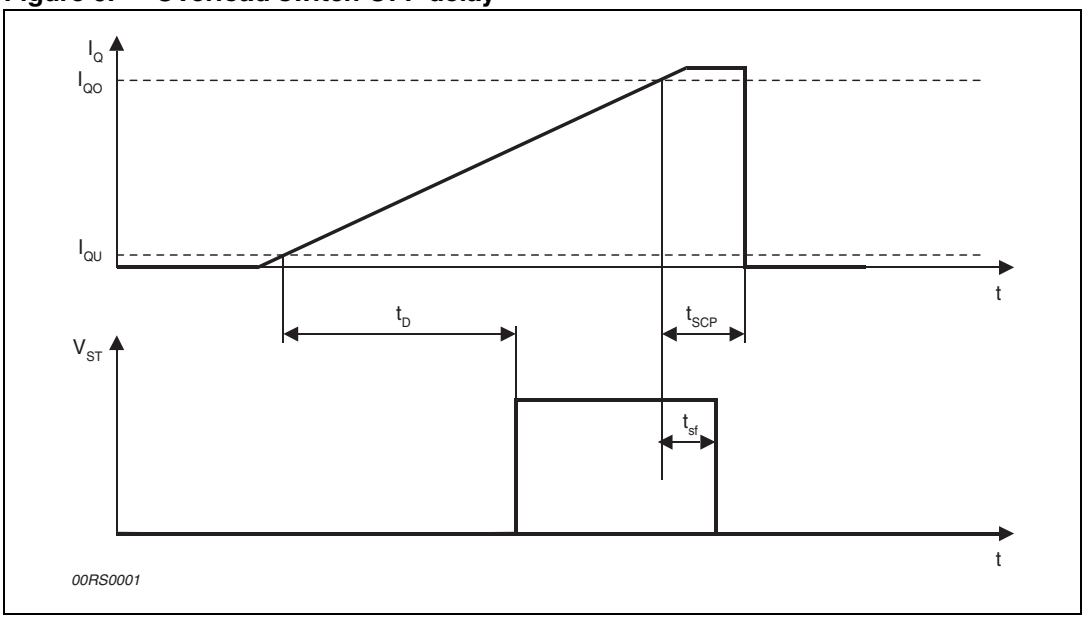


Figure 7. Normal condition, resistive load, pulsed input signal

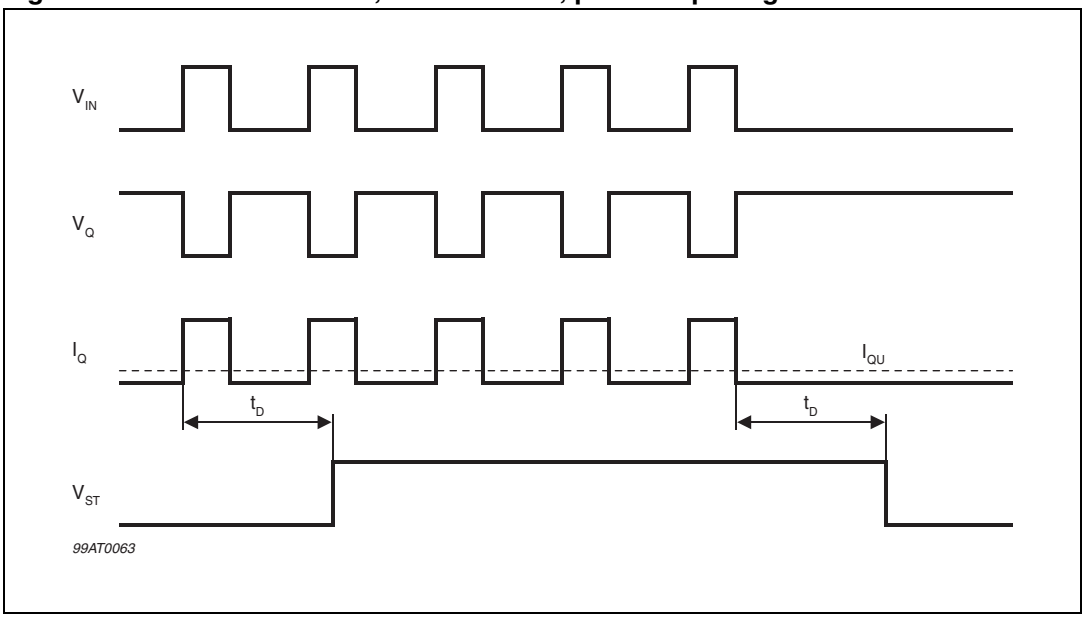


Figure 8. Current overload

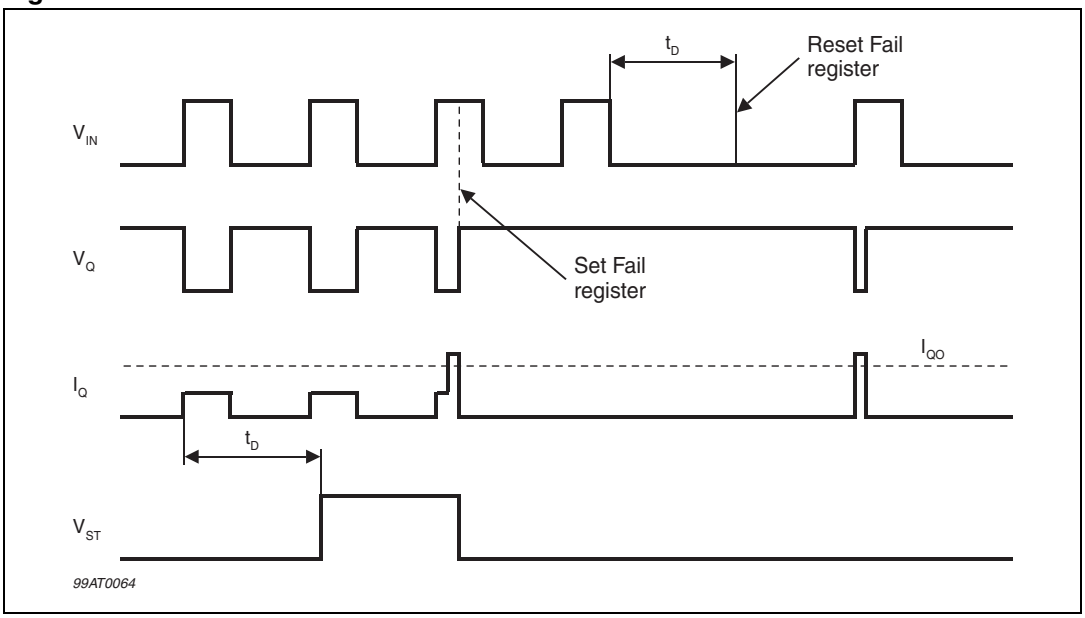


Figure 9 and *Figure 10* show diagnostic status output at different OPEN load current conditions followed by normal operation.

Figure 9. Under current condition

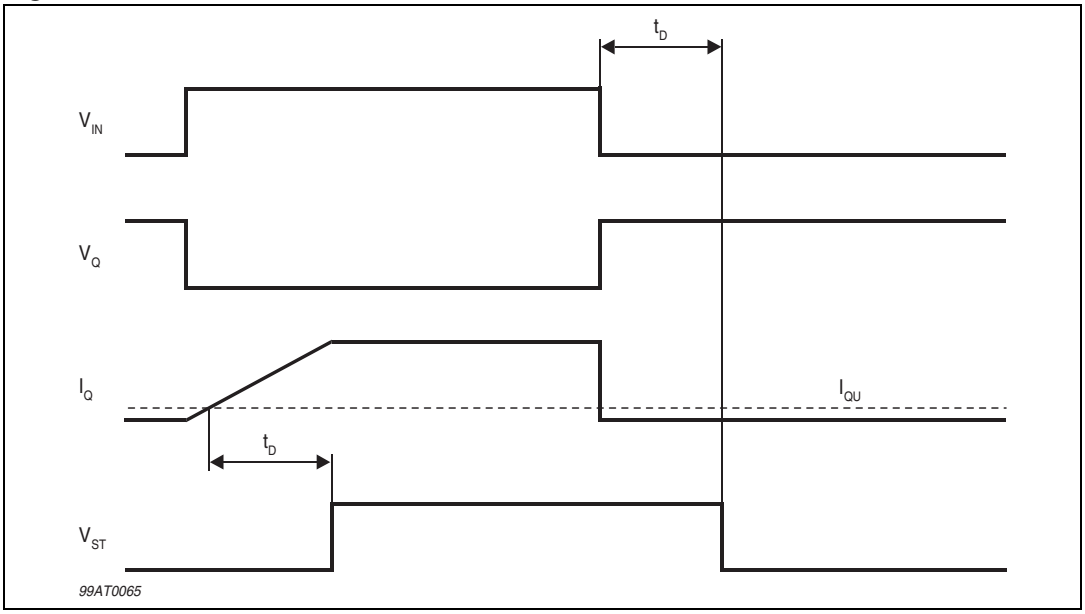


Figure 10. Open load condition in the case of pulsed input signal

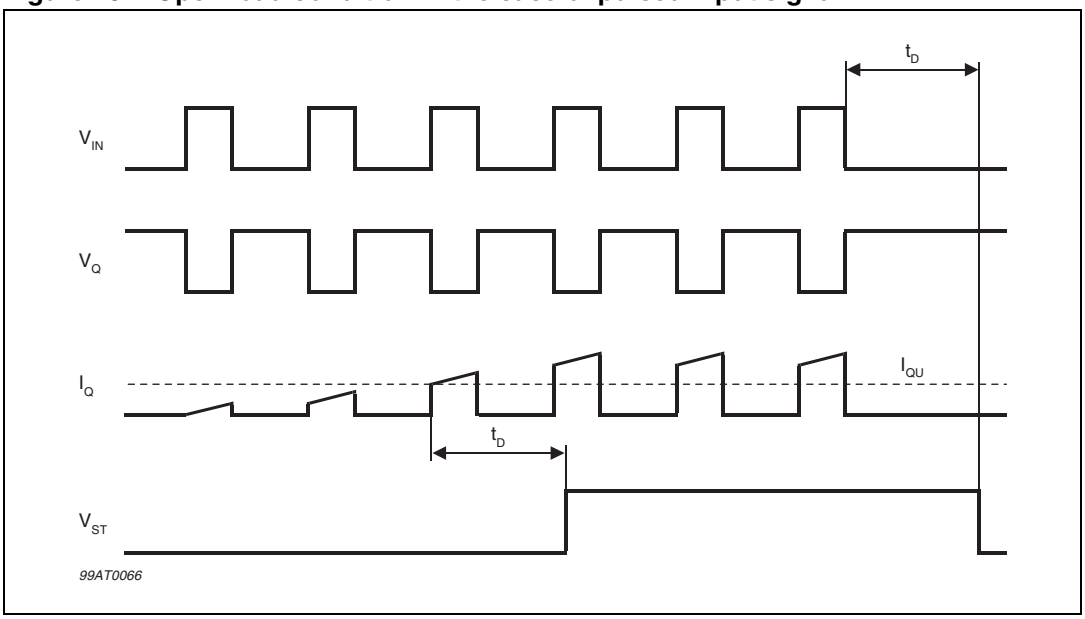
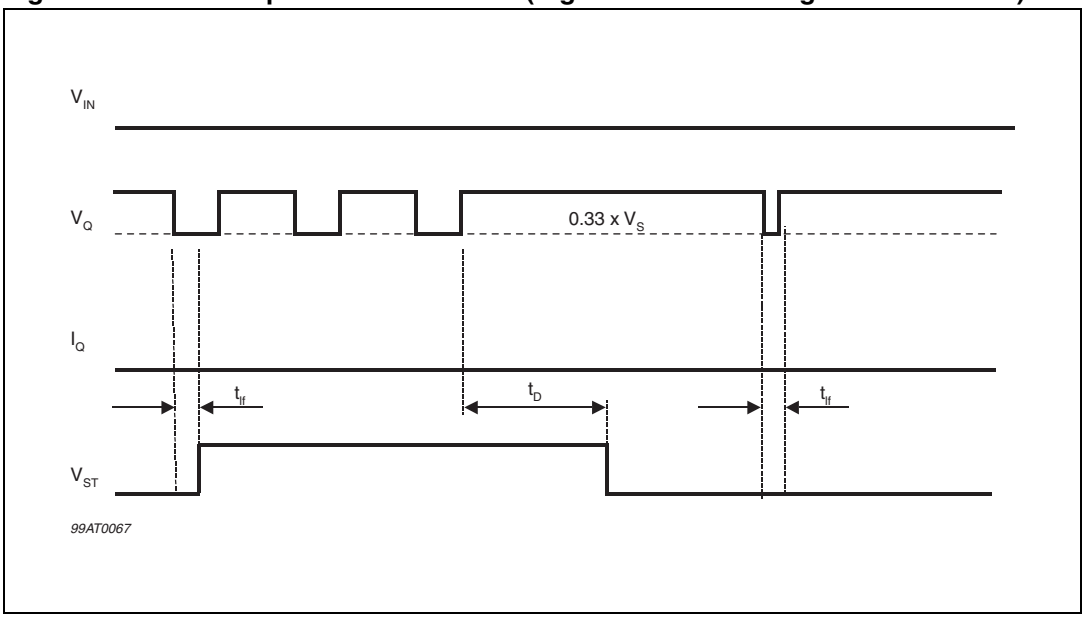


Figure 11. Pulsed open load conditions (regulated and non-regulated channels)



4.2 Regulated channels (timing diagrams of diagnostic with 2kHz PWM input signal)

Figure 12. Normal condition, inductive load

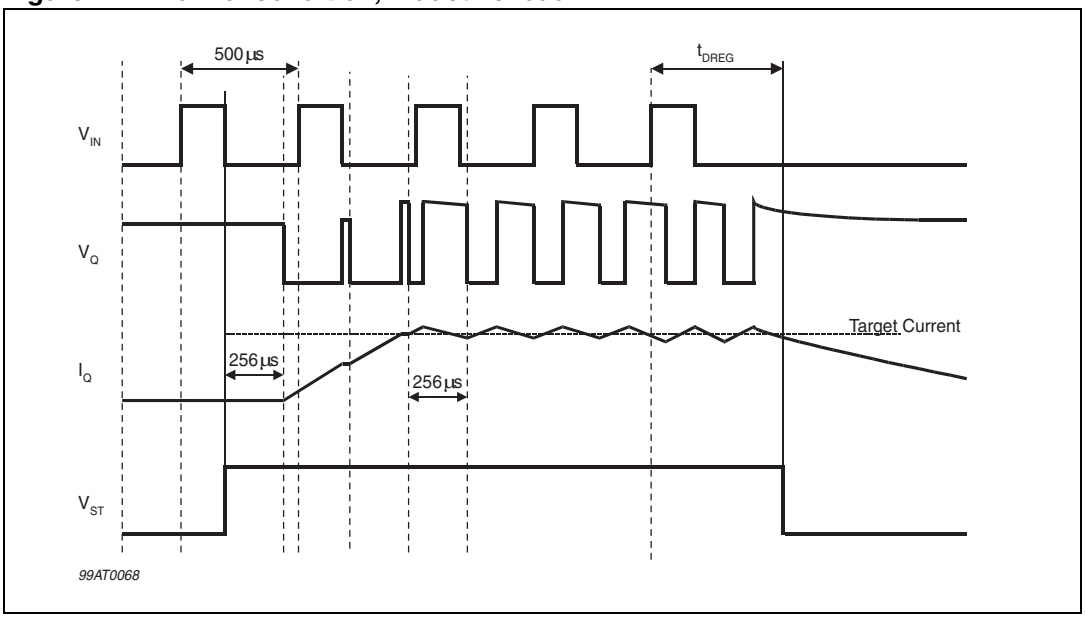


Figure 13. Current overload

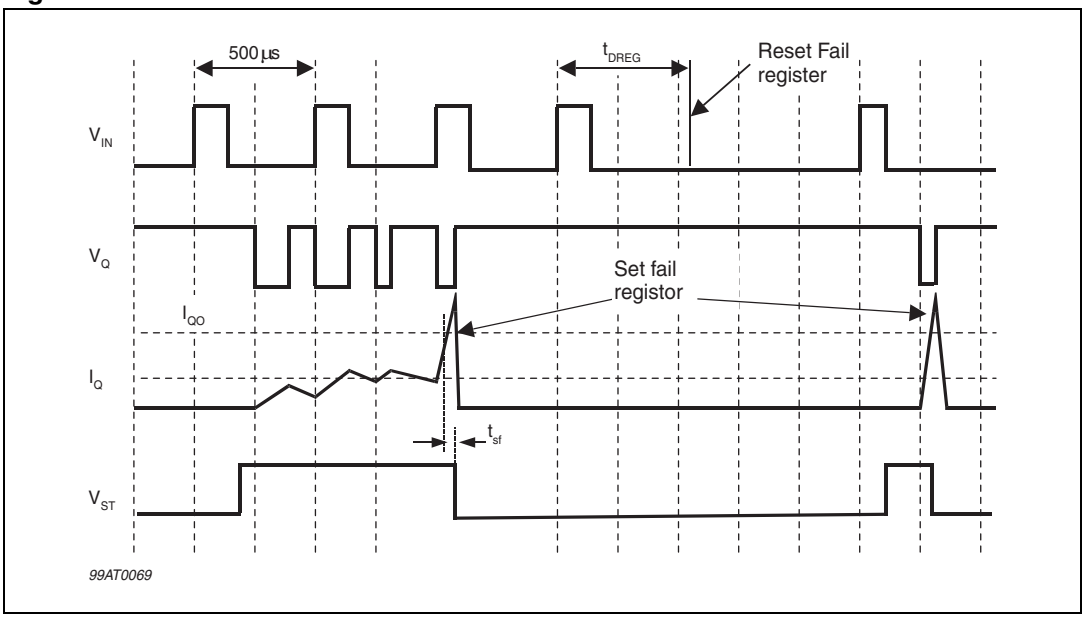


Figure 14. Recirculation error

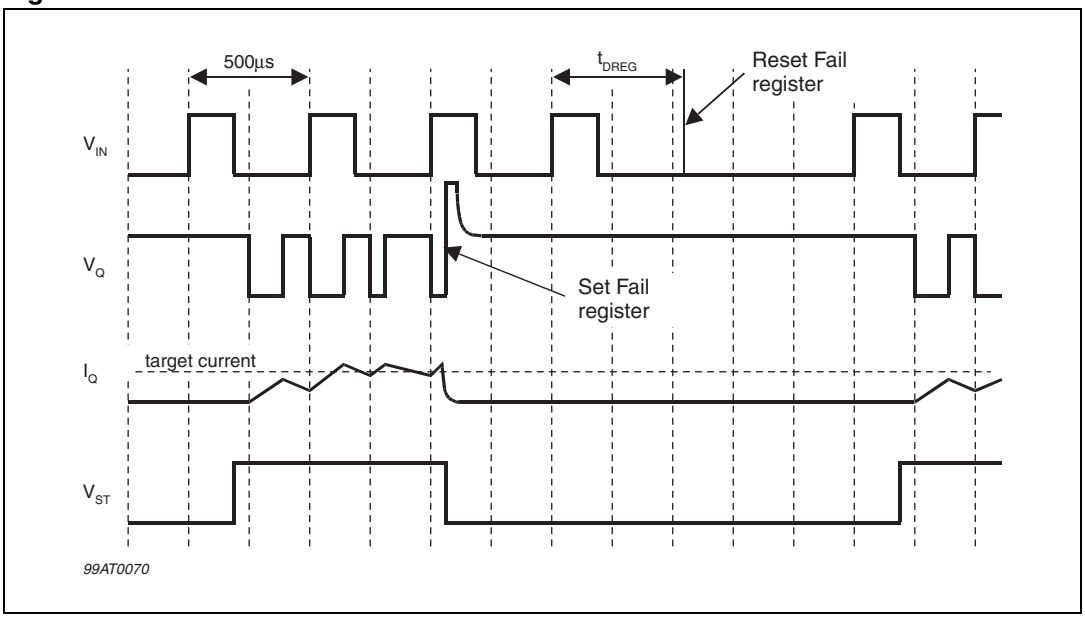


Figure 15. Current regulation error (e.g. as a result of voltage reduction)

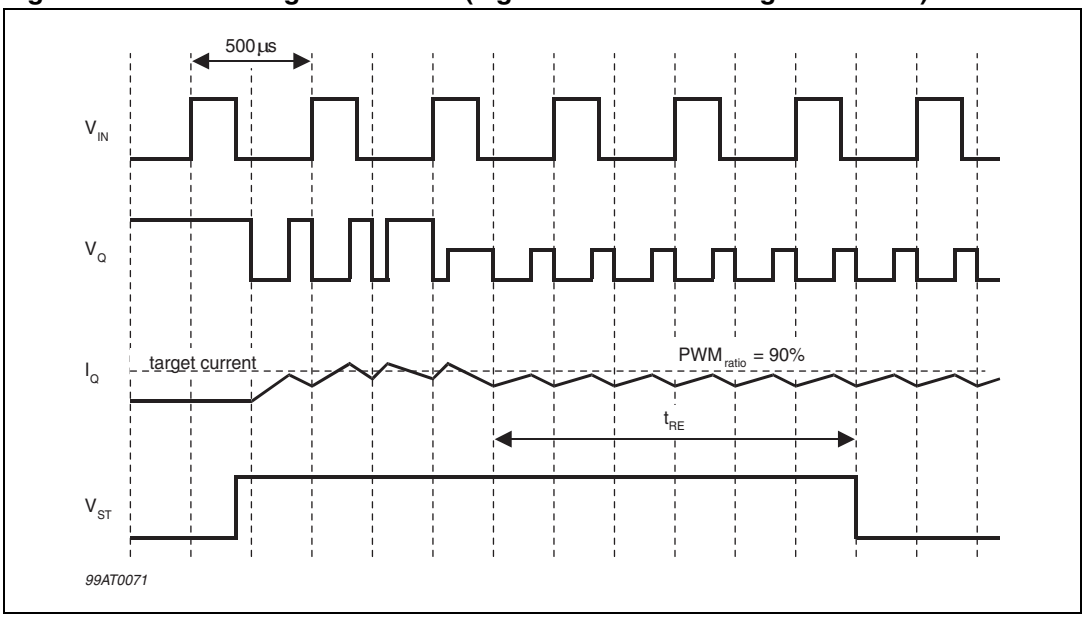


Figure 16. Over temperature

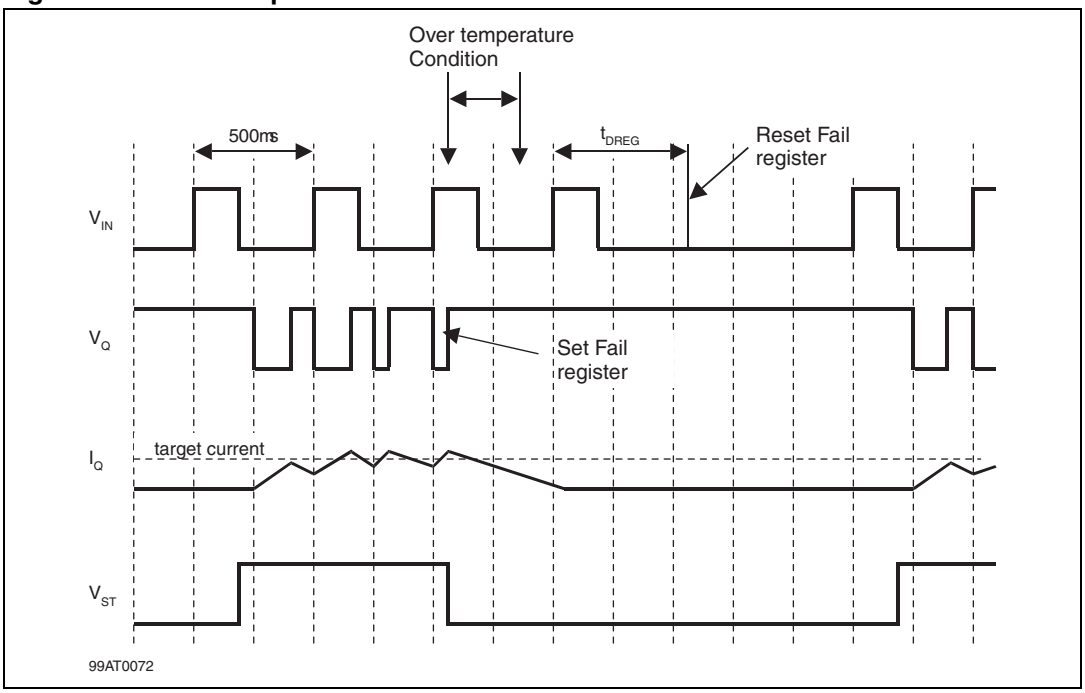
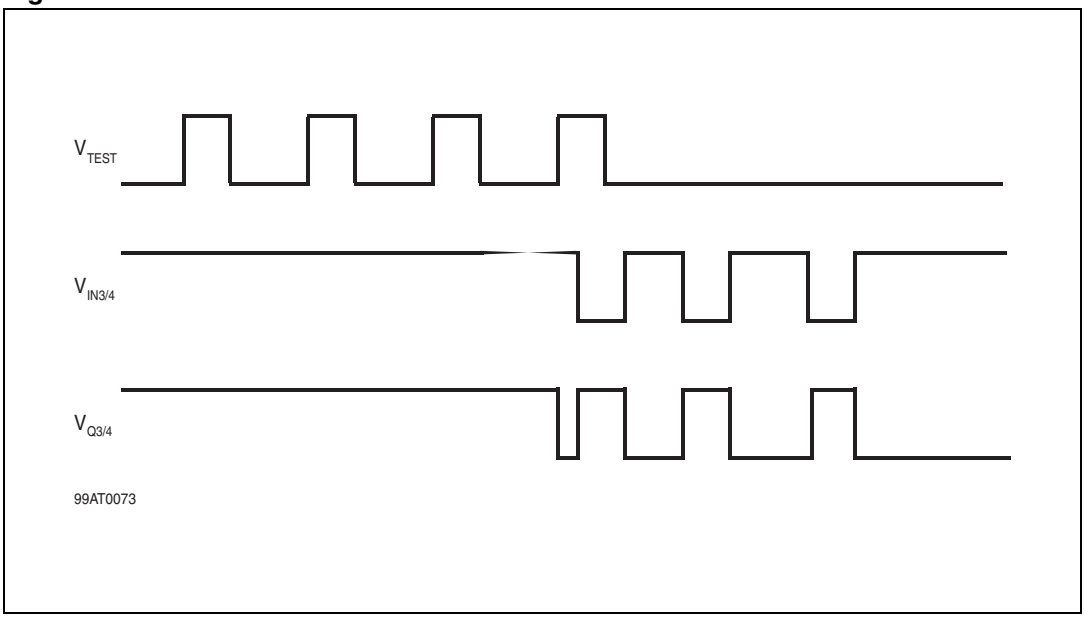


Figure 17. Test mode 4 VEN low



5 Package information

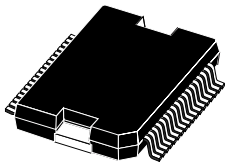
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 18. PowerSO-36 mechanical data and package dimensions

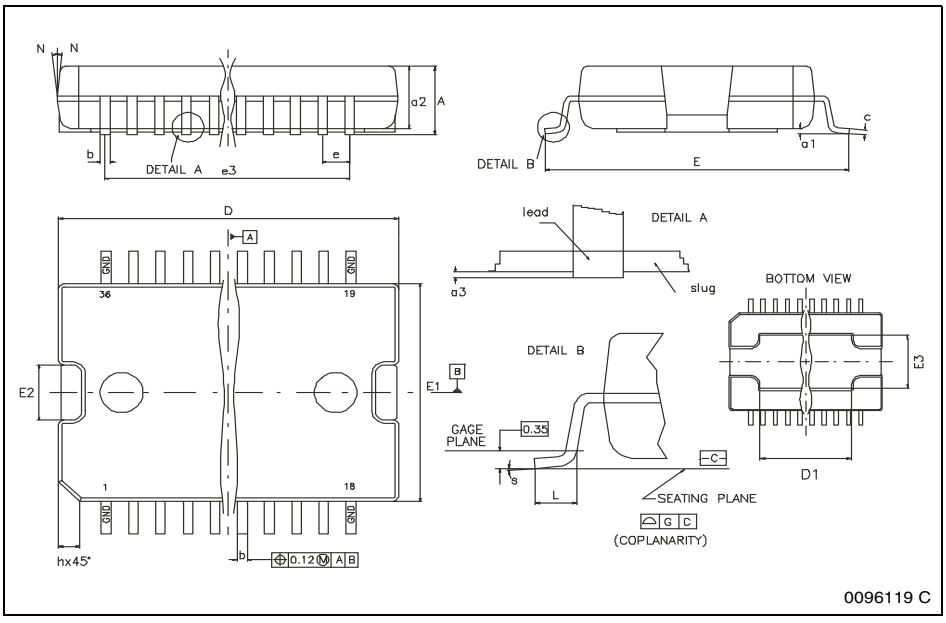
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10			0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.5	0.5472		0.5709
E1	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.80		6.20	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10			0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.8		1.10	0.0315		0.0433
N	10˚ (max)					
s	8˚ (max)					

Note: “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO-36



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
06-July-2002	1	Initial release.
02-May-2007	2	Package change, text modifications, corporate layout changes.
25-Sep-2013	3	Updated disclaimer.

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