PI2EQX5904

5.0Gbps 4-Lane PCIe® 2.0 ReDriver™ with Equalization & Emphasis

Features

➜ Up to 5.0Gbps PCIe® 2.0 Serial ReDriver™

➜ Supporting 8 differential channels or 4 lanes of PCIe Interface

➜ Pin strapped and I2C configuration controls (3.3V tolerant I^{2}C)

➜ Adjustable receiver equalization

➜ Adjustable transmitter amplitude and de-emphasis

➜ Variable input an output termination

➜ 1:2 channel broadcast

➜ Channel loop-back/Mux and Demux Mode

➜ Low Power: 660mW, Typical

➜ Electrical Idle fully supported

➜ Receiver detect and individual output control

➜ Single supply voltage, 1.2V ± 0.05V

➜ Power down modes

➜ Industrial Temp support, -40°C ~ +85°C

➜ Packaging: 100-contact LBGA, Pb-free & Green

Description

Pericom Semiconductor's PI2EQX5904 is a low power, PCIe® compliant signal ReDriver™. The device provides programmable equalization, amplification, and de-emphasis by using 8 select bits, to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

PI2EQX5904 supports eight 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or extends the signals across other distant data pathways on the user's platform. PI2EQX5904 compensates signal insertion loss at designated BER issued by PCIe2.0 endpoint device.

The integrated equalization circuitry provides flexibility with signal integrity of the PCIe signal before the ReDriver, whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the ReDriver.

In addition to providing signal re-conditioning, Pericom's PI2EQX5904 also provides power management Stand-by mode operated by a Power Down pin.
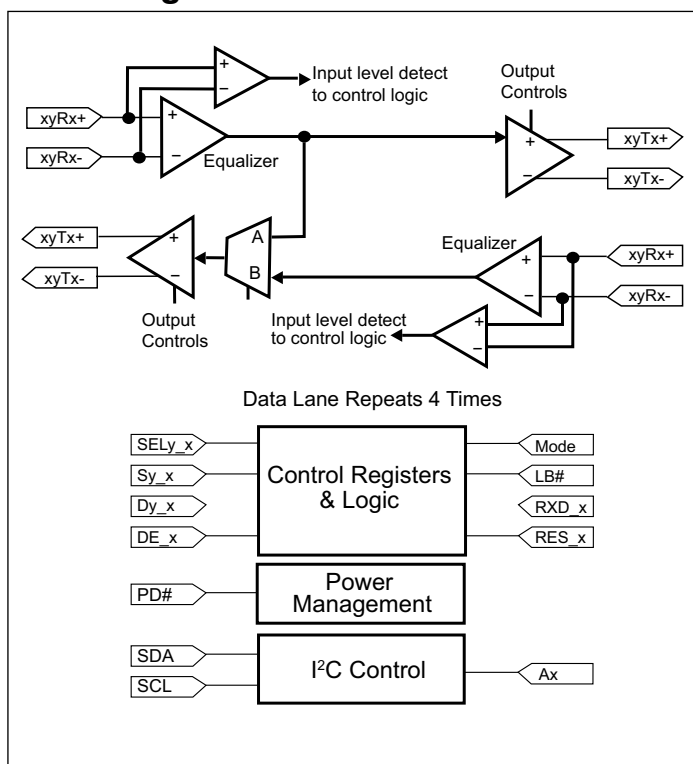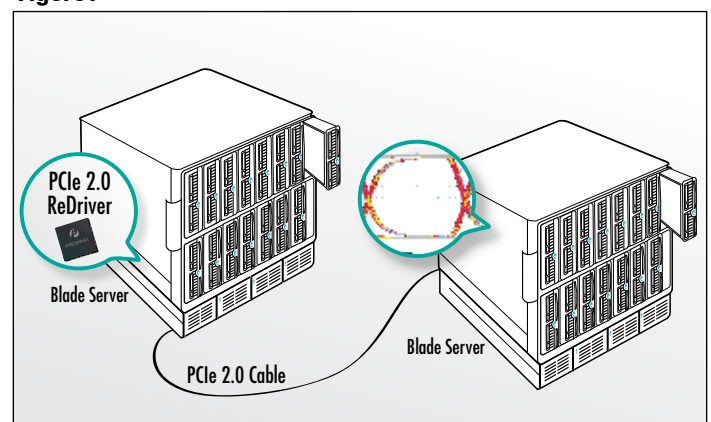
Block Diagram

Figure1

Pin Configuration (Top-Side View)

	1	2	3	4	5	6	7	8	9	10
A	VDD	B0TX-	B0TX+	VDD	SCL	SDA	VDD	B0RX+	B0RX-	VDD
B	A1RX+	GND	GND	A0RX-	DE_A	VDD	A0TX-	GND	GND	A1TX+
C	A1RX-	GND	GND	A0RX+	NC	PD#	A0TX+	GND	GND	A1TX-
D	VDD	B1TX+	B1TX-	VDD	D2_A	NC	VDD	B1RX-	B1RX+	VDD
E	SEL0_A	SEL1_A	SEL2_A	D0_A	D1_A	S0_A	RXD_A	S1_A	SIG_A	RX50_A
F	RX50_B	SIG_B	S1_B	RXD_B	S0_B	A1	SEL2_B	LB#	SEL1_B	SEL0_B
G	VDD	A2RX-	A2RX+	VDD	MODE	D0_B	VDD	A2TX+	A2TX-	VDD
H	B2TX+	GND	GND	B3TX-	DE_B	A0	B3RX-	GND	GND	B2RX+
J	B2TX-	GND	GND	B3TX+	RESET#	D1_B	B3RX+	GND	GND	B2RX-
K	VDD	A3RX+	A3RX-	VDD	D2_B	A4	VDD	A3TX-	A3TX+	VDD

Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
C4 B4	A0RX+, A0RX-	I I	CML inputs for Channel A0, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
C7 B7	A0TX+, A0TX-	O O	CML outputs for Channel A0, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
B1 C1	A1RX+, A1RX-	I I	CML inputs for Channel A1, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
B10 C10	A1TX+, A1TX-	O O	CML outputs for Channel A1, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
G3 G2	A2RX+, A2RX-	I I	CML inputs for Channel A2, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
G8 G9	A2TX+, A2TX-	O O	CML outputs for Channel A2, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
K2 K3	A3RX+, A3RX-	I I	CML inputs for Channel A3 with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
K9 K8	A3TX+, A3TX-	O O	CML outputs for Channel A3, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
A8 A9	B0RX+, B0RX-	I I	CML inputs for Channel B0, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
A3 A2	B0TX+, B0TX-	O O	CML outputs for Channel B0, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
D9 D8	B1RX+, B1RX-	I I	CML inputs for Channel B1, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
D2 D3	B1TX+, B1TX-	O O	CML outputs for Channel B1, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
H10 J10	B2RX+, B2RX-	I I	CML inputs for Channel B2, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
H1 J1	B2TX+, B2TX-	O O	CML outputs for Channel B2, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
J7 H7	B3RX+, B3RX-	I I	CML inputs for Channel B3, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
J4 H4	B3TX+, B3TX-	O O	CML outputs for Channel B3, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.

Pin Description (continued..)

Pin #	Pin Name	Type	Description
	Control Signals		
H6, F6, K6	A0, A1, A4	I	I^2C programmable address bit A0, A1 and A4.
E4, E5, D5	D[0:2]_A	I	Selection pins for Channel Ax emphasis (See emphasis Configuration Table) w/ 100K-Ohm internal pull up.
G6, J6, K5	D[0:2]_B	I	Selection pins for Channel Bx emphasis (See emphasis Configuration Table) w/ 100K-Ohm internal pull up.
B5	DE_A	I	De-emphasis enable input for Channel A0, A1, A2 and A3 with internal 100K-Ohm pull-up resistor. Set high selects output half bit de-emphasis and set low selects output full bit de-emphasis.
H5	DE_B	I	De-emphasis enable input for Channel B0, B1, B2 and B3 with internal 100K-Ohm pull-up resistor. Set high selects output half bit de-emphasis and set low selects output full bit de-emphasis.
F8	LB#	I	Input with internal 100K-Ohm pull-up resistor. LB# = High or open for normal operation. LB# = Low for loopback connection of A_RX to A_TX and B_TX.
G5	MODE	I	Input switch between pin control and I^2C control with internal 100k-ohm pull-up resistor. A LVCMOS high level selects input pin control, and disables I^2C operation. Note, during startup, input status of the control pin (LB#, RESET#, PD#, RXD_A/B, SEL0-2_A/B, D0-2_A/B, S0-1_A/B, DE_A/B) will be latched to the initial state of some I^2C control pins only once.
C6	PD#	I	Input with internal 100K-Ohm pull-up resistor, PD# =High or open is normal operation, PD# =Low disable the IC, and set IC to power down mode, both input and output go Hi-Z.
D6	NC		No Connect
C5	NC		No Connect
J5	RESET#	I	RESET# is an active low channel reset input for Channel A0, B0, A1, B1, A2, B2, A3 and B3 with internal 100K-Ohm pull-up resistor. When low, the receiver detection cycle is reset, and normal detection cycle is started after the pin goes high.
E10	RX50_A	O	Receiver detect output pin for Channel A0. RX50_A=High indicates that a 50-Ohm termination was sensed at the A0TX+/- outputs.
F1	RX50_B	O	Receiver detect output pin for Channel B0. RX50_B=High indicates that a 50-Ohm termination was sensed at the B0TX+/- outputs.
E7	RXD_A	I	Receiver detect enable input for Channel A0, A1, A2 and A3 with internal 100K-Ohm pull-up resistor.
F4	RXD_B	I	Receiver detect enable input for Channel B0, B1, B2 and B3 with internal 100K-Ohm pull-up resistor.
E6, E8	S[0:1]_A	I	Selection pins for Channel Ax output level (see Output Swing Configuration Table) w/ 100K-Ohm internal pull up.
F5, F3	S[0:1]_B	I	Selection pins for Channel Bx output level (see Output Swing Configuration Table) w/ 100K-Ohm internal pull up.
A5	SCL	I/O	I^2C SCL clock input.
A6	SDA	I/O	I^2C SDA data input.

Pin Description (continued..)

Pin #	Pin Name	Type	Description
E1, E2, E3	SEL[0:2]_A	I	Selection pins for Channel Ax equalization (see Equalizer Configuration Table) w/ 100K-Ohm internal pull up
F10, F9, F7	SEL[0:2]_B	I	Selection pins for Channel Bx Equalization (see Equalizer Configuration Table) w/ 100K-Ohm internal pull up
E9	SIG_A	O	Signal detect output pin for Channel A0. SIG_A=High represents a input signal > threshold at the differential inputs.
F2	SIG_B	O	Signal detect output pin for Channel B0. SIG_B=High represents a input signal > threshold at the differential inputs.
Power Pins			
B2, B3, B8, B9, C2, C3, C8, C9, H2, H3, H8, H9, J2, J3, J8, J9	GND	PWR	Supply Ground
A1, A4, A7, A10, B6, D1, D4, D7, D10, G1, G4, G7, G10, K1, K4, K7, K10	V_{DD}	PWR	1.2V Supply Voltage

DESCRIPTION of OPERATION

Configuration Modes

Device configuration can be performed in two ways depending on the state of the MODE input. MODE determines whether IC configuration status is from the input pins or via I2C control. When MODE is set high, the configuration input pins set the configuration operating state as stored in configuration registers. While MODE is set high, changes to these control registers are disabled and the initial condition is protected from any changes to insuring a known operating state. When the MODE pin is low, reprogramming of these control registers via I2C is allowed. Note that the MODE pin is not latched, and is always active to enable or disable I2C access.

During initial power-on, the value at the configuration input pins: LB#, RESET#, PD#, RXD_A and RXD_B, DE_A, DE_B, SEL0_A, SEL1_A, SEL2_A, D0_A, D1_A, D2_A, S0_A, S1_A, SEL0_B, SEL1_B, SEL2_B, D0_B, D1_B, D2_B, S0_B, S1_B, will be latched to the configuration registers as initial startup states.

Equalizer Configuration

The PI2EQX5904 input equalizer compensates for signal attenuation and Inter-Symbol Interference (ISI) resulting from long signal traces or cables, vias, signal crosstalk and other factors, by boosting the gain of high-frequency signal components. Because either too little, or too much, signal compensation may be non-optimal eight levels are provided to adjust for any application.

Equalizer configuration is performed in two ways determined by the state of the MODE pin. When the device first powers up, the SELx_[A:B] input pins are read into the appropriate control registers to set the equalization characteristic. If the MODE pin is low, reprogramming of these control registers via I^2C is allowed.

Each group of four channels, A and B, has separate equalization control, and all four channels within the group are assigned the same configuration state. The Equalizer Selection table below describes pin strapping options and associated operation of the equalizer. Refer to the section on I^2C programming for information on software configuration of the equalizer.

Equalizer Selection

SEL2_[A:B]	SEL1_[A:B]	SEL0_[A:B]	@1.25GHz	@2.5GHz
0	0	0	0.5dB	1.2dB
0	0	1	0.6dB	1.5dB
0	1	0	1.0dB	2.6dB
0	1	1	1.9dB	4.3dB
1	0	0	2.8dB	5.8dB
1	0	1	3.6dB	7.1dB
1	1	0	5.0dB	9.0dB
1	1	1	7.7dB	12.3dB

Output Configuration

The PI2EQX5904 provides flexible output strength and emphasis controls to provide the optimum signal to pre-compensate for losses across long trace or noisy environments so that the receiver gets a clean eye opening. Control of output configuration is grouped for the A and B channels, so that each channel within the group has the same setting.

Output configuration is performed in two ways depending on the state of the MODE pin. When the device first powers up, the Sx_[A:B], and Dx_[A:B] input pins are read into the appropriate control registers to set the power-on state. If the MODE pin is low, reprogramming of these control registers via I2C is allowed.

The Output Swing Control table shows available configuration settings for output level control, as specified using the Sx_y pins and registers.

Output Swing Control

S1_[A:B]	S0_[A:B]	Swing (Diff. VPP)
0	0	1.1V
0	1	0.5V
1	0	0.8V
1	1	1.0V

Output De-Emphasis Adjustment

De-emphasis settings are determined by the state of the DEx_y input pins and configuration registers, as shown in the Output De-emphasis table below. Half-bit-de-emphasis is selected as the default power-on mode, but can be changed to full-bit-de-emphasis via reprogramming the Loopback and De-emphasis Control register using the I^2C interface. Output de-emphasis settings are indpendant of the data rate.
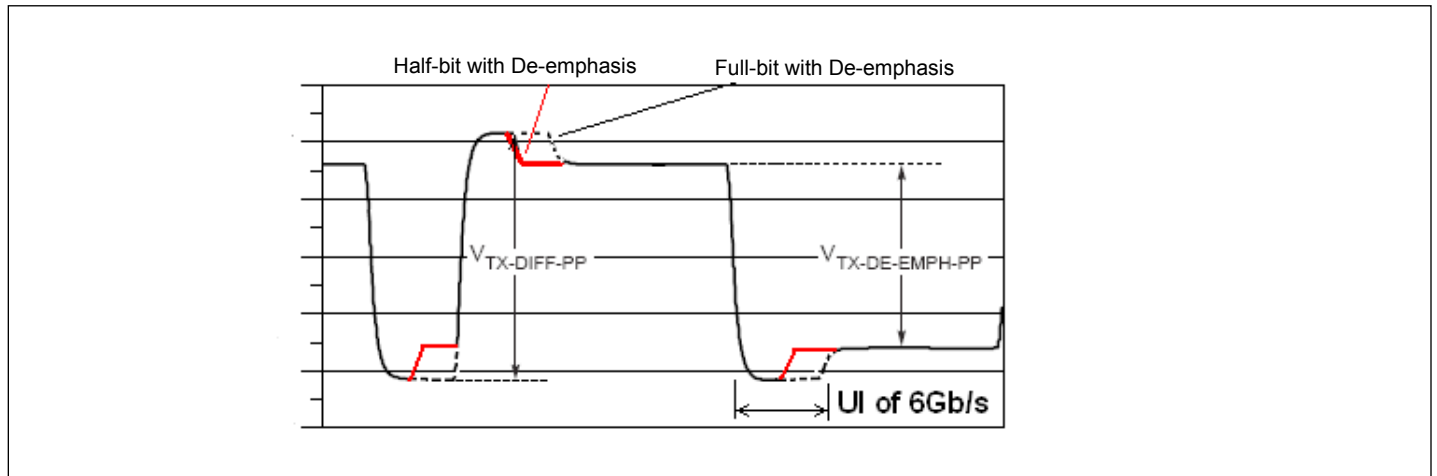
Output De-emphasis Adjustment

D2_[A:B]	D1_[A:B]	D0_[A:B]	De-emphasis
0	0	0	0dB
0	0	1	-2.5dB
0	1	0	-3.5dB
0	1	1	-4.5dB
1	0	0	-5.5dB
1	0	1	-6.5dB
1	1	0	-7.5dB
1	1	1	-8.5dB

Input Level Detect

An input level detect and output squelch function is provided on each channel to eliminate re-transmission of input noise. A continuous signal level below the Vth- threshold causes the output driver to go to a high-impedance state, so that both the positive and negative output signal are pulled to VDD by the internal pull-up resistors. This feature supports the L0s PCI Express Electrical Idle state.

Receiver Detect

Automatic Receiver Detection is a feature that can set the number of active channels. By sensing the presence of a load device on the output, the channel can be automatically enabled for operation. This allows the PI2EQX5904 to configure itself properly depending on the devices it is communicating with, whether it is a 4-lane, 3-lane, 2-lane or just 1-lane device or adapter card.

Receiver Detect is enabled by the RXD_A, or RXD_B pins, or alternatively via I2C programming. When RXD_A or RXD_B is set to low, then the Receiver Detect operation for that group of channel is disabled, and those channels go directly to 50-Ohm input termination to ground and 50-Ohm output termination to VDD (for a valid differential channel input level) or to 2K-Ohm (if the signal level is less than the threshold level).

(Continued)

The RESET# input is used to reset the receiver detect state machine to its initial state. The start of the receiver detect cycle starts when RESET# transitions from low to high.
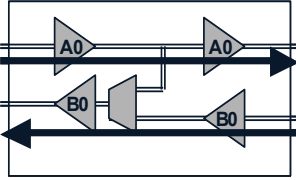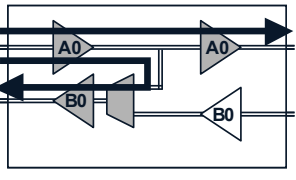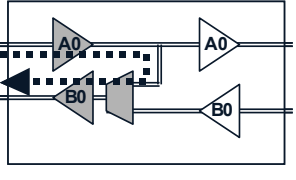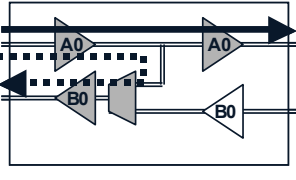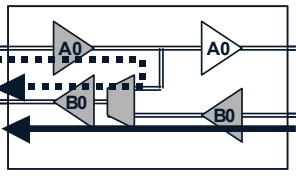
When a Receiver Detect cycle is begins the differential channel pins are enabled with a 2K-Ohm pullup to VDD. A 50-Ohm Receiver termination will change the pin level. This pin level is evaluated after a fixed time-out, and the channel is then set into the proper operating state. The output signals RX50_A and RX50_B represent the receiver detect result for their specific channels.

The I/O Operation table summaries the relationships and operation of receiver detect and other signals involved with I/O control.

Table 4 - I/O Operation Control

Control Inputs			Detection States		Data Channel I/O		
PD#	RXD_x	RESET#	RX50	SIG_x	Input Termination	Output Termination	Mode
0	X	X	X	X	Hi-Z	Hi-Z	Full IC power down, all channels disabled
1	0	0	X	X	Hi-Z	2K-Ohm pull-up	Channel disabled, output pulls to V_{DD}. Receiver detect reset
1	0	1	X	0	50-Ohm pull-down	2K-Ohm pull-up	Channel enabled, no input signal, output pulls to V_{DD}. Receiver detect disabled
1	0	1	X	1	50-Ohm pull-down	50-Ohm pull-up	Channel enabled, valid input signal detected, output driving. Receiver detect disabled.
1	1	0	X	X	Hi-Z	2K-Ohm pull-up	Channel disabled. Receiver detect reset.
1	1	1	0	X	Hi-Z	2K-Ohm pull-up	Channel disabled, output pulls to V_{DD}. Receiver detect enabled, no receiver detected.
1	1	1	1	0	50-Ohm pull-down	2K-Ohm pull-up	Channel inactive, output pulls to V_{DD}. Receiver detect enabled, receiver detected. No input signal
1	1	1	1	1	50-Ohm pull-down	50-Ohm pull-up	Channel active, valid input signal detected, output driving. Receiver detect enabled, load detected.

Loopback Operation

Loopback Modes		CONDITIONS
	NORMAL MODE A0Rx to A0Tx, B0Rx to B0Tx	LB_A0B0# = 1 INDIS_A0 = 0 OUTDIS_A0 = 0 INDIS_B0 = 0 OUTDIS_B0 = 0
	BROADCAST MODE A0Rx to A0Tx and B0Tx	LB_A0B0# = 0 INDIS_A0 =0 INDIS_B0 = 1 OUTDIS_B0 = 0
	LOOPBACK MODE A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUT_DIS_A0 = 1 INDIS_B0 = 1 OUTDIS_B0 = 0
	DEMUX MODE Solid Line A0Rx to A0Tx	LB_A0B0# = 1 INDIS_A0 = 0 OUTDIS_A0 = 0 INDIS_B0 = 1 OUTDIS_B0 = 0
	DEMUX MODE Dashed Line A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUTDIS_A0 = 0 INDIS_B0 = 1 OUTDIS_B0 = 0
	MUX MODE Solid Line B0Rx to B0Tx	LB_A0B0# = 1 INDIS_A0 = 0 OUTDIS_A0 = 1 INDIS_B0 = 0 OUTDIS_B0 = 0
	MUX MODE Dasked Line A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUTDIS_A0 = 1 INDIS_B0 = 0 OUTDIS_B0 = 0

Each lane provides a loopback mode for test purposes which is controlled by a strapping pin and I^{2}C register bit. The LB# pin controls all lanes together. When this pin is high normal data mode is enabled. When LB# is low the loopfeature mode is enabled. The adjacent figure diagrams this operation. Loopback is not intended to be dynamically switched, and the normal system application is to initialize to one configuration or the other.

The Loopback mode can also support mux/demux operation. Using I^{2}C configuration, unused inputs and outputs can be disabled to minimize power and noise.

I²C Operation

The integrated I2C interface operates as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode. The data byte format is 8 bit bytes. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred. Address bits A4, A1 and A0 are programmable to support multiple chips environment. The data is loaded until a Stop sequence is issued.

Configuration Register Summary

Byte	Mnemonic	Function
0	SIG	Signal Detect, indicates valid input signal level
1	RX50	Receiver Detect Output, indicates whether a receiver load was detected
2	LBEC	Loopback and Emphasis Control, provides for control of the loopback function and emphasis mode (pre-emphasis or de-emphasis)
3	INDIS	Channel Input Disable, controls whether s channels input buffer is enabled or disabled
4	OUTDIS	Channel Output Disable: Controls whether a channels output buffer is enabled or disabled
5	RESET	Channel Reset
6	PWR	Power Down Control, enables power down for each channel individually
7	RXDE	Receiver Detect Enable, controls the receiver detect operation
8	AEOC	A-Channels Equalizer and Output Control
9	AEOC	B-Channels Equalizer and Output Control
10	RSVD	Reserved
11	VTH	Idle detect threshold control

Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I2C Data Transfer diagram). The PI2EQX5904 will never hold the clock line SCL LOW to force the master into a wait state.

Note: Byte-write and byte-read transfers have a fixed offset of 0x00, because of the very small number of configuration bytes. An offset byte presented by a host to the PI2EQX5904 is not used.

Addressing

Up to eight PI2EQX5904 devices can be connected to a single I2C bus. The PI2EQX5904 supports 7-bit addressing, with the LSB indicating either a read or write operation. The address for a specific device is determined by the A0, A1 and A4 input pins.

Address Assignment							
A6	A5	A4	A3	A2	A1	A0	R/W
1	1	Program	0	0	Programmable		1=R, 0=W

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the PI2EQX5904 will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. The PI2EQX5904 will generate an acknowledge after each byte has been received.

Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the PI2EQX5904 will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. For a write cycle, the first data byte following the address byte is a dummy or fill byte that is not used by the PI2EQX5904. This byte is provided to provided compatibility with systems implementing 10-bit addressing. Data is transferred with the most significant bit (MSB) first. After each block write, address pointer will reset to byte 0.

Register Description

Byte 0 - Signal Detect (SIG)

SIG_xy=0=low input signal, SIG_xy=1=valid input signal

Bit	7	6	5	4	3	2	1	0
Name	**SIG_A0**	**SIG_B0**	**SIG_A1**	**SIG_B1**	**SIG_A2**	**SIG_B2**	**SIG_A3**	**SIG_B3**
Type	R	R	R	R	R	R	R	R
Power-on State	X	X	X	X	X	X	X	X

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Signal Detect register provides information on the instantaneous status of the channel input from the Input Level Threshold Detect circuit. If the input level falls below the Vth- level the relevant SIG_xy bit will be 0, indicating a low-level noise or electrical idle input, resulting in the outputs going to the high-impedance off state or squelch mode. If the input level is above Vth-, then SIG_xy is 1, indicating a valid input signal, and active signal recovery operation.

Byte 1 - Receiver Detect Output Register (RX50)

Bit	7	6	5	4	3	2	1	0
Name	**RX50_A0**	**RX50_B0**	**RX50_A1**	**RX50_B1**	**RX50_A2**	**RX50_B2**	**RX50_A3**	**RX50_B3**
Type	R	R	R	R	R	R	R	R
Power-on State	X	X	X	X	X	X	X	X

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The RX50_xy bits report the result of a receiver detection cycle. One bit is assigned for each channel of the device. RX50_xy is at a logic 1 level indicating a load and receiver was detected. When RX50_xy is 0 then a load device was not detected. The RX50 register is read-only, and is undefined after power-up until a Receiver Detection cycle completes.

Byte 2 - Loopback and Emphasis Control Register (LBEC)

LB_xyxy#=0=loopback mode, LB_xyxy#=1=normal mode, DE_x=0=Full Bit de-emphasis, DE_x=1= Half Bit de-emphasis

Bit	7	6	5	4	3	2	1	0
Name	LB_A0B0#	LB_A1B1#	LB_A2B2#	LB_A3B3#	DE_A	DE_B	rsvd	rsvd
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Power-on State	LB#	LB#	LB#	LB#	DE_A	DE_B	X	X

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

Individual control for each lane is provided for the loopback function via this register.

BYTE 3 - Channel Input Disable (INDIS)

INDIS_xy=0=enable input, INDIS_xy=1=disable input

Bit	7	6	5	4	3	2	1	0
Name	INDIS_A0	INDIS_B0	INDIS_A1	INDIS_B1	INDIS_A2	INDIS_B2	INDIS_A3	INDIS_B3
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	0	0	0	0	0	0	0	0

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Input Disable register, provides control over the input buffer of each channel independently. When and INDIS_xy bit is logic 1, then the input buffer is switched off and the input termination is high impedance. This feature can be used for PCB testing, and when only one input is used during Loopback as a demux function. When INDIS_xy is at a logic 0 state then the input buffer is enabled (normal operating mode).

BYTE 4 - Channel Output Disable (OUTDIS)

ODIS_xy=0=enable output, ODIS_xy=1=disable output

Bit	7	6	5	4	3	2	1	0
Name	ODIS_A0	ODIS_B0	ODIS_A1	ODIS_B1	ODIS_A2	ODIS_B2	ODIS_A3	ODIS_B3
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	0	0	0	0	0	0	0	0

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Output Disable register, allows control over the output buffer of each channel independently. When and OUTDIS_xy bit is logic 1, then the output buffer is switched off and the termination is high impedance. This feature can be used for PCB testing, and when only one output is used during Loopback as a mux function. When INDIS_xy is at a logic 0 state then the input buffer is enabled (normal operating mode).

BYTE 5 - Channel Reset (RESET)

RES_xy# =0=reset, RES_xy# =1=normal operation. Latch from RESET# input at startup

Bit	7	6	5	4	3	2	1	0
Name	RES_A0#	RES_B0#	RES_A1#	RES_B1#	RES_A2#	RES_B2#	RES_A3#	RES_B3#
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Reset register allows for restart of an individual channels Receiver Detect function. A transition from 0 to 1 initiates a new Receiver Detect cycle (if the channel is enabled and receiver detect is enabled). While static at 0 or 1, the RES_zy# bit will have no effect on operation. The Channel Reset bits are read/write allowing the current state to be checked.

BYTE 6 - Power Down Control (PWR)

PD_xy# =0=channel off/power down, PD_xy# =1=normal operation, Latch from PD# input at startup

Bit	7	6	5	4	3	2	1	0
Name	PD_A0#	PD_B0#	PD_A1#	PD_B1#	PD_A2#	PD_B2#	PD_A3#	PD_B3#
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	PD#	PD#	PD#	PD#	PD#	PD#	PD#	PD#

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Power Down Control register allows for individual control over each channel for power savings. When PD_xy# is logic 0 the channel is turned off. When PD_xy# is 1 then the channel is enabled for normal operation.

BYTE 7 - Receiver Detect Enable (RXD)

RXD_xy =0=channel off/power down, RXD_xy =1=normal operation, Latch from PD# input at startup

Bit	7	6	5	4	3	2	1	0
Name	RXD_A0	RXD_B0	RXD_A1	RXD_B1	RXD_A2	RXD_B2	RXD_A3	RXD_B3
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	RXD_A	RXD_B	RXD_A	RXD_B	RXD_A	RXD_B	RXD_A	RXD_B

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Receiver Detect Enable register allows for control of the receiver detect state machine for each individual channel. When RXD_xy is set to 0, then the receiver detect function is disabled. When RXD_xy is logic 1, then the receiver detect state machine is enabled for operation.   The initial state of the register bits are determined by the RXD_A and RXD_B input pins during power-up.

BYTE 8 - A-Channels Equalizer and Output Control (AEOC)

SELx_A: Equalizer configuration, Dx_A: Emphasis control, Sx_A: Output level control (see Configuration Table)

Bit	7	6	5	4	3	2	1	0
Name	SEL0_A	SEL1_A	SEL2_A	D0_A	D1_A	D2_A	S0_A	S1_A
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	SEL0_A	SEL1_A	SEL2_A	D0_A	D1_A	D2_A	S0_A	S1_A

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The A-Channels Equalizer and Output Control register is used to control the configuration of the input equalizer and output emphasis and levels of the four A channels. These register bits are loaded from the input configuration pins of the same name at power-on. These bits may be changed if the MODE# input is set to allow I2C configuration. Please refer to the tables (1) Equalizer Configuration, (2) Output Swing Configuration and

(3) Output Emphasis Configuration earlier in this document for setting information. All four A channels get the same configuration settings.

BYTE 9 - B-Channels Equalizer and Output Control (BEOC)

SELx_B: Equalizer configuration,
Dx_B: Emphasis control,

Sx_B: Output level control (see Configuration Table)

Bit	7	6	5	4	3	2	1	0
Name	SEL0_B	SEL1_B	SEL2_B	D0_B	D1_B	D2_B	S0_B	S1_B
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	SEL0_B	SEL1_B	SEL2_B	D0_B	D1_B	D2_B	S0_B	S1_B

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The B-Channels Equalizer and Output Control register is used to control the configuration of the input equalizer and output emphasis and levels of the four B channels. These register bits are loaded from the input configuration pins of the same name at power-on. These bits may be changed if the MODE# input is set to allow I2C configuration. Please refer to the tables (1) Equalizer Configuration, (2) Output Swing Configuration and (3) Output Emphasis Configuration earlier in this document for setting information. All four B channels get the same configuration settings.

BYTE 10 - Reserved

Reserved Byte 10 is also visible via the I2C interface. This byte is R/W, is initialized to 0 at power up, is used for IC manufacturing test purposes and should not be changed for normal operation.

## BYTE 11 - Idle Detect Threshold Control

Bit	7	6	5	4	3	2	1	0
Name	VTH7	VTH6	VTH5	VTH4	VTH3	VTH2	VTH1	VTH0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	1	1	1	0	1	1	1	1

Note:

1. R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

2. 0 = enable

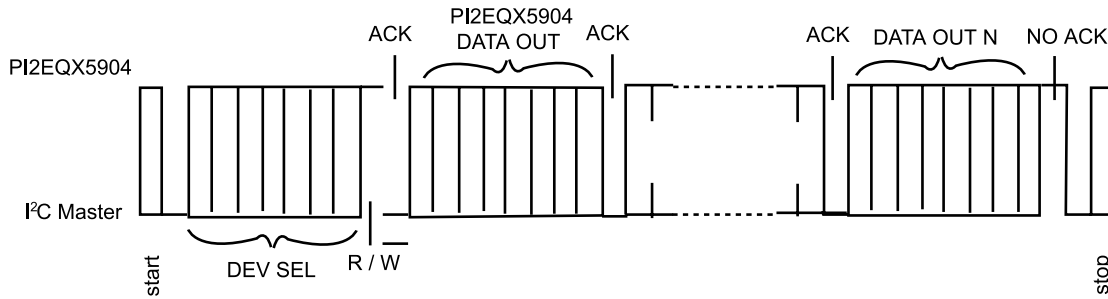3. Only 1 bit can be enabled at a time

Start & Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.
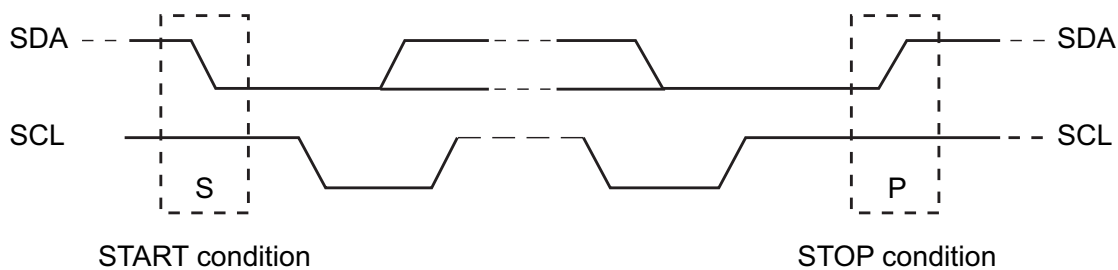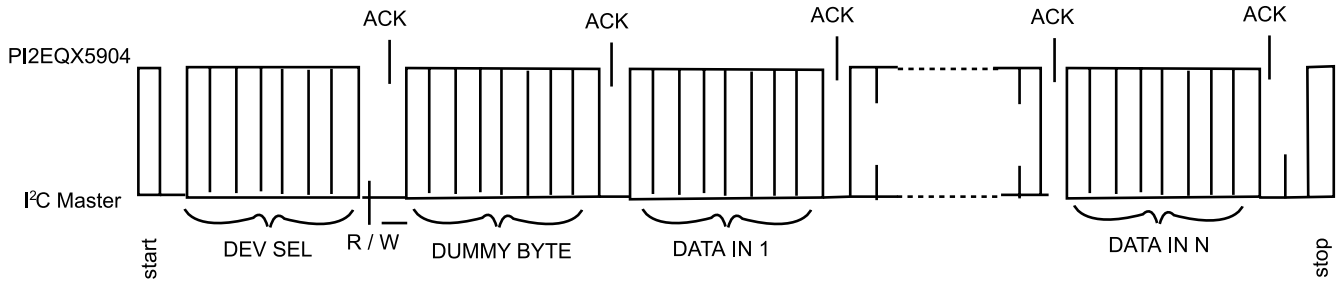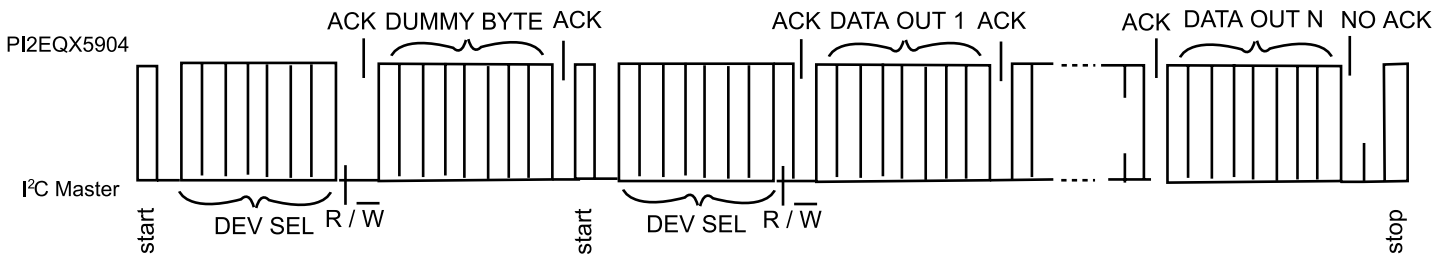

I²C START and STOP conditions.

I2C Data Transfer

1. Read sequence

2. Write sequence

3. Combined sequence

Notes:
1. only block read and block write from the lowest byte are supported for this application.
2. for some I2C application, an offset address byte will be presented at the second byte in write command, which is called dummy byte here and will be simply ignored in this application for correct interoperation.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . −65°C to +150°C
Supply Voltage to Ground Potential . . . . −0.5V to +2.5V
DC SIG Voltage . . . . −0.5V to V_{DD} +0.5V
I^2C DC SIG Voltage . . . .−0.5V to +3.6V
Current Output . . . . −25mA to +25mA
Power Dissipation Continuous 1W
Operating Temperature . . . .−40°C to +85°C
ESD, HBM: I^2C pins . . . . −1kV to +1kV
ESD, HBM: All other pins . . . . −2kV to +2kV

Note:

Stresses greater than those listed under MAXI-MUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

Power Supply Characteristics (V_{DD} = 1.2 ±0.05V, T_A = -40°C ~ +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{DDactive}$	Power supply current - active	All channels switching			800	
$I_{DDstandby}$	Power supply current - standby	PD# = 0		1	5	mA
$I_{DD-channel}$	Power supply current - per channel, Active			50		

AC Performance Characteristics (V_{DD} = 1.2 ±0.05V, T_A = -40°C ~ +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{pd}	Channel latency from input to output			750		ps

CML Receiver Input (V_{DD} = 1.2 ±0.05V, T_A = -40°C ~ +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ZRX-DIFF-DC	DC Differential Input Impedance		80	100	120	Ohms
ZRX-DC	DC Input Impedance		40	50	60	
VRX-DIFFP-P	Differential Input Peak-to-peak Voltage		0.175		1.200	V
VRX-CM-ACP	AC Peak Common Mode Input Voltage				150	mV
Vth-DIFF p-p	Signal detect threshold voltage		65	100	175	

Equalizer

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
J_{RS-T}	Residual jitter	Total			0.3	Ulp-p
J_{RS-D}	Residual jitter	Deterministic			0.2	Ulp-p
J_{RM}	Random jitter	Note 2		1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in AC test circuit (see figure).

2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of the AC test circuit (see figure).

CML Transmitter Output $(V_{DD} = 1.2V \pm 0.05V, T_A = -40°C \sim +85°C)$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Z_{OUT}	Output resistance	Single ended	40	50	60	Ohms
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	
V_{DIFFP}	Output Voltage Swing, Differential	|VTX-D+ - VTX-D-|	200		800	mVp-p
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage	VTX-DIFFP-P = 2 * | VTX-D+ - VTX-D- |	0.4		1.6	V
V_{TX-C}	Common-Mode Voltage	| VTX-D+ + VTX-D- | / 2		VDD- 0.3		
t_F, t_R	Transition Time	20% to 80%			150	ps
$C_{TX}^{(1)}$	AC Coupling Capacitor		75		200	nF

Note:

1. Recommended external blocking capacitor.

SDA and SCL I/O for I2C-bus $(V_{DD} = 1.2 \pm 0.05v, T_A = -40°C \sim +85°C)$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		$0.85V_{DD}$		3.6	V
V_{IL}	DC input logic low		-0.3		$0.3V_{DD}$	
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	
V_{hys}	Hysteresis of Schmitt trigger input		0.2			

Characteristics of the SDA and SCl bus lines for Standard Mode I^{2}C-bus devices[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f$_{SCL}$	SCL clock frequency		0		100	kHz
t$_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0		–	
t$_{LOW}$	LOW period of the SCL clock		4.7		–	μs
t$_{HIGH}$	HIGH period of the SCL clock		4.0		–	
t$_{SU;STA}$	Set-up time for a repeated START condition		4.7		–	
t$_{HD;DAT}$	Data hold time		10		–	ns
t$_{SU;DAT}$	Data set-up time		250		–	
t$_r$	Rise time of both SDA and SCL signals		-		1000	ns
t$_f$	Fall time of both SDA and SCL signals				300	
t$_{SU;STO}$	Set-up time for STOP condition		4.0		–	
t$_{BUF}$	Bus free time between a STOP and STOP condition		4.7		–	μs
C$_b$	Capacitive load for each bus line		-		400	pF

Notes:

**1.** All values referred to VIH min and VIL max levels

Digital I/O DC Specifications (V_{DD} = 1.2V ± 0.05V, T_A = -40°C ~ +85°C)

| Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		VDD/2 +0.2		VDD+0.3	V
V_{IL}	DC input logic low		-0.3		VDD/2 -0.2	
V_{OH}	DC output logic high	I_{OH} = 4mA	VDD-0.4			
V_{OL}	DC output logic low	I_{OL} = 4mA			0.4	
V_{hys}	Hysteresis of Schmitt trigger input		0.2			
I_{IH}[1]	Input high current				100	µA
I_{IL1}[2]	Input low current		-20			
I_{IL2}[3]	Input low current		-20			

Notes:

1. Includes input signals A1, A2, A4, Dx_[A:B], DE_[A:B], LB#, MODE#, PD#, RESET#, RXD_[A:B], Sx_[A:B], SCL, SDA, SEL_x[A:B]

2. For control inputs without pullups: SCL, SDA

3. Control inputs with pull-ups include: Dx_[A:B], DE_[A:B], LB#, MODE#, PD#, RESET#, RXD_[A:B], Sx_[A:B], SEL_x[A:B], A1, A2, A4
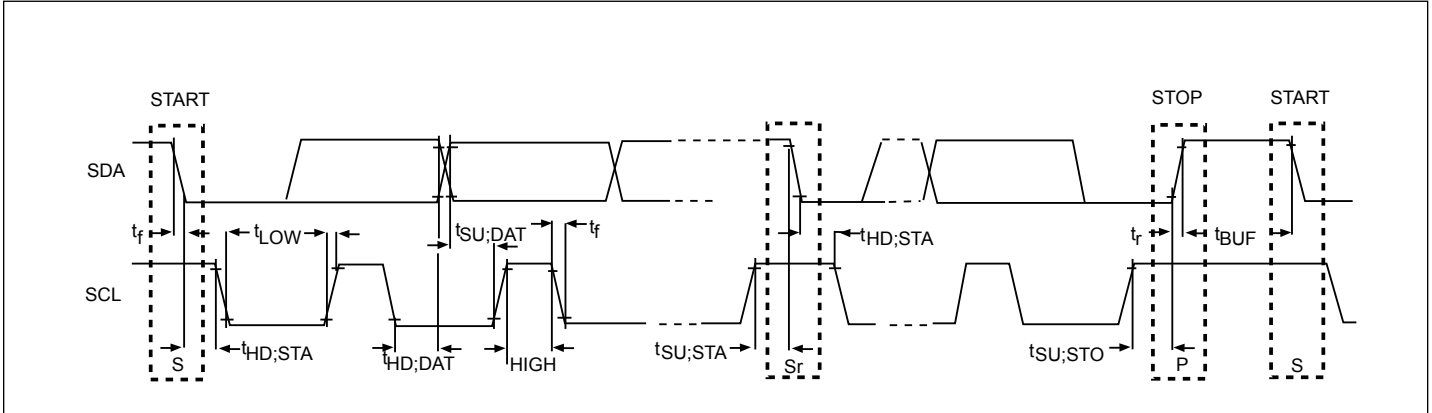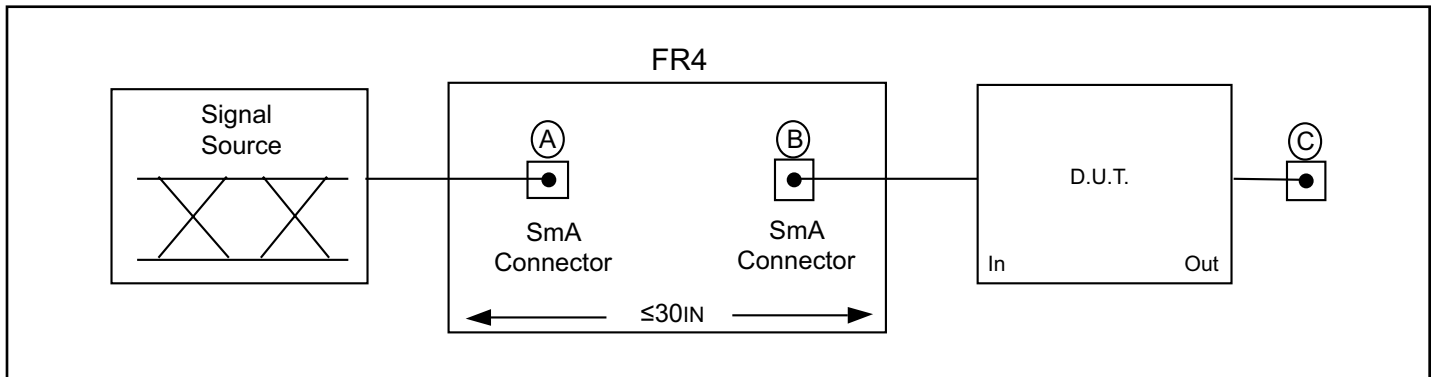
I²C Timing
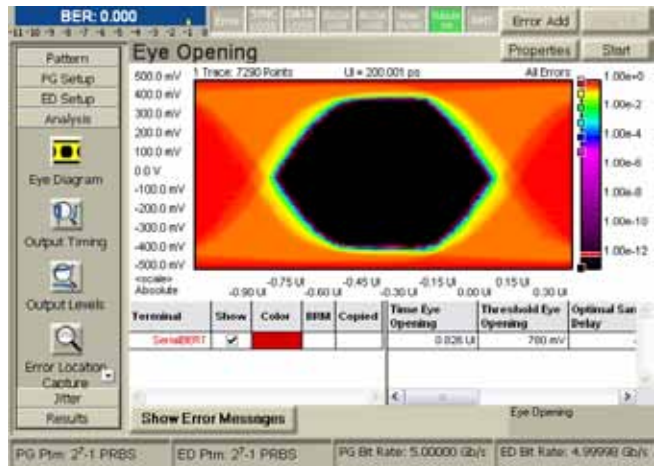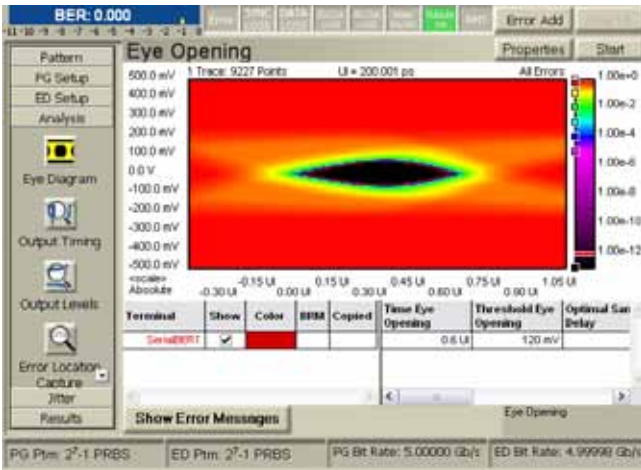
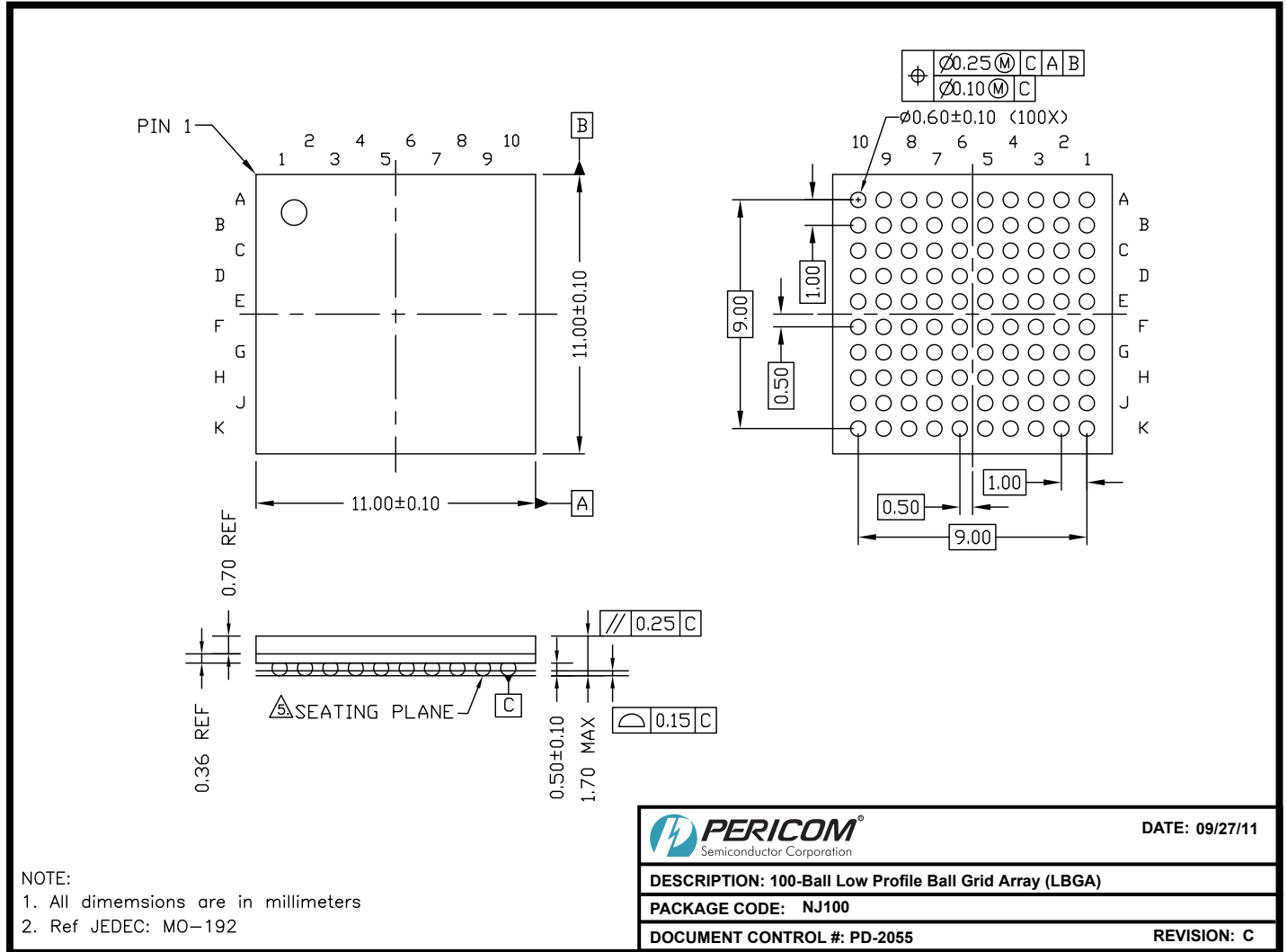**Eye Diagrams 5.0Gbps (input left, output right)**

Data Waveforms, 2.5Gbps (left) & 5.0Gbps (right)

AC Test Circuit Referenced in the Electrical Characteristic Table

Packaging Information

NOTE:
1. All dimensions are in millimeters
2. Ref JEDEC: MO−192

DESCRIPTION: 100-Ball Low Profile Ball Grid Array (LBGA)

PACKAGE CODE: NJ100

DOCUMENT CONTROL #: PD-2055

DATE: 09/27/11

REVISION: C

11-0196

Note: For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX5904NJE	NJ	Pb-free & Green 100-Contact LBGA

Notes:

• **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**

• **E = Pb-free and Green**

• **X suffix = Tape/Reel**