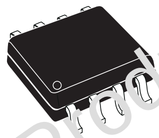
TSH350

550MHz low noise current feedback amplifier

Features

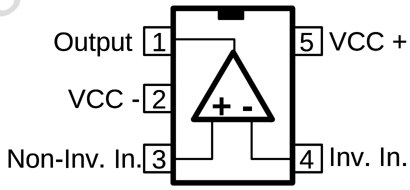
- Bandwidth: 550MHz in unity gain
- Quiescent current: 4.1mA
- Slew rate: 940V/µs
- Input noise: 1.5nV/√Hz
- Distortion: SFDR=-66dBc (10MHz, $1V_{pp}$)
- $2.8V_{pp}$ minimum output swing on 100Ω load for a 5V supply
- Tested on 5V power supply

SOT23-5

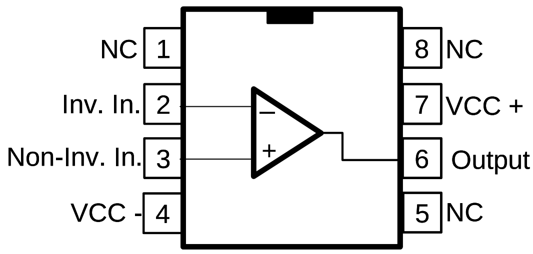


SO-8

Pin connections (top view)



SOT23-5



SO-8

Applications

- Communication & video test equipment
- Medical instrumentation
- ADC drivers

Description

The TSH350 is a current feedback operational amplifier using a very high-speed complementary technology to provide a bandwidth up to 410MHz while drawing only 4.1mA of quiescent current. With a slew rate of 940V/µs and an output stage optimized for driving a standard 100Ω load, this circuit is highly suitable for applications where speed and power-saving are the main requirements.

The TSH350 is a single operator available in the tiny SOT23-5 and SO-8 plastic packages, saving board space as well as providing excellent thermal and dynamic performance.

1 Absolute maximum ratings

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{id}	Differential input voltage(2)	+/-0.5	V
V_{in}	Input voltage range(3)	+/-2.5	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient SOT23-5 SO-8	 250 150	°C/W
R_{thjc}	Thermal resistance junction to case SOT23-5 SO-8	 80 28	°C/W
P_{max}	Maximum power dissipation(4) (@T_{amb}=25°C) for T_j=150°C SOT23-5 SO-8	 500 830	mW
ESD	HBM: human body model (5) pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	 2 0.5	kV
	MM: machine model (6) pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	 200 60	V
	CDM: charged device model(7) pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	 1.5 1.5	kV
	Latch-up immunity	200	mA

1. All voltage values are measured with respect to the ground pin.
2. Differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltage must never exceed V_{CC} +0.3V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on all amplifiers.
5. Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	4.5 to 5.5	V
V_{icm}	Common mode input voltage	$-V_{CC}$+1.5V to $+V_{CC}$-1.5V	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C

1. Tested in full production at 5V (±2.5V) supply voltage.

2 Electrical characteristics

Table 3. Electrical characteristics for $V_{CC} = \pm2.5V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	**Input offset voltage** Offset voltage between both inputs	T_{amb}		0.8	4	mV
		$T_{min} < T_{amb} < T_{max}$		1		
ΔV_{io}	V_{io} drift vs. temperature	$T_{min} < T_{amb} < T_{max}$		0.9		µV/°C
I_{ib+}	**Non inverting input bias current** DC current necessary to bias the input +	T_{amb}		12	35	µA
		$T_{min} < T_{amb} < T_{max}$		13		
I_{ib-}	**Inverting input bias current** DC current necessary to bias the input -	T_{amb}		1	20	µA
		$T_{min} < T_{amb} < T_{max}$		2.5		
CMR	Common mode rejection ratio 20 log $(\Delta V_{ic}/\Delta V_{io})$	$\Delta V_{ic} = \pm1V$	56	60		dB
		$T_{min} < T_{amb} < T_{max}$		58		
SVR	Supply voltage rejection ratio 20 log $(\Delta V_{CC}/\Delta V_{io})$	ΔV_{CC}=+3.5V to +5V	68	81		dB
		$T_{min} < T_{amb} < T_{max}$		78		
PSR	Power supply rejection ratio 20 log $(\Delta V_{CC}/\Delta V_{out})$	$A_V = +1$, $\Delta V_{CC}=\pm100mV$ at 1kHz		51		dB
		$T_{min} < T_{amb} < T_{max}$		48		
I_{CC}	**Positive supply current** DC consumption with no input signal	No load		4.1	4.9	mA
Dynamic performance and output characteristics						
R_{OL}	**Transimpedance** Output voltage/input current gain in open loop of a CFA. For a VFA, the analog of this feature is the open loop gain (A_{VD})	$\Delta V_{out} = \pm1V$, $R_L = 100\Omega$	170	270		kΩ
		$T_{min} < T_{amb} < T_{max}$		250		kΩ
Bw	**-3dB bandwidth** Frequency where the gain is 3dB below the DC gain A_V Note: Gain bandwidth product criterion is not applicable for current-feedback-amplifiers	Small signal $V_{out}=20mV_{pp}$ $A_V = +1$, $R_L = 100\Omega$ $A_V = +2$, $R_L = 100\Omega$ $A_V = +10$, $R_L = 100\Omega$ $A_V = -2$, $R_L = 100\Omega$	250	550 390 125 370		MHz
	Gain flatness @ 0.1dB Band of frequency where the gain variation does not exceed 0.1dB	Small signal $V_{out}=100mV_p$ $A_v = +1$, $R_L = 100\Omega$		65		
SR	**Slew rate** Maximum output speed of sweep in large signal	$V_{out} = 2V_{pp}$, $A_V = +2$, $R_L = 100\Omega$		940		V/µs
V_{OH}	High level output voltage	$R_L = 100\Omega$	1.44	1.56		V
		$T_{min} < T_{amb} < T_{max}$		1.49		

Table 3. Electrical characteristics for V_{CC} = ±2.5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	$R_L = 100\Omega$		-1.53	-1.44	V
		$T_{min} < T_{amb} < T_{max}$		-1.49		
I_{out}	**I_{sink}** Short-circuit output current coming in the op-amp (see *Figure 9*)	Output to GND	135	205		mA
		$T_{min} < T_{amb} < T_{max}$		195		
	I_{source} Output current coming out from the op-amp (see *Figure 10*)	Output to GND	-140	-210		
		$T_{min} < T_{amb} < T_{max}$		-185		
Noise and distortion						
eN	**Equivalent input noise voltage** See *Section 5: Noise measurements*	F = 100kHz		1.5		nV/√Hz
iN	**Equivalent input noise current (+)** See *Section 5: Noise measurements*	F = 100kHz		20		pA/√Hz
	Equivalent input noise current (-) See *Section 5: Noise measurements*	F = 100kHz		13		pA/√Hz
SFDR	**Spurious free dynamic range** The highest harmonic of the output spectrum when injecting a filtered sine wave	$A_V = +1$, $V_{out} = 1V_{pp}$ F = 10MHz F = 20MHz F = 50MHz F = 100MHz		 -66 -57 -46 -42		dBc

Table 4. Closed-loop gain and feedback components

V_{CC} (V)	Gain	R_{fb} (Ω)	-3dB Bw (MHz)	0.1dB Bw (MHz)
±2.5	+10	300	125	22
	-10	300	120	20
	+2	300	390	110
	-2	300	370	70
	+1	820	550	65
	-1	300	350	120

Figure 1. Frequency response, positive gain

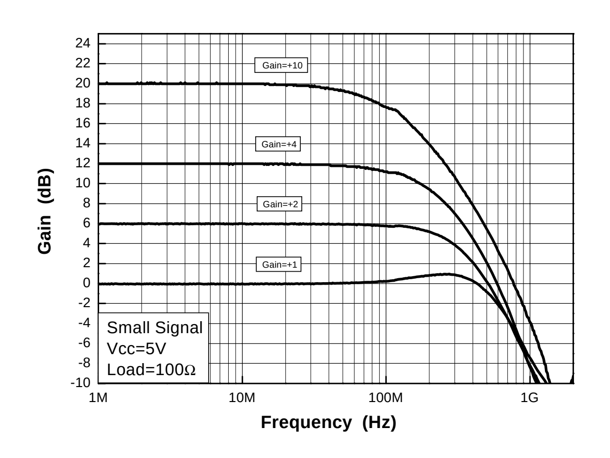


Figure 2. Frequency response, negative gain

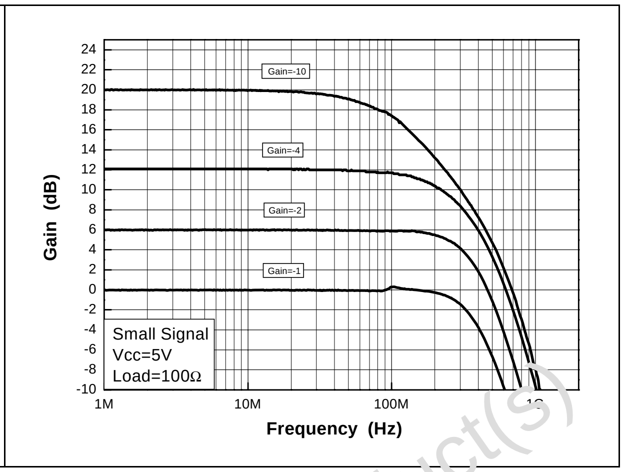


Figure 3. Compensation, gain=+4

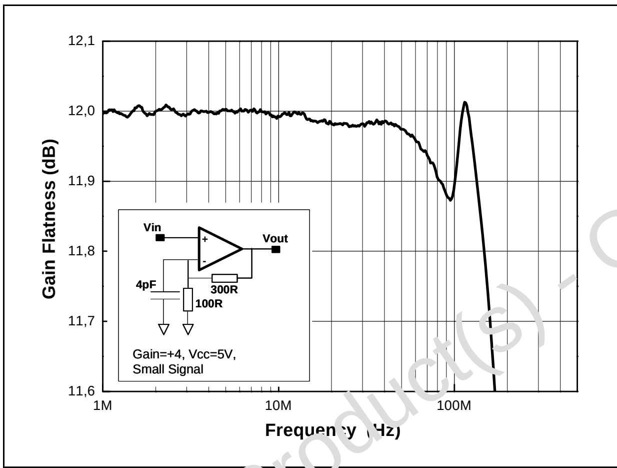


Figure 4. Compensation, gain=+2

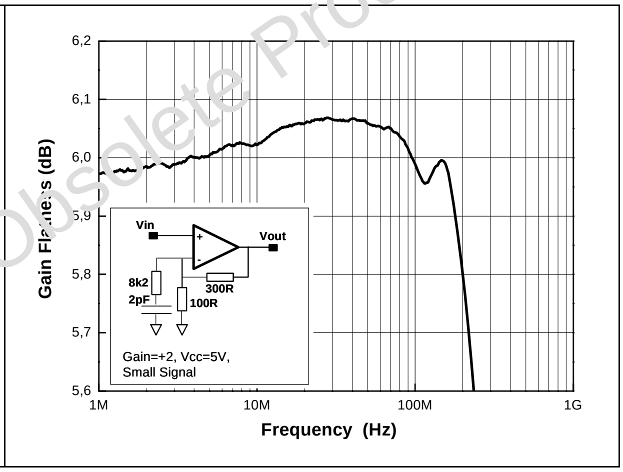


Figure 5. Frequency response vs. capacitor load

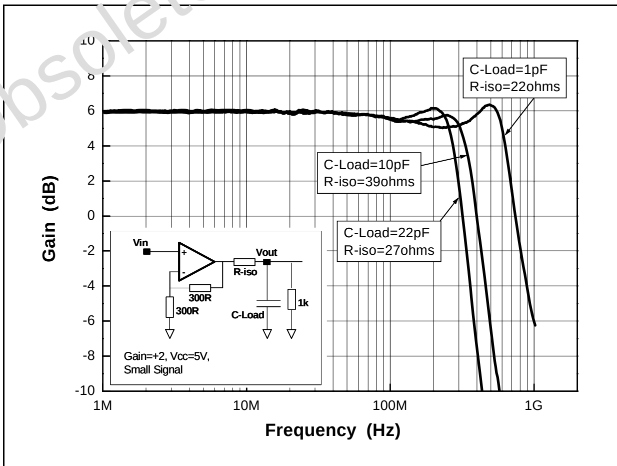


Figure 6. Step response vs. capacitor load

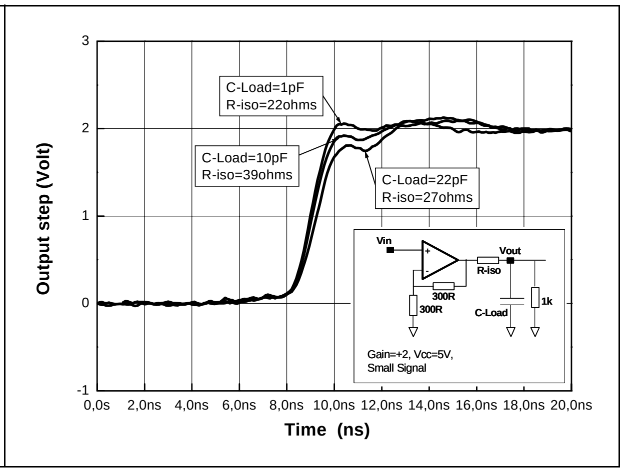


Figure 7. Slew rate

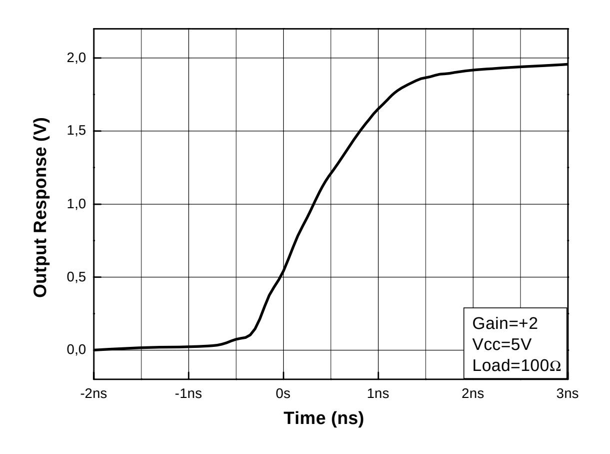


Figure 8. Output amplitude vs. load

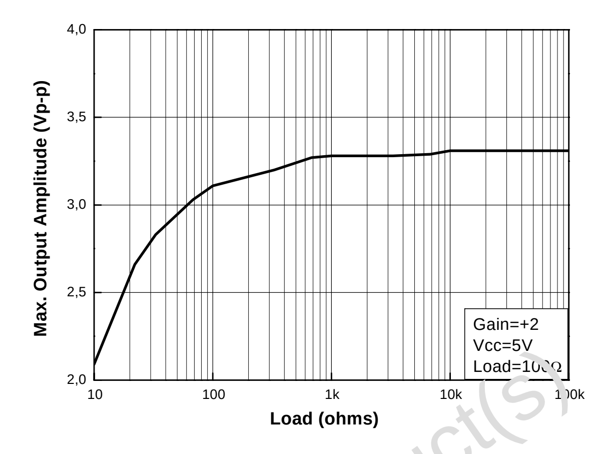


Figure 9. I_{sink}

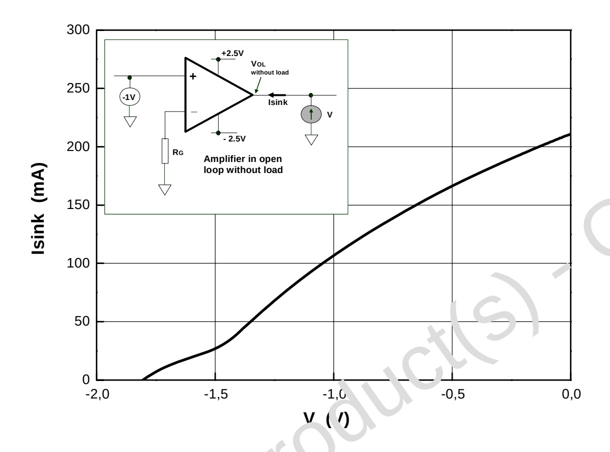


Figure 10. I_{source}

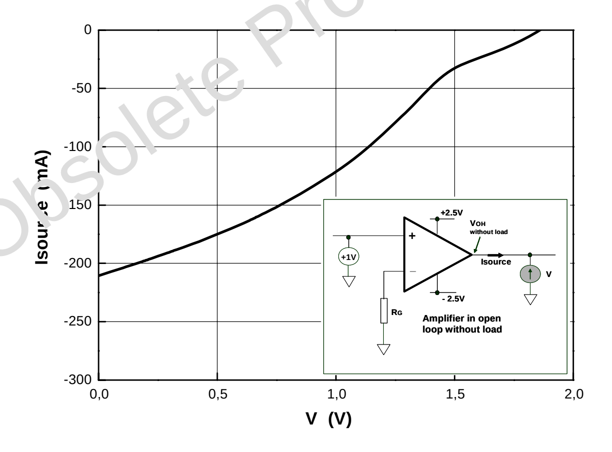


Figure 11. Input current noise vs. frequency

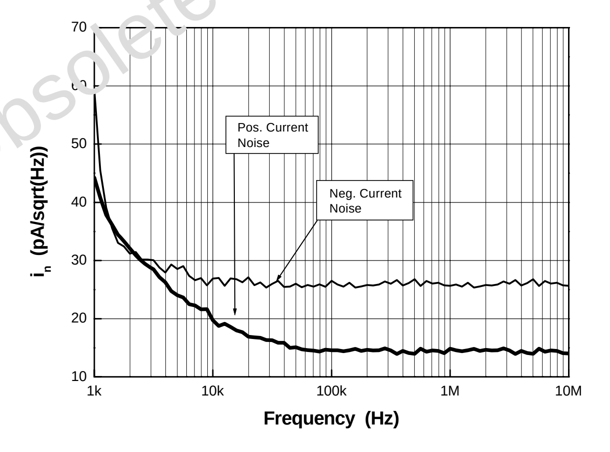


Figure 12. Input voltage noise vs. frequency

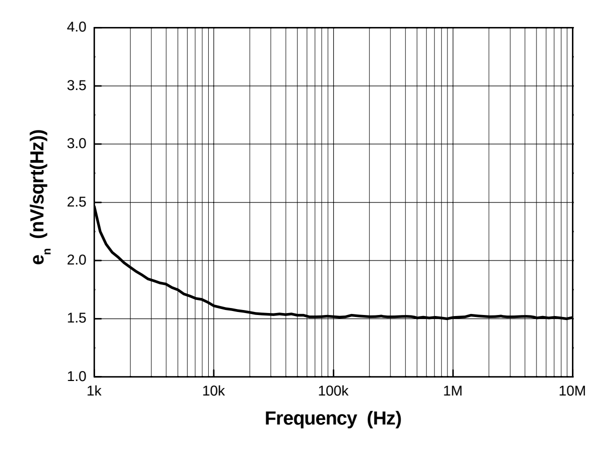


Figure 13. Quiescent current vs. V_{CC}

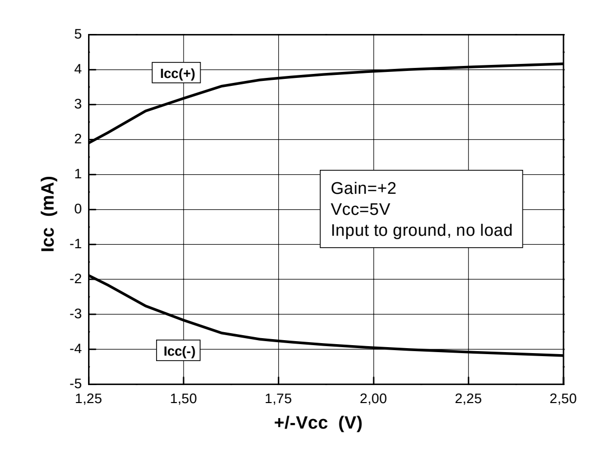


Figure 14. Distortion vs. output amplitude

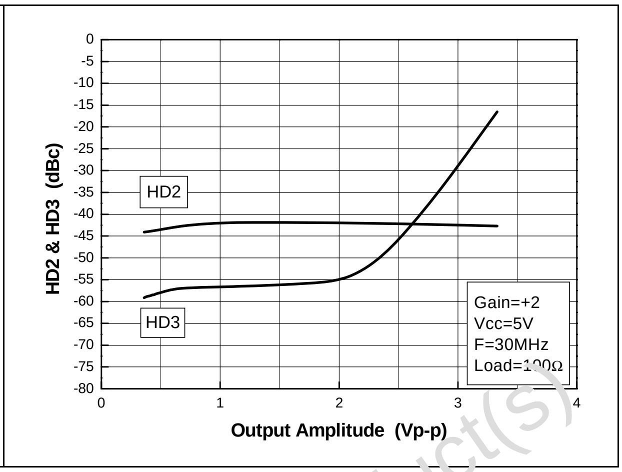


Figure 15. Distortion vs. output amplitude

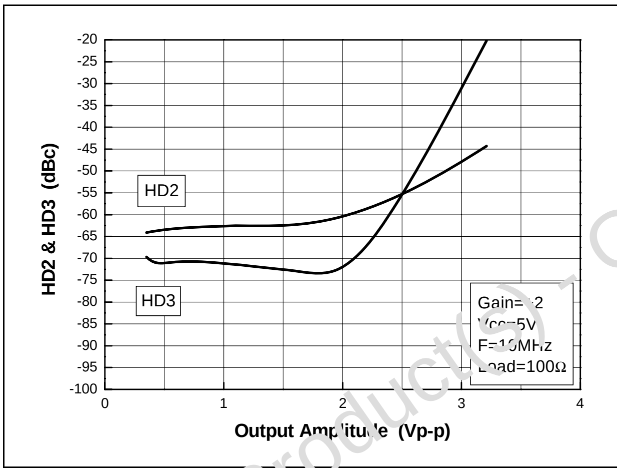


Figure 16. Noise figure

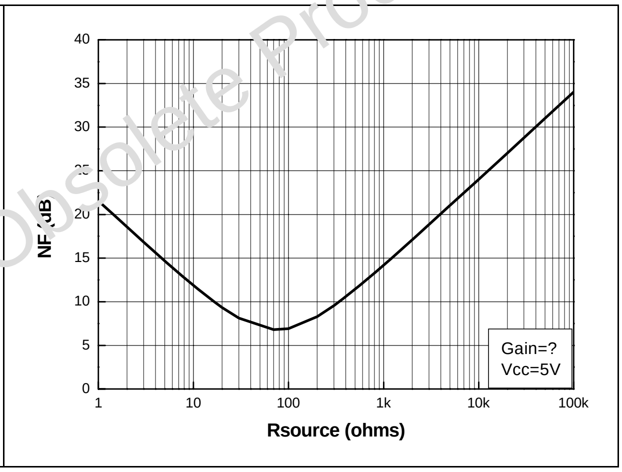


Figure 17. Distortion vs. output amplitude

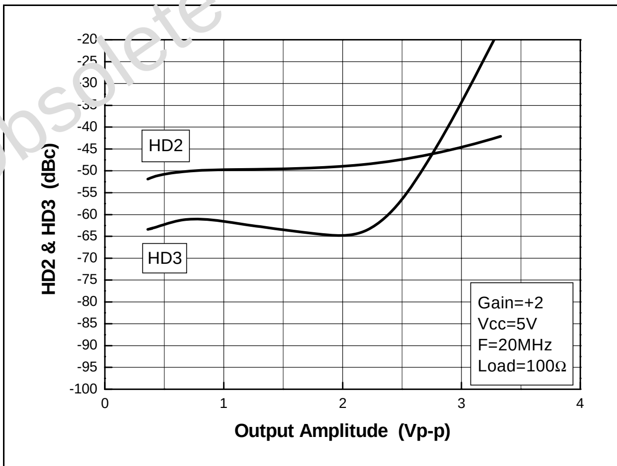


Figure 18. Output amplitude vs. frequency

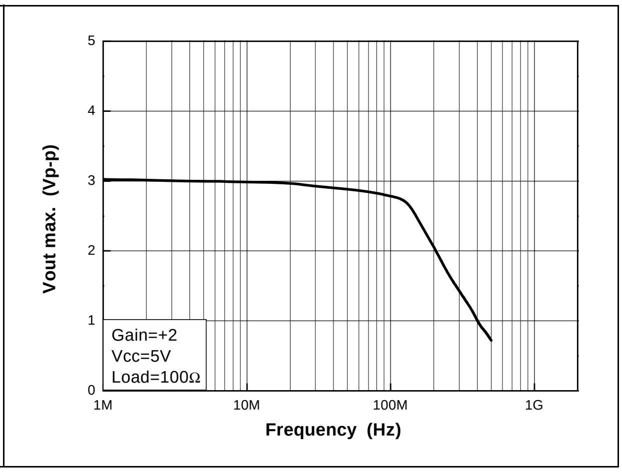


Figure 19. Reverse isolation vs. frequency

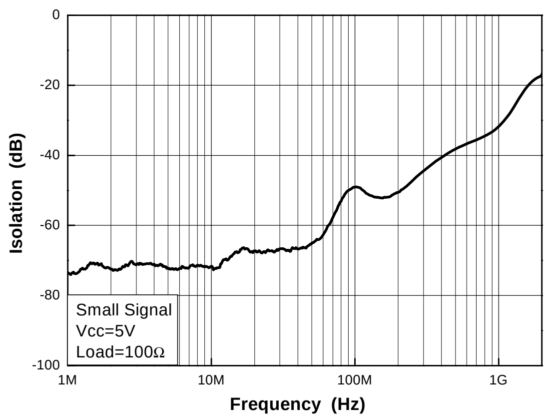


Figure 20. SVR vs. temperature

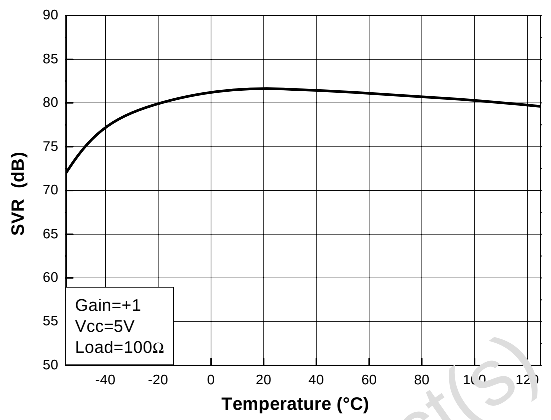


Figure 21. Bandwidth vs. temperature

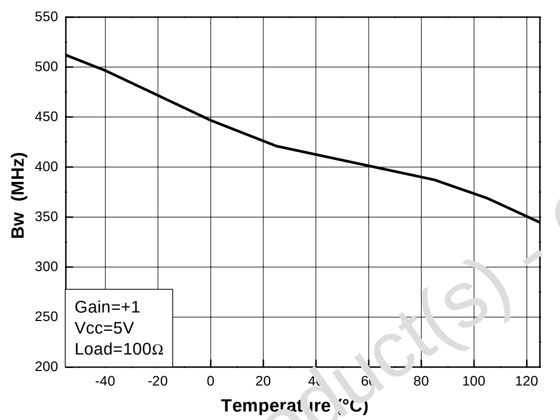


Figure 22. R_{OL} vs. temperature

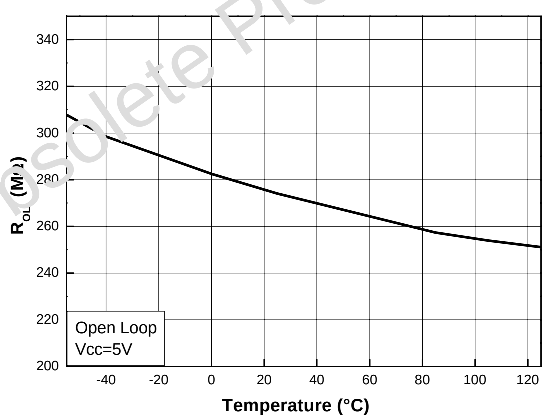


Figure 23. CMR vs. temperature

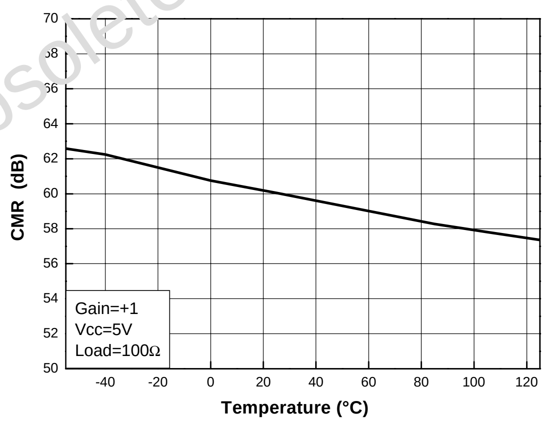


Figure 24. I_{bias} vs. temperature

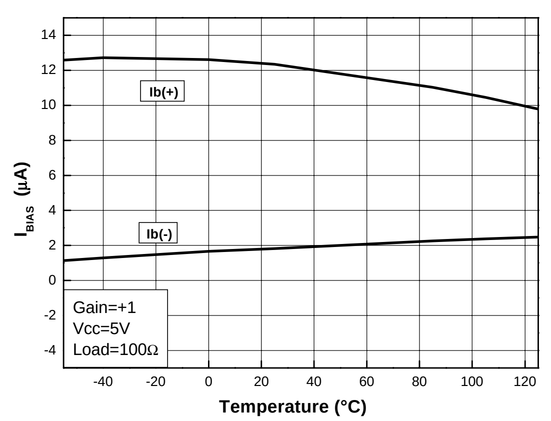


Figure 25. V_{io} vs. temperature

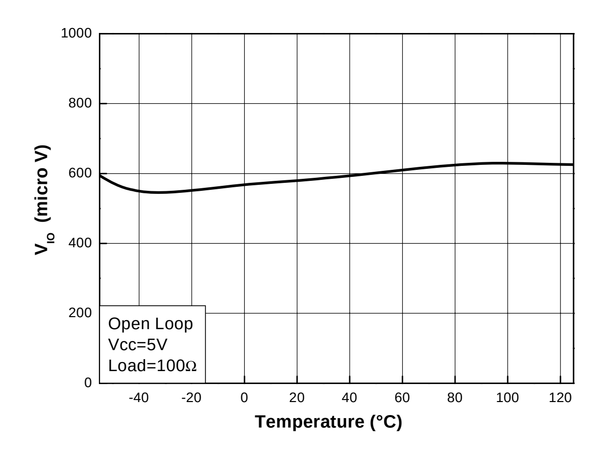


Figure 26. I_{CC} vs. temperature

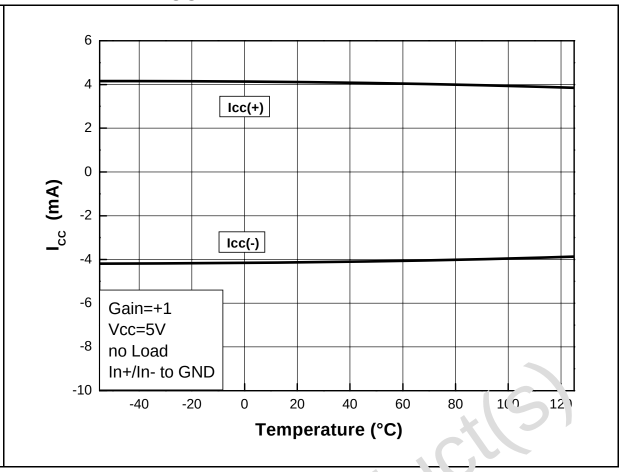


Figure 27. V_{OH} and V_{OL} vs. temperature

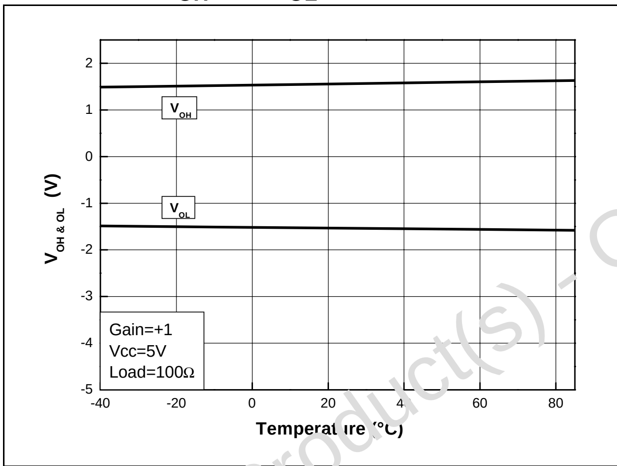
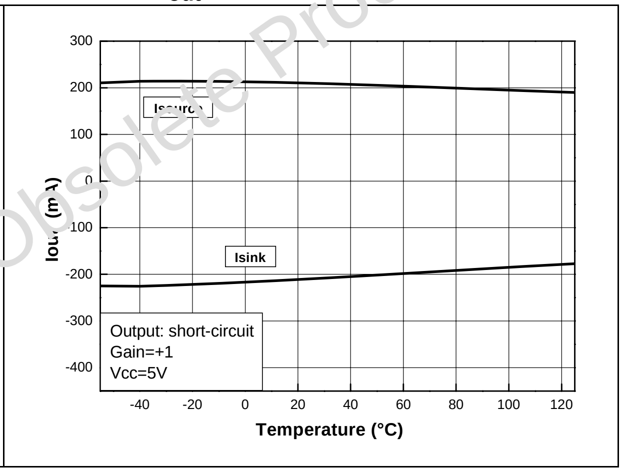


Figure 28. I_{out} vs. temperature



3 Evaluation boards

An evaluation board kit optimized for high-speed operational amplifiers is available (order code: KITHSEVAL/STDL). As well as a CD-ROM containing datasheets, articles, application notes and a user manual, the kit includes the following evaluation boards:

- SOT23_SINGLE_HF BOARD
  Board for the evaluation of a single high-speed op-amp in SOT23-5 package.
- SO8_SINGLE_HF
  Board for the evaluation of a single high-speed op-amp in SO-8 package.
- SO8_DUAL_HF
  Board for the evaluation of a dual high-speed op-amp in SO-8 package.
- SO8_S_MULTI
  Board for the evaluation of a single high-speed op-amp in SO-8 package in inverting and non-inverting configuration, dual and single supply.
- SO14_TRIPLE
  Board for the evaluation of a triple high-speed op-amp in SO-14 package with video application considerations.

Board material:

- 2 layers
- FR4 (ε_r=4.6)
- epoxy 1.6mm
- copper thickness: 35µm

Figure 29. Evaluation kit for high-speed op-amps

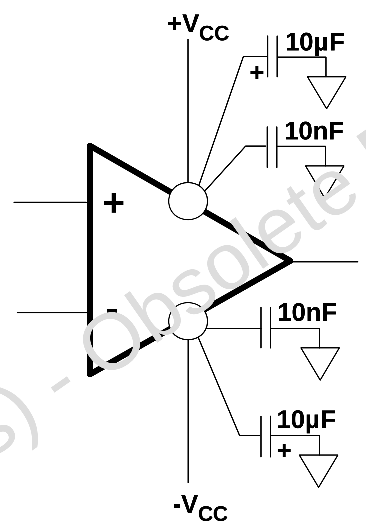
4 Power supply considerations

Correct power supply bypassing is very important for optimizing performance in high-frequency ranges. Bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than 1µF is necessary to minimize the distortion. For better quality bypassing, a capacitor of 10nF can be added which should also be placed as close as possible to the IC pins.

Bypass capacitors must be incorporated for both the negative and the positive supply.

Note: On the SO8_SINGLE_HF board, these capacitors are C6, C7, C8, C9.

Figure 30. Circuit for power supply bypassing



Single power supply

In the event that a single supply system is used, biasing is necessary to obtain a positive output dynamic range between 0V and +V_{CC} supply rails. Considering the values of V_{OH} and V_{OL}, the amplifier will provide an output swing from +0.9V to +4.1V on a 100Ω load.

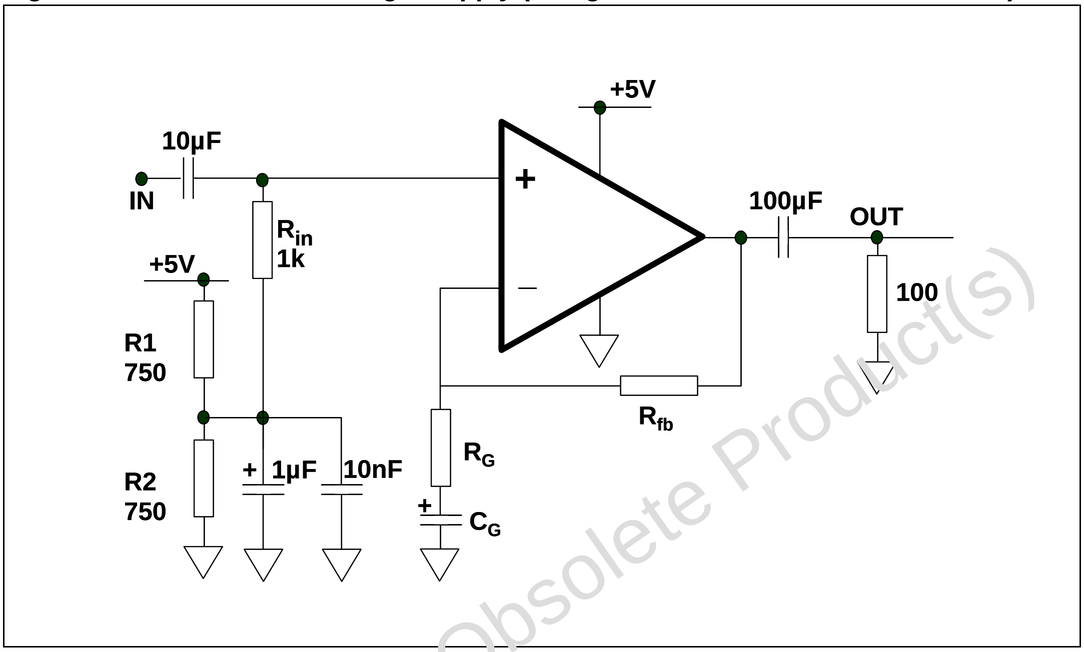
The amplifier must be biased with a mid-supply (nominally +V_{CC}/2), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (35µA maximum) as 1% of the current through the resistance divider, to keep a stable mid-supply, two resistances of 750Ω can be used.

The input provides a high-pass filter with a break frequency below 10Hz which is necessary to remove the original 0 volt DC component of the input signal, and to fix it at +V_{CC}/2.

Figure 31 illustrates a 5V single power supply configuration for the SO8_S_MULTI evaluation board (see *Evaluation boards* on page 11).

A capacitor C_G is added in the gain network to ensure a unity gain in low frequency to keep the right DC component at the output. C_G contributes to a high-pass filter with $R_{fb}//R_G$ and its value is calculated with a consideration of the cut off frequency of this low-pass filter.

Figure 31. Circuit for +5V single supply (using evaluation board SO8_S_MULTI)

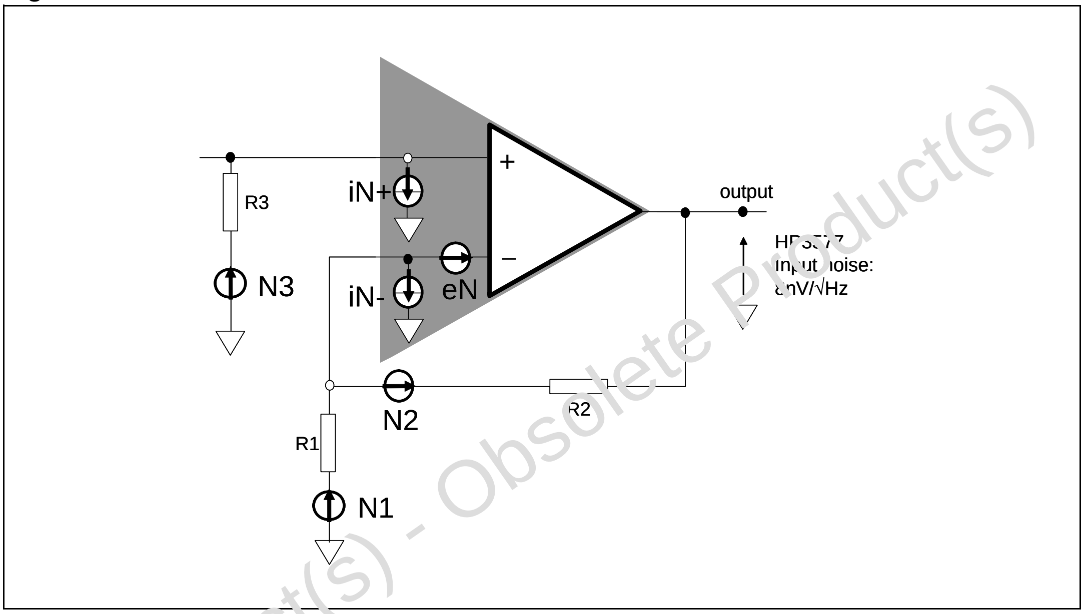


5 Noise measurements

The noise model is shown in *Figure 32*:

- eN is the input voltage noise of the amplifier
- iNn is the negative input current noise of the amplifier
- iNp is the positive input current noise of the amplifier

Figure 32. Noise model



The thermal noise of a resistance R is

$$\sqrt{4kTR\Delta F}$$

where ΔF is the specified bandwidth.

On a 1Hz bandwidth the thermal noise is reduced to:

$$\sqrt{4kTR}$$

where k is the Boltzmann's constant, equal to 1,374.10-23J/°K. T is the temperature (°K).

The output noise eNo is calculated using the Superposition Theorem. However, eNo is not the simple sum of all noise sources, but rather the square root of the sum of the square of each noise source, as shown in *Equation 1*:

Equation 1

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2}$$

Equation 2

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + \frac{R2^2}{R1} \times 4kTR1 + 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

Equation 3

$$eNo = \sqrt{(Measured)^2 - (instrumentation)^2}$$

The input noise is called **equivalent input noise** because it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain (eNo/g).

After simplification of the fourth and the fifth term of *Equation 2* we obtain:

Equation 4

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + g \times 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3$$

Measurement of the input voltage noise *eN*

If we assume a short-circuit on the non-inverting input (R3=0), from *Equation 4* we can derive:

Equation 5

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2}$$

In order to easily extract the value of eN, the resistance R2 will be chosen to be as low as possible. In the other hand, the gain must be large enough:

R3=0, gain: g=100

Measurement of the negative input current noise *iNn*

To measure the negative input current noise iNn, we set R3=0 and use *Equation 5*. This time, the gain must be lower in order to decrease the thermal noise contribution:

R3=0, gain: g=10

Measurement of the positive input current noise *iNp*

To extract iNp from *Equation 3*, a resistance R3 is connected to the non-inverting input. The value of R3 must be chosen in order to keep its thermal noise contribution as low as possible against the iNp contribution:

R3=100W, gain: g=10

6 Intermodulation distortion product

The non-ideal output of the amplifier can be described by the following series:

$$V_{out} = C_0 + C_1 V_{in} + C_2 V^2{}_{in} + \ldots + C_n V^n{}_{in}$$

where the input is V_{in}=Asinωt, C_0 is the DC component, $C_1(V_{in})$ is the fundamental and C_n is the amplitude of the harmonics of the output signal V_{out}.

A one-frequency (one-tone) input signal contributes to harmonic distortion. A two-tone input signal contributes to harmonic distortion and to the intermodulation product.

The study of the intermodulation and distortion for a two-tone input signal is the first step in characterizing the driving capability of multi-tone input signals.

In this case:

$$V_{in} = A\sin\omega_1 t + A\sin\omega_2 t$$

then:

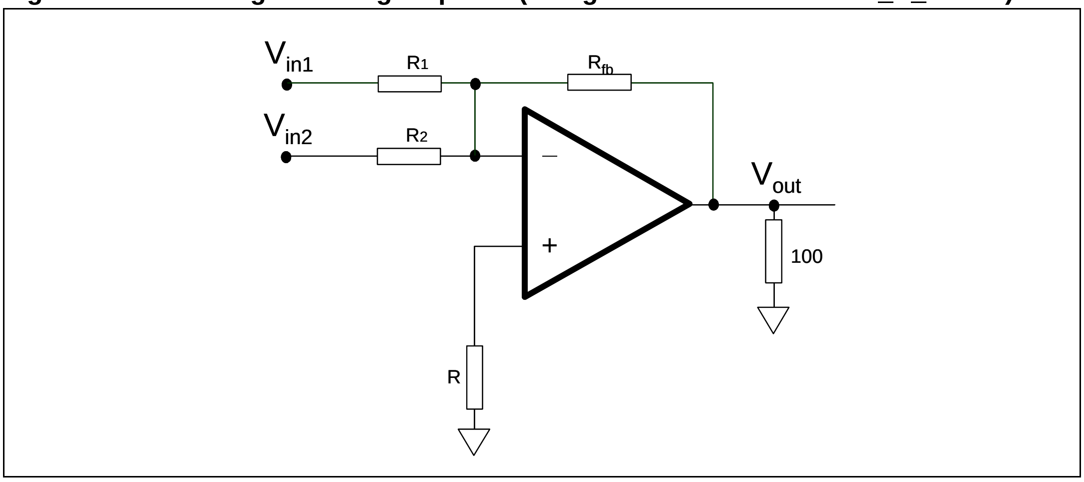
$$V_{out} = C_0 + C_1(A\sin\omega_1 t + A\sin\omega_2 t) + C_2(A\sin\omega_1 t + A\sin\omega_2 t)^2 \ldots + C_n(A\sin\omega_1 t + A\sin\omega_2 t)^n$$

From this expression, we can extract the distortion terms, and the intermodulation terms from a single sine wave:

- second order intermodulation terms IM2 by the frequencies $(\omega_1\text{-}\omega_2)$ and $(\omega_1+\omega_2)$ with an amplitude of $C2A^2$
- third order intermodulation terms IM3 by the frequencies $(2\omega_1\text{-}\omega_2)$, $(2\omega_1+\omega_2)$, $(-\omega_1+2\omega_2)$ and $(\omega_1+2\omega_2)$ with an amplitude of $(3/4)C3A^3$

The intermodulation product of the driver is measured by using the driver as a mixer in a summing amplifier configuration (see *Figure 33*). In this way, the non-linearity problem of an external mixing device is avoided.

Figure 33. Inverting summing amplifier (using evaluation board SO8_S_MULTI)



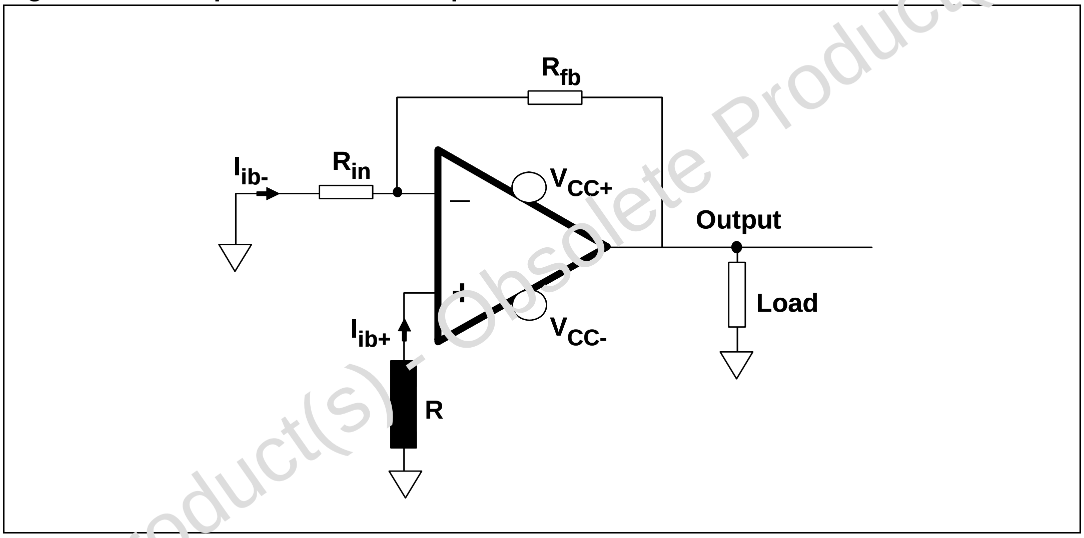
7 Inverting amplifier biasing

A resistance is necessary to achieve good input biasing, such as resistance R shown in *Figure 34*.

The magnitude of this resistance is calculated by assuming the negative and positive input bias current. The aim is to compensate for the offset bias current, which could affect the input offset voltage and the output DC component. Assuming I_{ib-}, I_{ib+}, R_{in}, R_{fb} and a zero volt output, the resistance R is:

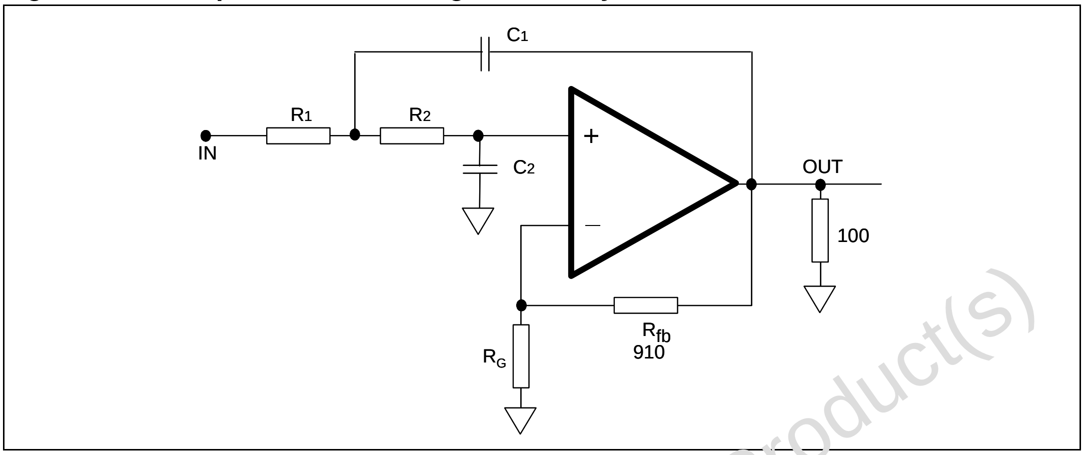
$$R = \frac{R_{in} \times R_{fb}}{R_{in} + R_{fb}}$$

Figure 34. Compensation of the input bias current



8 Active filtering

Figure 35. Low-pass active filtering, Sallen-Key



From the resistors R_{fb} and R_G we can directly calculate the gain of the filter in a classic non-inverting amplification configuration:

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

We assume the following expression as the response of the system:

$$T_{j\omega} = \frac{Vout_{j\omega}}{Vin_{j\omega}} = \frac{g}{1 + 2\zeta\frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^{\ 2}}}$$

The cut-off frequency is not gain-dependent and so becomes:

$$\omega_c = \frac{1}{\sqrt{R1R2C1C2}}$$

The damping factor is calculated by the following expression:

$$\zeta = \frac{1}{2}\omega_c(C_1R_1 + C_1R_2 + C_2R_1 - C_1R_1g)$$

The higher the gain, the more sensitive the damping factor is. When the gain is higher than 1, it is preferable to use some very stable resistor and capacitor values. In the case of R1=R2=R:

$$\zeta = \frac{2C_2 - C_1\frac{R_{fb}}{R_g}}{2\sqrt{C_1C_2}}$$

Due to a limited selection of values of capacitors in comparison with resistors, we can set C1=C2=C, so that:

$$\zeta = \frac{2R_2 - R_1\frac{R_{fb}}{R_g}}{2\sqrt{R_1R_2}}$$

9 Package information

Figure 36. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.00		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6

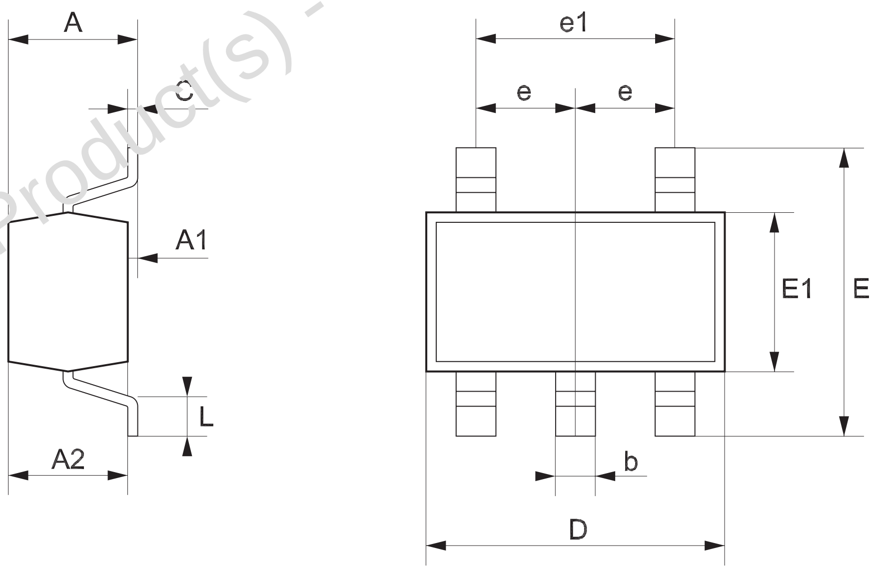
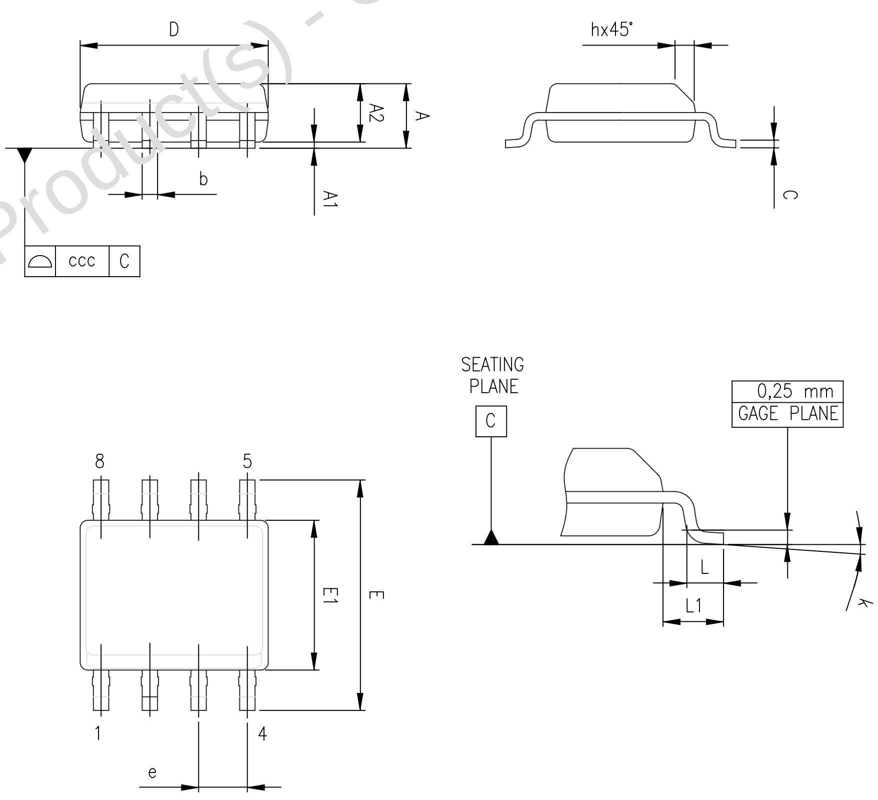


Figure 37. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
H	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004



10 Ordering information

Table 5. Order codes

Part number	Temperature range	Package	Packing	Marking
TSH350ILT	-40°C to +85°C	SOT23-5	Tape & reel	K305
TSH350ID		SO-8	Tube	TSH350I
TSH350IDT		SO-8	Tape & reel	TSH350I

11 Revision history

Date	Revision	Changes
1-Oct-2004	1	First release corresponding to Preliminary Data version of datasheet.
10-Dec-2004	2	Release of mature product datasheet.
21-Jun-2005	3	In *Table 1* on page 2, R_{thjc} thermal resistance junction to ambient replaced by thermal resistance junction to case.
8-Jun-2007	4	Format update.