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November 2013

### FQP32N20C / FQPF32N20C

## N-Channel QFET® MOSFET

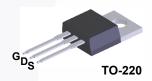
### 200 V, 28 A, 82 m $\Omega$

### **Features**

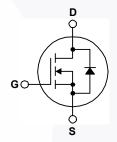
- 28 A, 200 V,  $R_{DS(on)}$  = 82 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 14 A
- Low Gate Charge (Typ. 82.5 nC)
- Low Crss (Typ. 185 pF)
- · 100% Avalanche Tested

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.







### MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQP32N20C	FQPF32N20C	Unit	
V <sub>DSS</sub>	Drain to Source Voltage		200		V	
I <sub>D</sub>	-Continuous (T <sub>C</sub> = 25			28.0	28.0 *	Α
	Drain Current	-Continuous (T <sub>C</sub> = 100°C)	-Continuous (T <sub>C</sub> = 100°C)		17.8 *	Α
$I_{DM}$	Drain Current	- Pulsed	(Note 1)	112	112 *	Α
V <sub>GSS</sub>	Gate to Source Voltage		± 30		V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note		(Note 2)	955		mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	28.0		Α
E <sub>AR</sub>	Repetitive Avalanche Energy		(Note 1)	15.6		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		5.5		V/ns	
$P_{D}$	Power Dissipation	(T <sub>C</sub> = 25°C)		156	50	W
	- Derate above 25°C			1.25	0.4	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150		°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300		°C

<sup>\*</sup>Drain current limited by maximum junction temperature

#### **Thermal Characteristics**

Symbol	Parameter	FQP32N20C	FQPF32N20C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.8	2.51	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	62.5	°C/W

©2004 Fairchild Semiconductor Corporation FQP32N20C / FQPF32N20C Rev. C1

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQP32N20C	FQP32N20C	TO-220	Tube	N/A	50 units
FQPF32N20C	FQPF32N20C	TO-220F	Tube	N/A	50 units

### **Electrical Characteristics** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	200			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C		0.24		V/°C
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			10	μА
I <sub>DSS</sub>		V <sub>DS</sub> = 160 V, T <sub>C</sub> = 125°C			100	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14 A	-	0.068	0.082	Ω
9 <sub>FS</sub>	Forward Transconductance V <sub>DS</sub> = 40 V, I <sub>D</sub> = 14 A			20		S
-	ic Characteristics			4700	0000	
Ciss	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		1700	2220	pF
Coss	Output Capacitance	f = 1.0 MHz		400	520	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			185	245	pF
Switchi	ing Characteristics					
$t_{d(on)}$	Turn-On Delay Time	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 32 A,		25	60	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		270	550	ns
$t_{d(off)}$	Turn-Off Delay Time			245	500	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		210	430	ns
$Q_g$	Total Gate Charge	V <sub>DS</sub> = 160 V, I <sub>D</sub> = 32 A,	/	82.5	110	nC
$Q_{gs}$	Gate-Source Charge	V <sub>GS</sub> = 10 V		10.5		nC
$Q_{gd}$	Gate-Drain Charge	(Note 4)		44.5		nC
Drain-S	Source Diode Characteristics and	l Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				28	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				112	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 28 A			1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 32 A,		265		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dl <sub>F</sub> / dt = 100 A/μs		2.73		μС

#### Notes

- 1. Repetitive Rating : Pulse width limited by maximum junction temperature.
- 2. L = 1.4 mH, I $_{AS}$  = 32 A, V $_{DD}$  = 50 V, R $_{G}$  = 25  $\Omega$ , starting T $_{J}$  = 25°C.
- 3.  $I_{SD} \le 28$  A, di/dt  $\le 300$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J$  = 25°C.
- 4. Essentially independent of operating temperature.

### **Typical Characteristics**

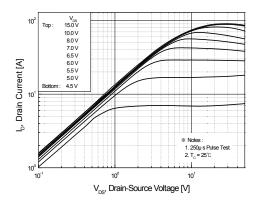


Figure 1. On-Region Characteristics

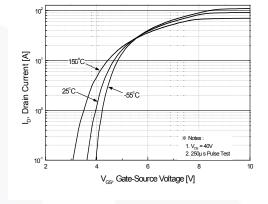


Figure 2. Transfer Characteristics

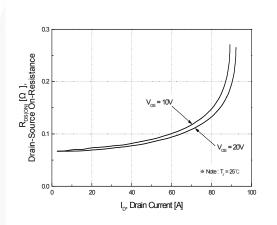


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

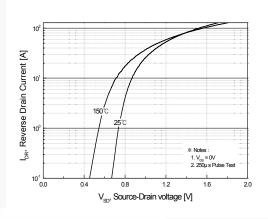


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

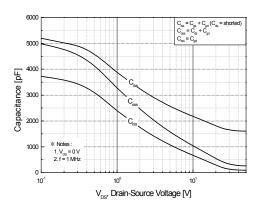


Figure 5. Capacitance Characteristics

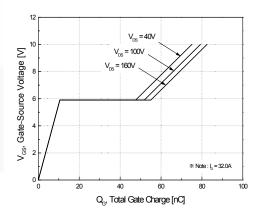


Figure 6. Gate Charge Characteristics

### Typical Characteristics (Continued)

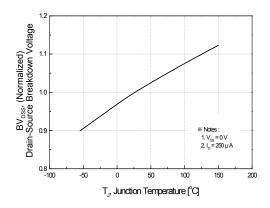


Figure 7. Breakdown Voltage Variation vs Temperature

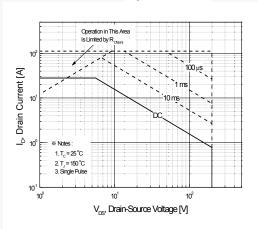


Figure 9-1. Maximum Safe Operating Area for FQP32N20C

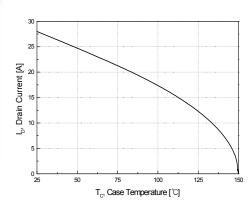


Figure 10. Maximum Drain Current vs Case Temperature

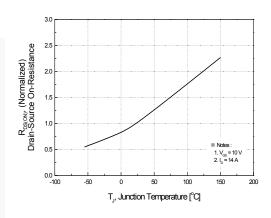


Figure 8. On-Resistance Variation vs Temperature

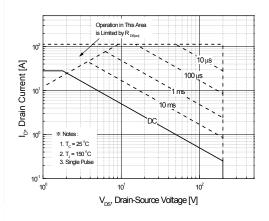


Figure 9-2. Maximum Safe Operating Area for FQPF32N20C

### Typical Characteristics (Continued)

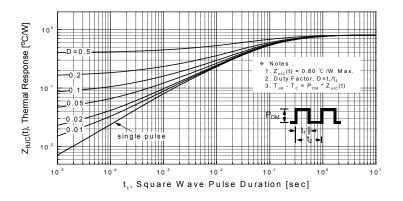


Figure 11-1. Transient Thermal Response Curve for FQP32N20C

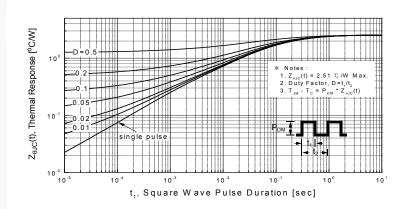


Figure 11-2. Transient Thermal Response Curve for FQPF32N20C

Figure 12. Gate Charge Test Circuit & Waveform

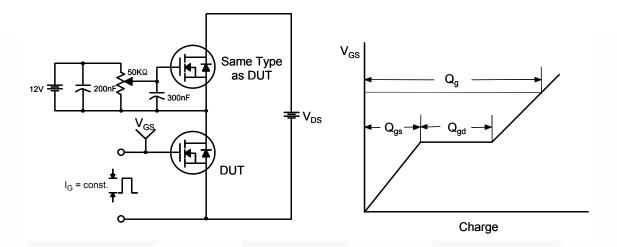


Figure 13. Resistive Switching Test Circuit & Waveforms

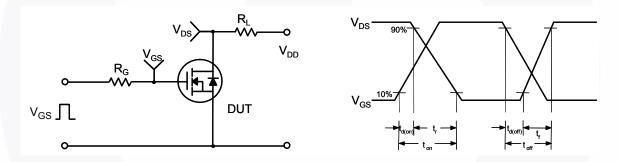
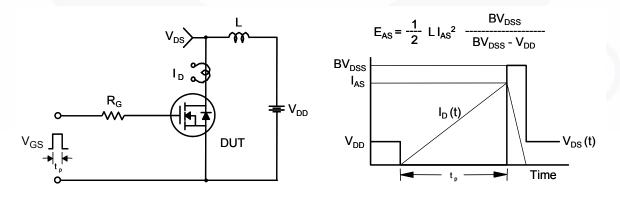
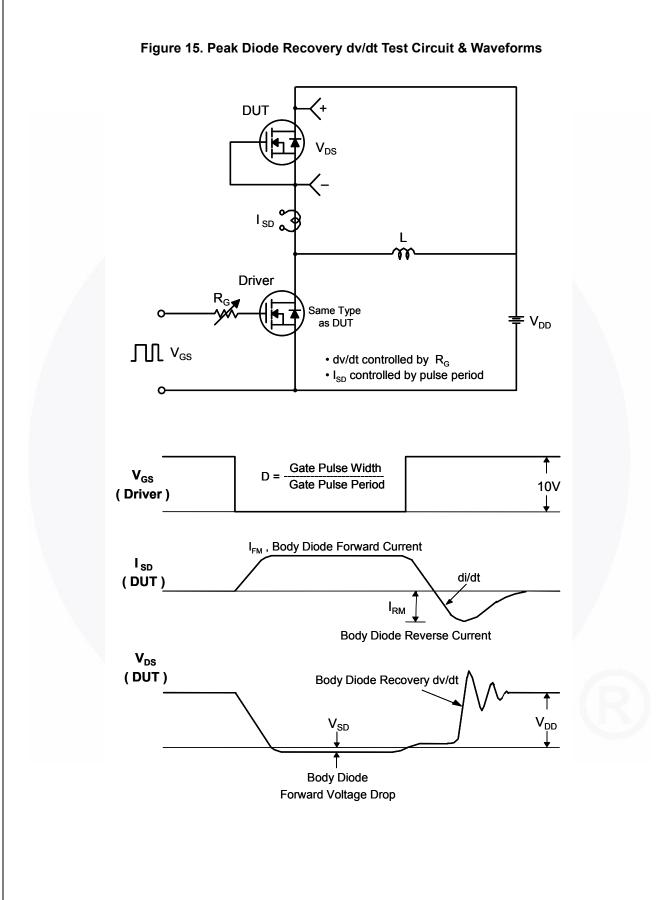


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms





### **Mechanical Dimensions**

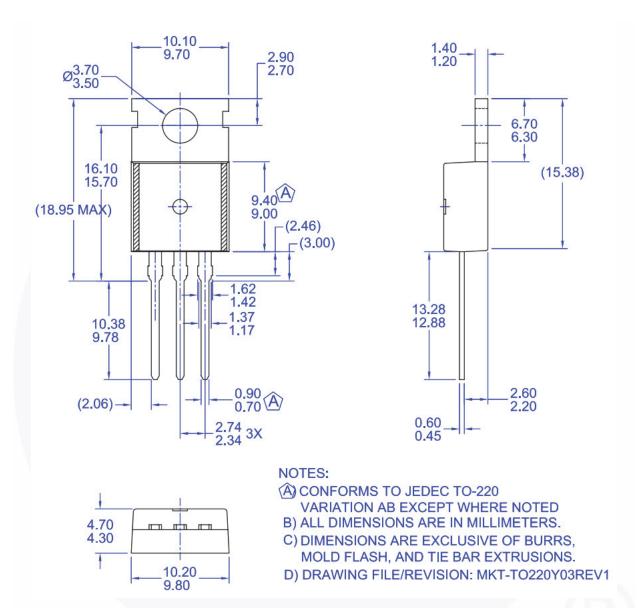


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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### **Mechanical Dimensions**

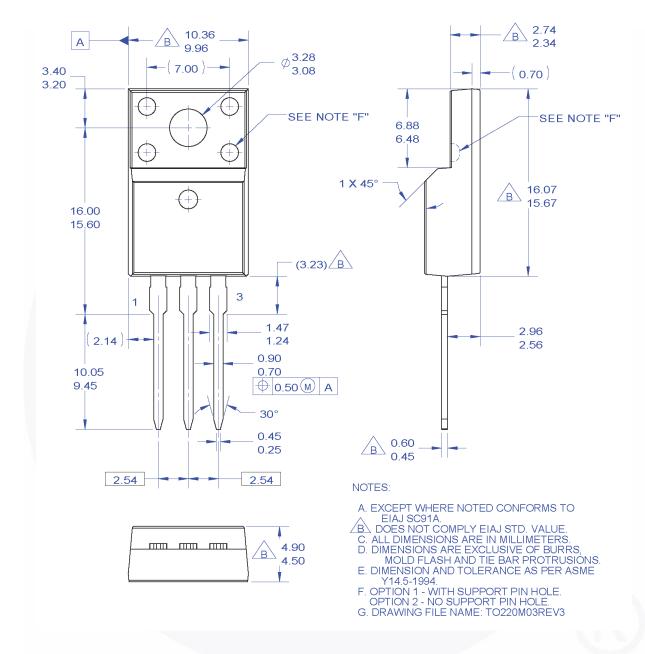


Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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