MOSFET – N-Channel, POWERTRENCH®

75 V, 80 A, 4.7 mΩ

FDH047AN08A0, FDP047AN08A0

ON Semiconductor®

www.onsemi.com

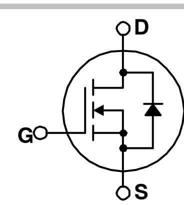
Features

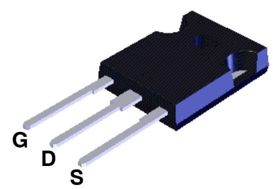
- $R_{DS(ON)}$ = 4.0 mΩ (Typ.), V_{GS} = 10 V, I_D = 80 A
- Q_g (tot) = 92 nC (Typ.), V_{GS} = 10 V
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- This Device is Pb−Free and is RoHS Compliant

Applications

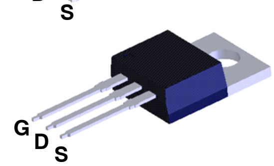
- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
75 V	4.7 mΩ	80 A



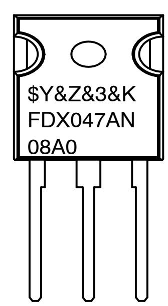


TO−247−3
CASE 340CK



TO−220−3
CASE 340AT

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDX047AN08A0	= Specific Device Code
X	= H/P

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

December, 2019 − Rev. 4

Publication Order Number:
FDH047AN08A0/D

MOSFET MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		75	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	– Continuous (T_C < 144°C, V_{GS} = 10 V)	80	A
		– Continuous (T_C = 25°C, V_{GS} = 10 V, $R_{\theta JA}$ = 62°C/W)	15	
I_D	Drain Current	– Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)		475	mJ
P_D	Power Dissipation		310	W
	Derate Above 25°C		2.0	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T_J = 25°C, L = 0.232 mH, I_{AS} = 64 A.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max. TO−220, TO−247	0.48	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. TO−220 (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. TO−247 (Note 2)	30	°C/W

2. Pulse Width = 100 s.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDH047AN08A0	FDH047AN08A0	TO−247	Tube	N/A	30 Units
FDP047AN08A0	FDP047AN08A0	TO−220	Tube	N/A	50 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	75			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			1	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_C = 150°C			250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0		4.0	V
$R_{DS(ON)}$	Drain to Source On Resistance	I_D = 80 A, V_{GS} = 10 V		0.0040	0.0047	Ω
		I_D = 37 V, V_{GS} = 6 V		0.0058	0.0087	
		I_D = 80 A, V_{GS} = 10 V, T_j = 175 °C		0.0082	0.011	
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		6600		pF
C_{OSS}	Output Capacitance			1000		pF
C_{RSS}	Reverse Transfer Capacitance			240		pF
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 40 V, I_D = 80 A, I_g = 1.0 mA		92	138	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V, V_{DD} = 40 V, I_D = 80 A, I_g = 1.0 mA		11	17	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 40 V, I_D = 80 A, I_g = 1.0 mA		27		nC
Q_{gs2}	Gate Charge Threshold to Plateau			16		nC
Q_{gd}	Gate to Drain “Miller” Charge			21		nC
SWITCHING CHARACTERISTICS (V_{GS} = 10 V)						
t_{ON}	Turn-On Time	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10 V, R_{GS} = 3.3 Ω			160	ns
$t_{d(ON)}$	Turn-On Delay Time			18		ns
t_r	Rise Time			88		ns
$t_{d(OFF)}$	Turn-Off Delay Time			40		ns
t_f	Fall Time			45		ns
t_{OFF}	Turn-Off Time				128	ns
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80 A			1.25	V
		I_{SD} = 40 A			1	V
t_{rr}	Reverse Recovery Time	I_{SD} = 75 A, dI_{SD}/dt = 100 A/μs			53	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 75 A, dI_{SD}/dt = 100 A/μs			54	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_C = 25°C unless otherwise noted)

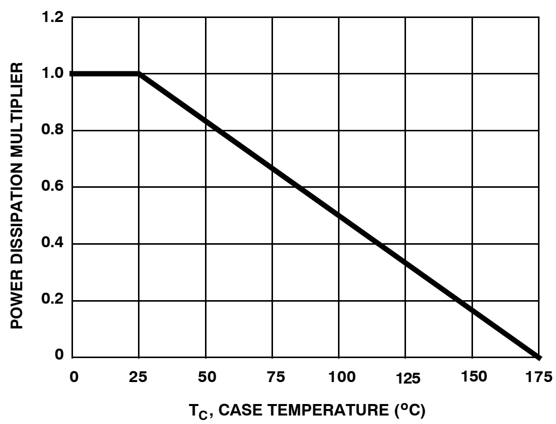


Figure 1. Normalized Power Dissipation vs. Case Temperature

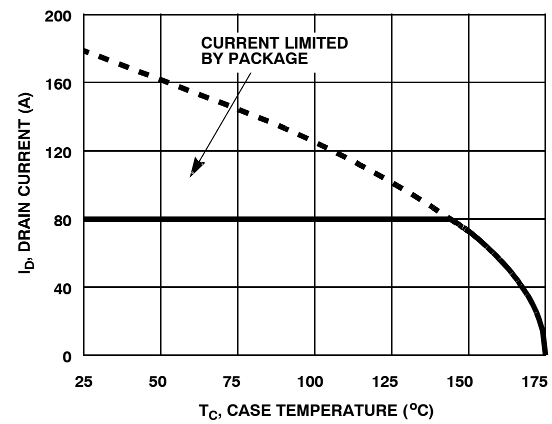


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

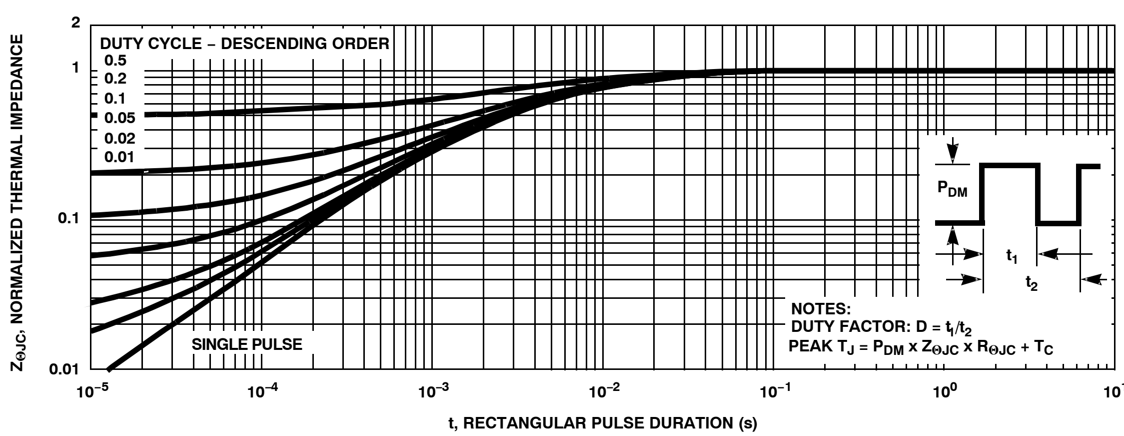


Figure 3. Normalized Maximum Transient Thermal Impedance

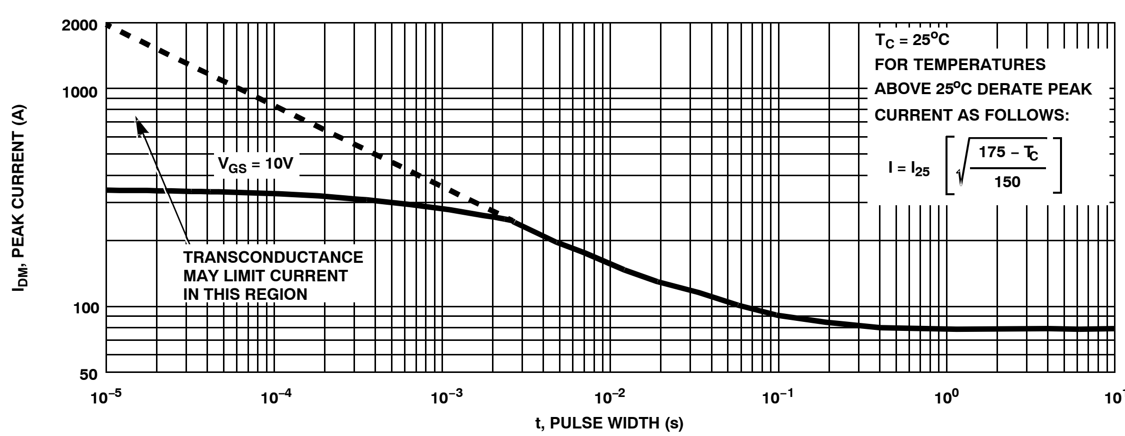


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (Continued)

(T_C = 25°C unless otherwise noted)

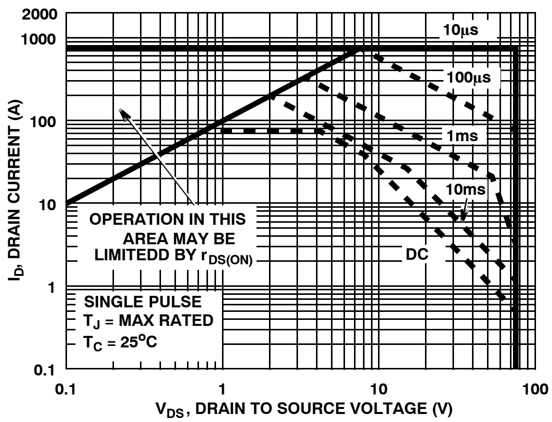


Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to ON Semiconductor Application Notes AN−7514 and AN−7515

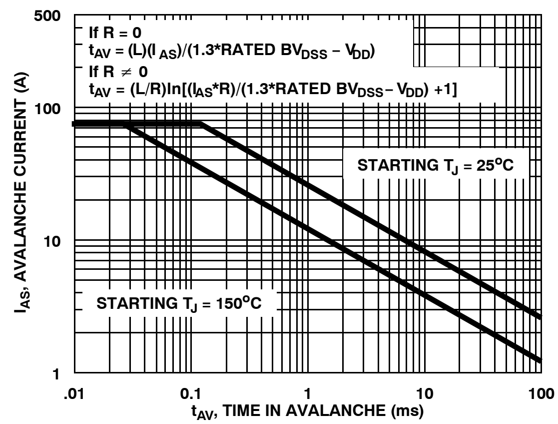


Figure 6. Unclamped Inductive Switching Capability

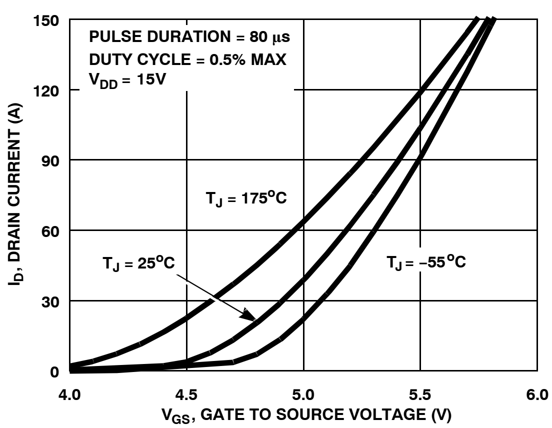


Figure 7. Transfer Characteristics

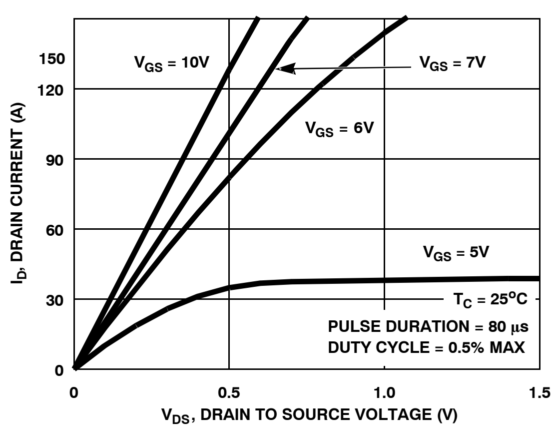


Figure 8. Saturation Characteristics

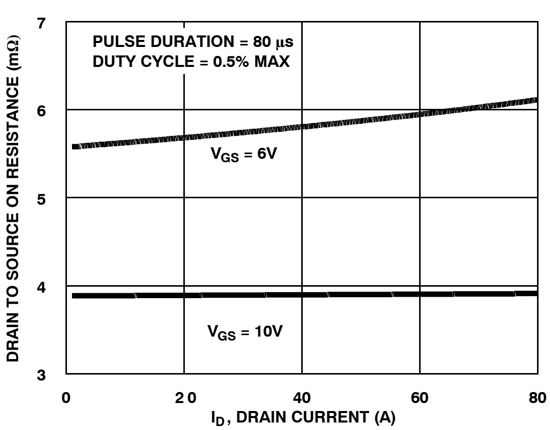


Figure 9. Drain to Source On Resistance vs. Drain Current

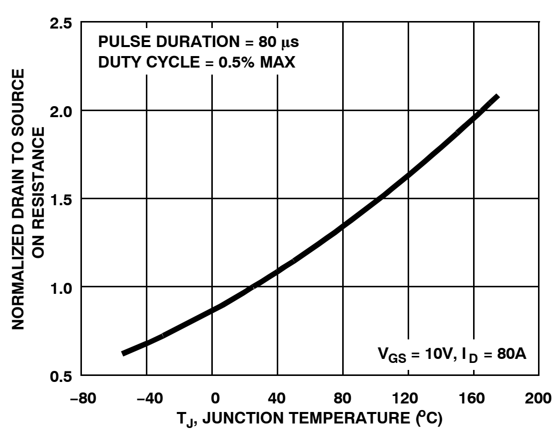


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (Continued)

(T_C = 25°C unless otherwise noted)

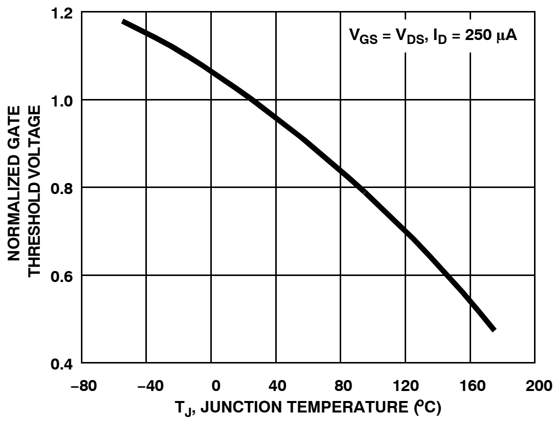


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

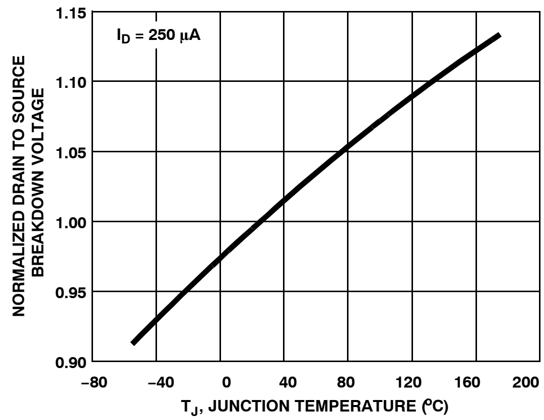


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

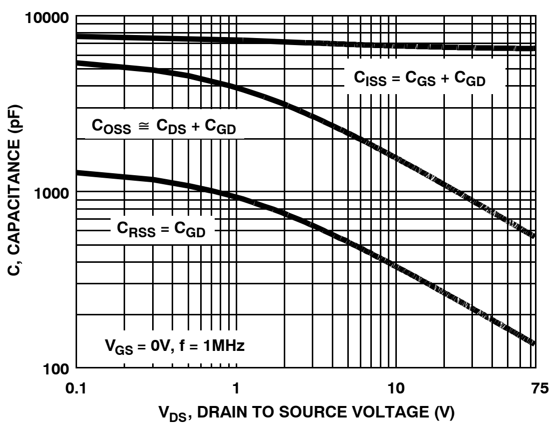


Figure 13. Capacitance vs. Drain to Source Voltage

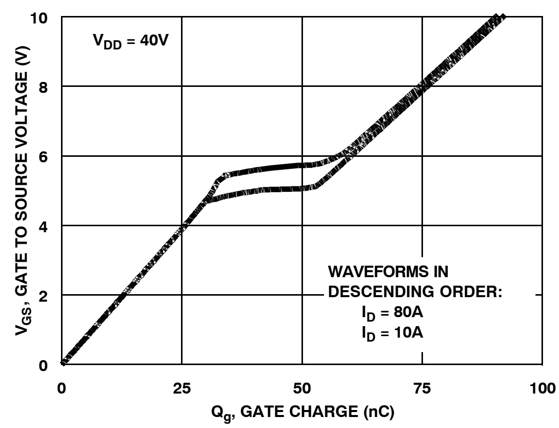


Figure 14. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS AND WAVEFORMS

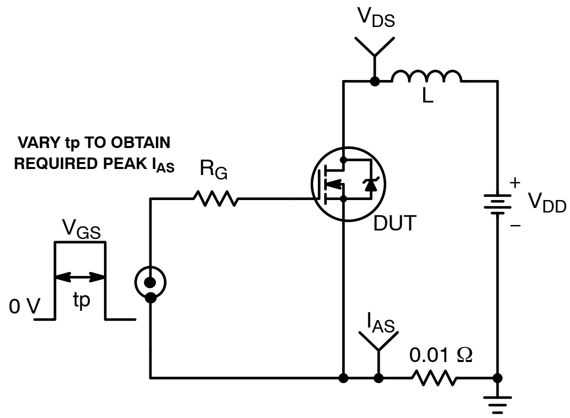


Figure 15. Unclamped Energy Test Circuit

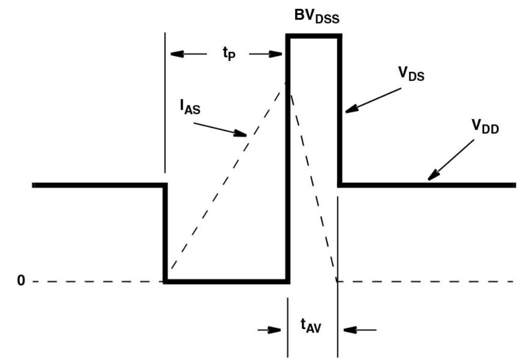


Figure 16. Unclamped Energy Waveforms

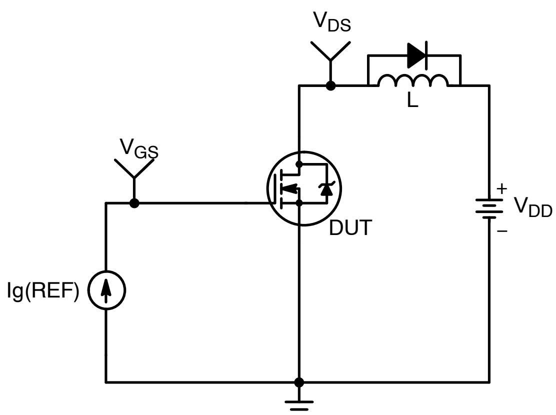


Figure 17. Gate Charge Test Circuit

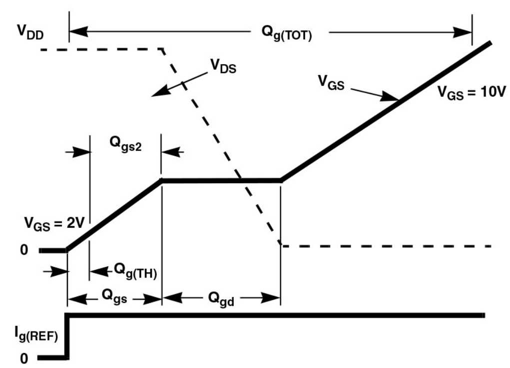


Figure 18. Gate Charge Waveforms

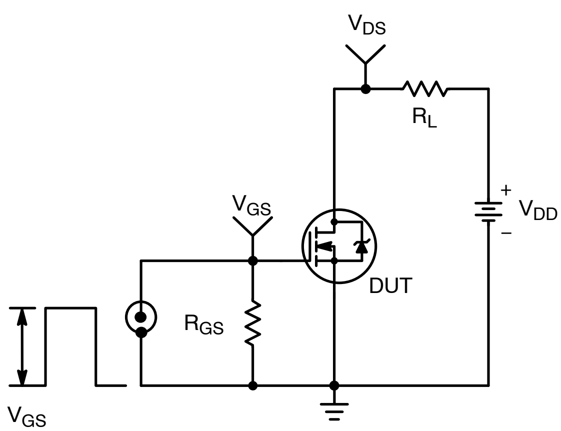


Figure 19. Switching Time Test Circuit

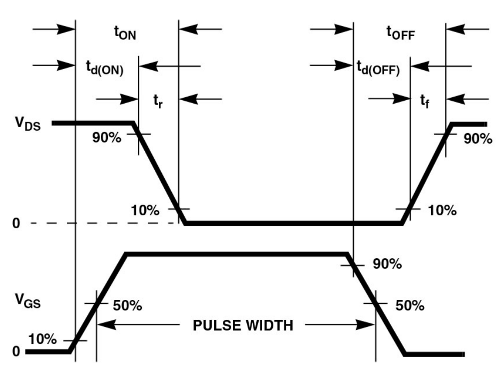


Figure 20. Switching Time Waveforms

PSPICE Electrical Model

```
.SUBCKT FDP047AN08A0 2 1 3 ; rev March 2002
CA 12 8 1.5e−9
CB 15 14 1.5e−9
CIN 6 8 6.4e−9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 82.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e−9
LGATE 1 9 4.81e−9
LSOURCE 3 7 4.63e−9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 9e−4
RGATE 9 20 1.36
RLDRAIN 2 5 10
RLGATE 1 9 48.1
RLSOURCE 3 7 46.3
RSLC1 5 51 RSLCMOD 1e−6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 2.3e−3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e−6*250),10))}

.MODEL DBODYMOD D (IS = 2.4e−11 N = 1.04 RS = 1.76e−3 TRS1 = 2.7e−3 TRS2 = 2e−7 XTI=3.9 CJO = 4.35e−9
TT = 1e−8 M = 5.4e−1)
.MODEL DBREAKMOD D (RS = 1.5e−1 TRS1 = 1e−3 TRS2 = −8.9e−6)
.MODEL DPLCAPMOD D (CJO = 1.35e−9 IS = 1e−30 N = 10 M = 0.53)
.MODEL MMEDMOD NMOS (VTO = 3.7 KP = 9 IS =1e−30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.36)
.MODEL MSTROMOD NMOS (VTO = 4.4 KP = 250 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 3.05 KP = 0.03 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.36e1 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.05e−3 TC2 = −9e−7)
.MODEL RDRAINMOD RES (TC1 = 1.9e−2 TC2 = 4e−5)
.MODEL RSLCMOD RES (TC1 = 1.3e−3 TC2 = 1e−5)
.MODEL RSOURCEMOD RES (TC1 = 1e−3 TC2 = 1e−6)
```

.MODEL RVTHRESMOD RES (TC1 = −6e−3 TC2 = −1.9e−5)
.MODEL RVTEMPMOD RES (TC1 = −2.4e−3 TC2 = 1e−6)

.MODEL S1AMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −4.0 VOFF= −1.5)
.MODEL S1BMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −1.5 VOFF= −4.0)
.MODEL S2AMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −1.0 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = 0.5 VOFF= −1.0)

.ENDS

NOTE: For further discussion of the PSPICE model, consult A New PSPICE Sub−Circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

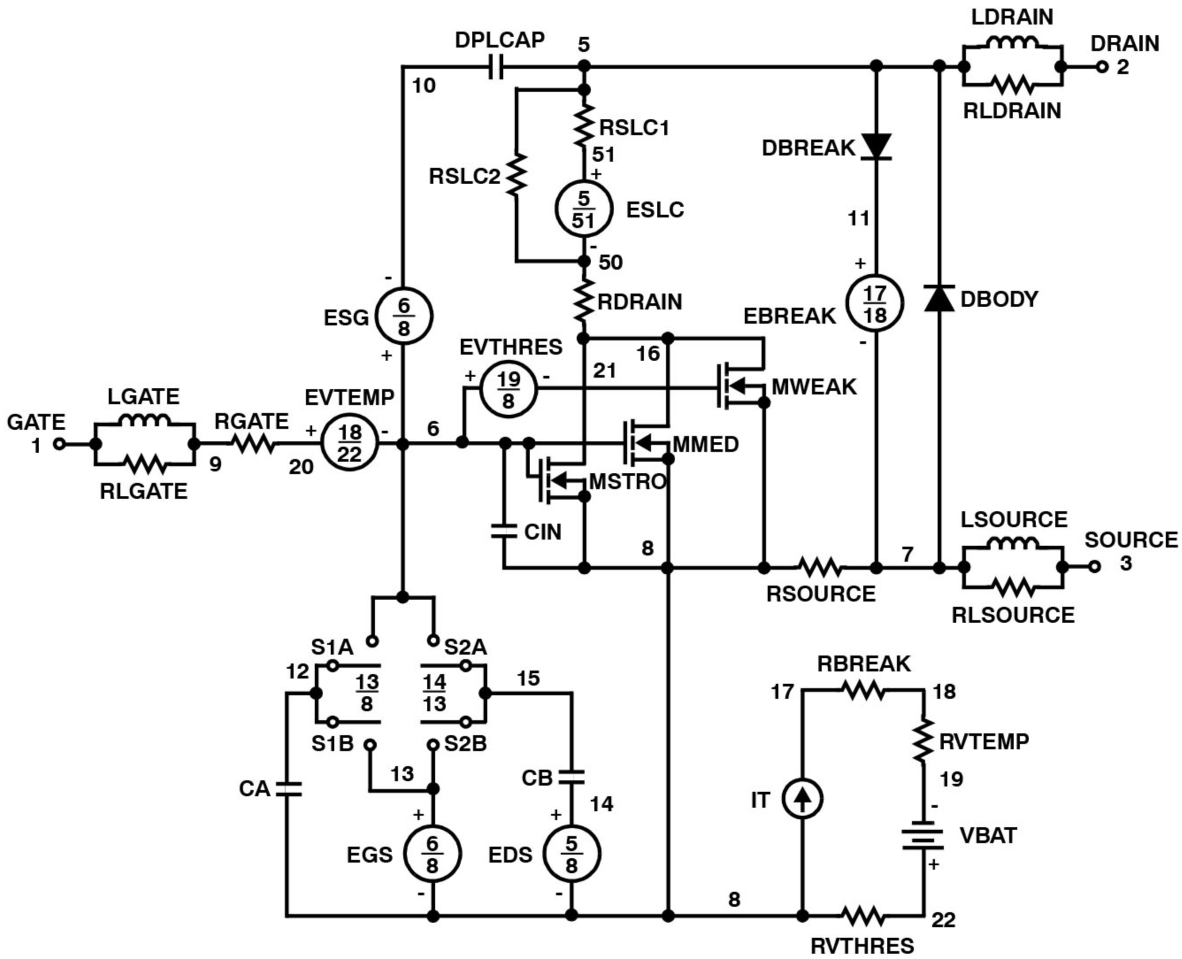


Figure 21. PSPICE Electrical Model

SABER Electrical Model

```
REV March 2002
template FDP047AN08A0 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl = 2.4e−11, n1 = 1.04, rs = 1.76e−3, trs1 = 2.7e−3, trs2 = 2e−7, xti = 3.9, cjo = 4.35e−9, tt = 1e−8,
m = 5.4e−1)
dp..model dbreakmod = (rs = 1.5e−1, trs1 = 1e−3, trs2 = −8.9e−6)
dp..model dplcapmod = (cjo = 1.35e−9, isl =10e−30, nl =10, m = 0.53)
m..model mmedmod = (type=_n, vto = 3.7, kp = 9, is =1e−30, tox=1)
m..model mstrongmod = (type=_n, vto = 4.4, kp = 250, is = 1e−30, tox = 1)
m..model mweakmod = (type=_n, vto = 3.05, kp = 0.03, is = 1e−30, tox = 1, rs=0.1)
sw_vcsp..model s1amod = (ron = 1e−5, roff = 0.1, von = −4.0, voff = −1.5)
sw_vcsp..model s1bmod = (ron =1e−5, roff = 0.1, von = −1.5, voff = −4.0)
sw_vcsp..model s2amod = (ron = 1e−5, roff = 0.1, von = −1.0, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e−5, roff = 0.1, von = 0.5, voff = −1.0)

c.ca n12 n8 = 1.5e−9
c.cb n15 n14 = 1.5e−9
c.cin n6 n8 = 6.4e−9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e−9
l.lgate n1 n9 = 4.81e−9
l.lsource n3 n7 = 4.63e−9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1 = 1.05e−3, tc2 = −9e−7
res.rdrain n50 n16 = 9e−4, tc1 = 1.9e−2, tc2 = 4e−5
res.rgate n9 n20 = 1.36
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 48.1
res.rlsource n3 n7 = 46.3
res.rslc1 n5 n51= 1e−6, tc1 = 1e−3, tc2 =1e−5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 2.3e−3, tc1 = 1e−3, tc2 =1e−6
res.rvtemp n18 n19 = 1, tc1 = −2.4e−3, tc2 = 1e−6
res.rvthres n22 n8 = 1, tc1 = −6e−3, tc2 = −1.9e−5

spe.ebreak n11 n7 n17 n18 = 82.3
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
```

```
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51−>n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e−9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/250))** 10))
}
}
```

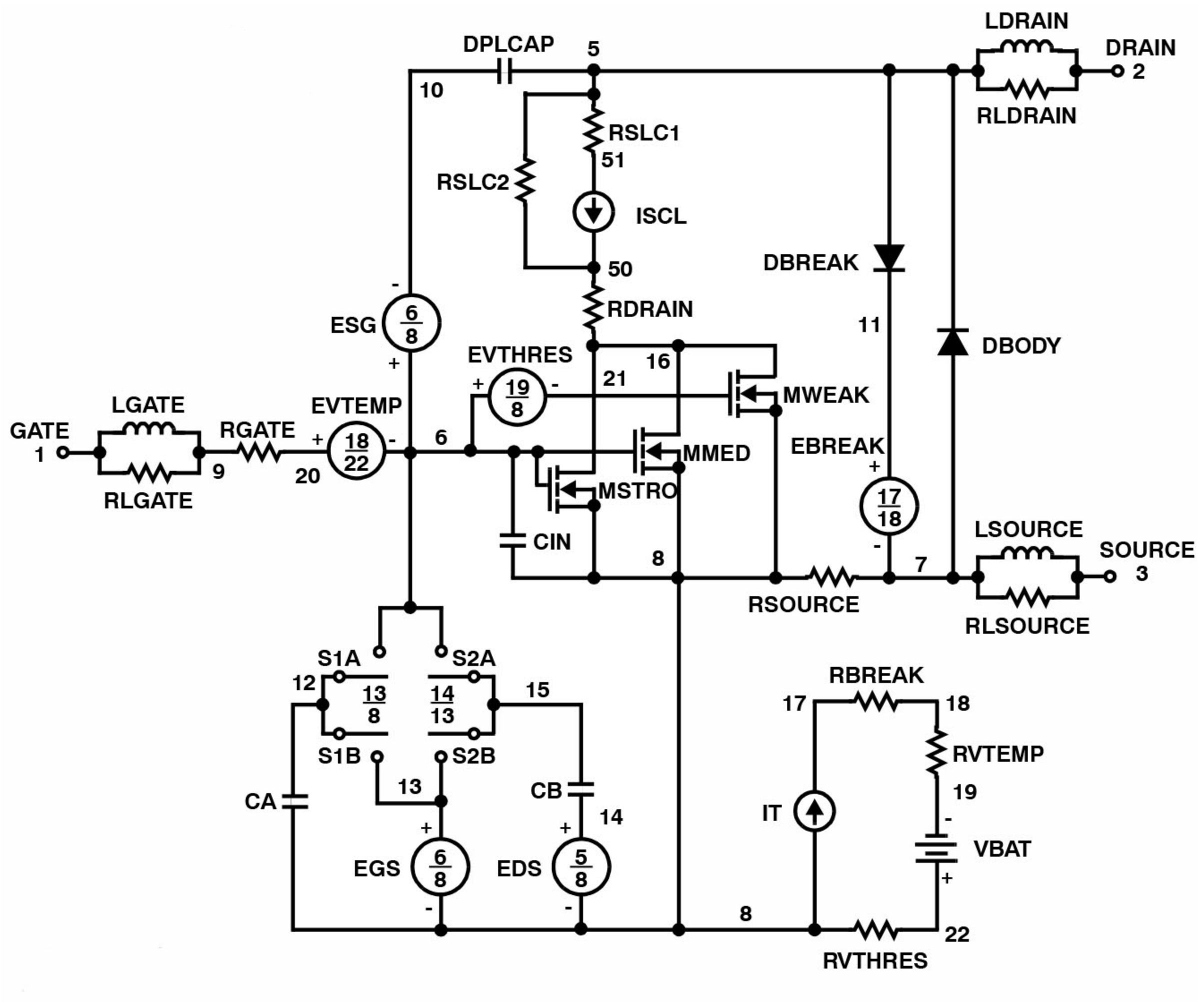


Figure 22. SABER Electrical Model

SPICE Thermal Model

REV 23 March 2002

FDP047AN08A0T

CTHERM1 th 6 6.45e−3
CTHERM2 6 5 3e−2
CTHERM3 5 4 1.4e−2
CTHERM4 4 3 1.65e−2
CTHERM5 3 2 4.85e−2
CTHERM6 2 tl 1e−1

RTHERM1 th 6 3.24e−3
RTHERM2 6 5 8.08e−3
RTHERM3 5 4 2.28e−2
RTHERM4 4 3 1e−1
RTHERM5 3 2 1.1e−1
RTHERM6 2 tl 1.4e−1

SABER Thermal Model

SABER thermal model FDP047AN08A0T
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 6.45e−3
ctherm.ctherm2 6 5 = 3e−2
ctherm.ctherm3 5 4 = 1.4e−2
ctherm.ctherm4 4 3 = 1.65e−2
ctherm.ctherm5 3 2 = 4.85e−2
ctherm.ctherm6 2 tl = 1e−1

rtherm.rtherm1 th 6 = 3.24e−3
rtherm.rtherm2 6 5 = 8.08e−3
rtherm.rtherm3 5 4 = 2.28e−2
rtherm.rtherm4 4 3 = 1e−1
rtherm.rtherm5 3 2 = 1.1e−1
rtherm.rtherm6 2 tl = 1.4e−1
}

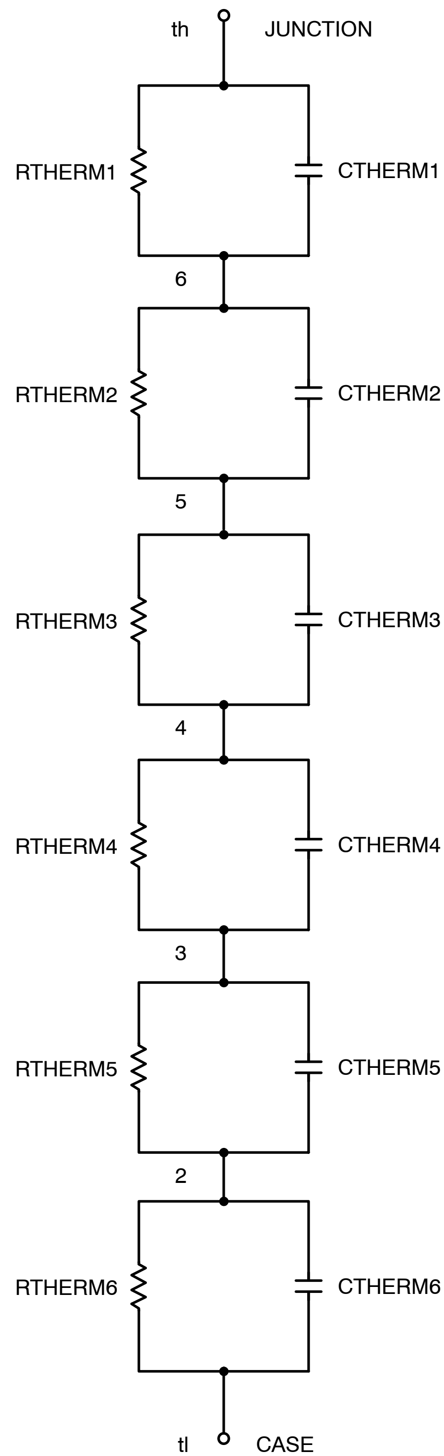
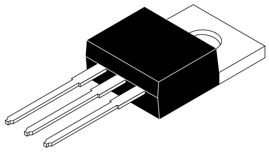


Figure 23. Thermal Model



Scale 1:1

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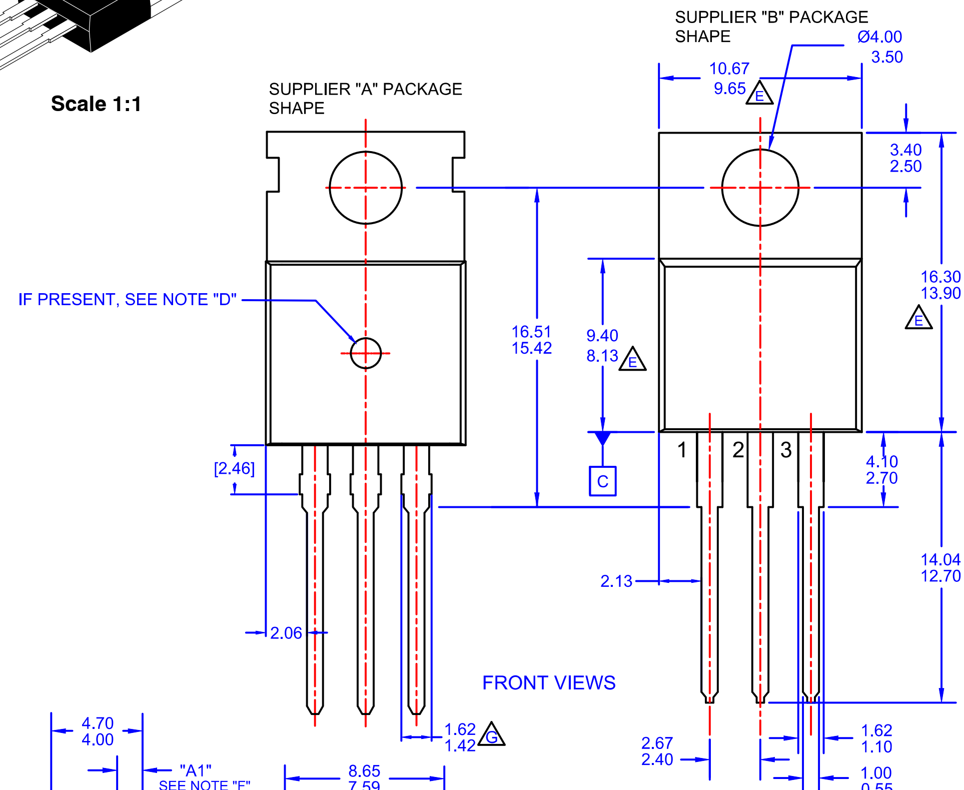

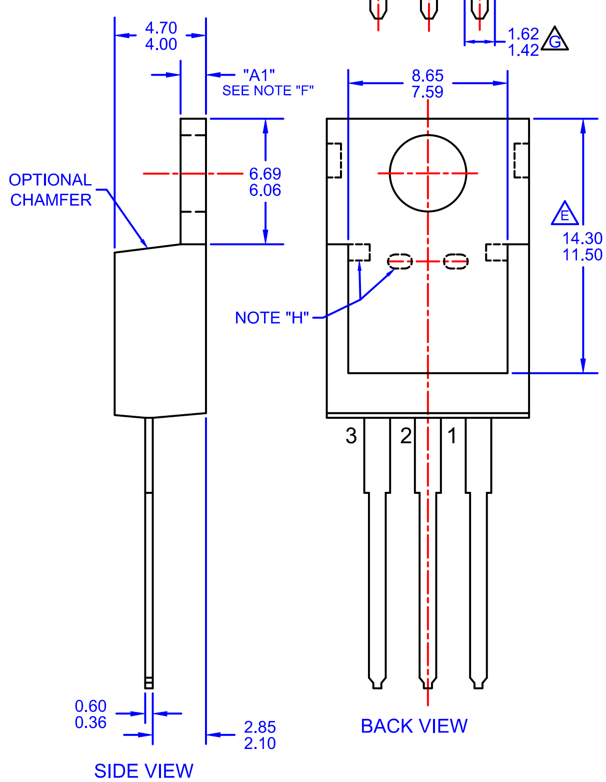

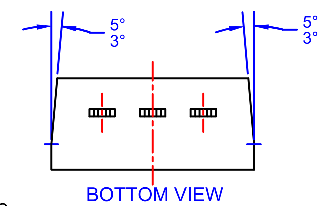

NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E) DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
  - SINGLE GAUGE = 0.51 - 0.61
  - DUAL GAUGE = 1.10 - 1.45
- G) PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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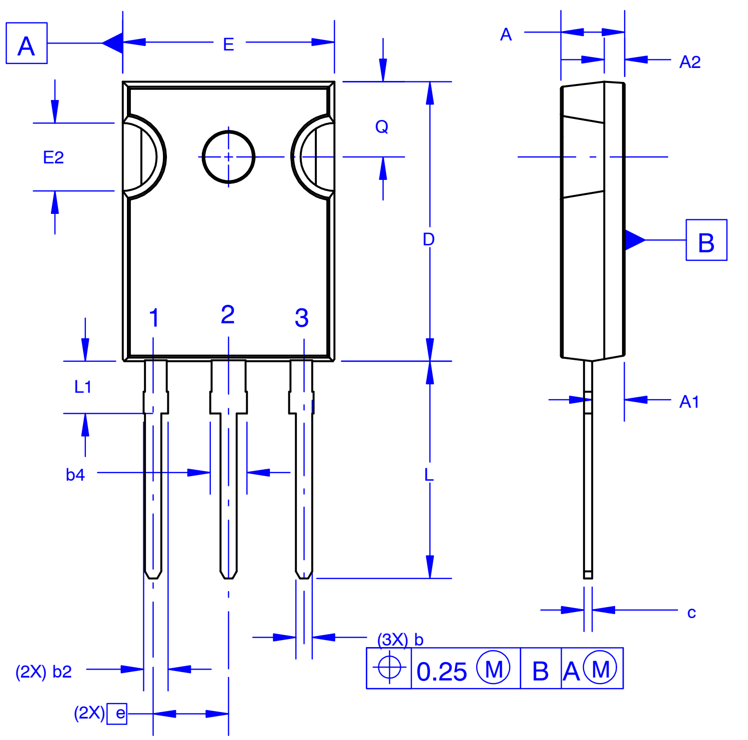
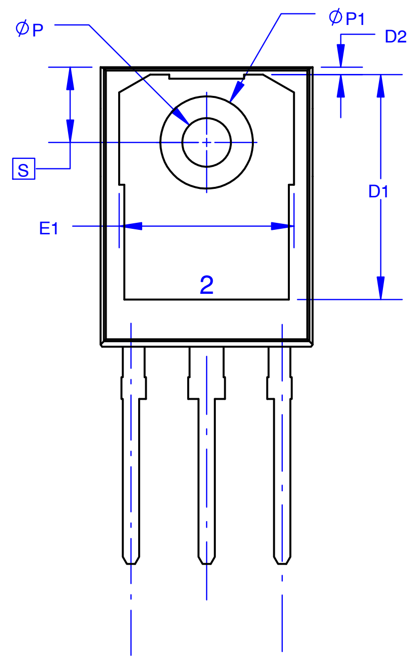
DATE 31 JAN 2019





NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

GENERIC MARKING DIAGRAM*

AYWWZZ
XXXXXXX
XXXXXXX
∘

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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