NVD5C632NL

[MOSFET](#) – Power, Single N-Channel

60 V, 2.5 mΩ, 155 A

Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	2.5 mΩ @ 10 V	155 A
	3.4 mΩ @ 4.5 V	

N−CHANNEL MOSFET

DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM
& PIN ASSIGNMENT

A	= Assembly Location
Y	= Year
WW	= Work Week
5C632L	= Device Code
G	= Pb−Free Package

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	T_C = 25°C	I_D	155	A
		T_C = 100°C		110	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	115	W
		T_C = 100°C		58	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	T_A = 25°C	I_D	29	A
		T_A = 100°C		21	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25°C	P_D	4	W
		T_A = 100°C		2	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	96	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 14.4 A)			E_{AS}	363	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

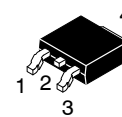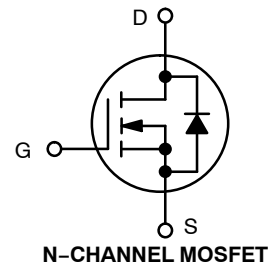| Parameter	Symbol	Value	Unit
Junction−to−Case (Drain) (Note 1)	$R_{\theta JC}$	1.3	°C/W
Junction−to−Ambient – Steady State (Note 2)	$R_{\theta JA}$	37	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.
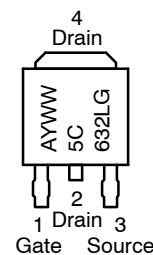
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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NVD5C632NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				24		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			10	µA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 µA		1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.8		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A			2.1	2.5	mΩ
		V_{GS} = 4.5 V, I_D = 50 A			2.7	3.4	
Forward Transconductance	g_{FS}	V_{DS} = 3 V, I_D = 50 A			185		S
CHARGES, CAPACITANCES AND GATE RESISTANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			5700		pF
Output Capacitance	C_{oss}				2800		
Reverse Transfer Capacitance	C_{rss}				36		
Total Gate Charge	$Q_{G(TOT)}$	V_{DS} = 48 V, I_D = 50 A	V_{GS} = 4.5 V		34		nC
			V_{GS} = 10 V		78		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 50 A			34.0		nC
Threshold Gate Charge	$Q_{G(TH)}$				9.5		
Gate−to−Source Charge	Q_{GS}				16.8		
Gate−to−Drain Charge	Q_{GD}				6.1		
Plateau Voltage	V_{GP}				3.1		V
Gate Resistance	R_G				0.7		Ω
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 50 A, R_G = 2.5 Ω			20		ns
Rise Time	t_r				126		
Turn−Off Delay Time	$t_{d(off)}$				65		
Fall Time	t_f				121		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/µs, I_S = 50 A			71		ns
Charge Time	ta				36		
Discharge Time	tb				36		
Reverse Recovery Charge	Q_{RR}				110		nC

4. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

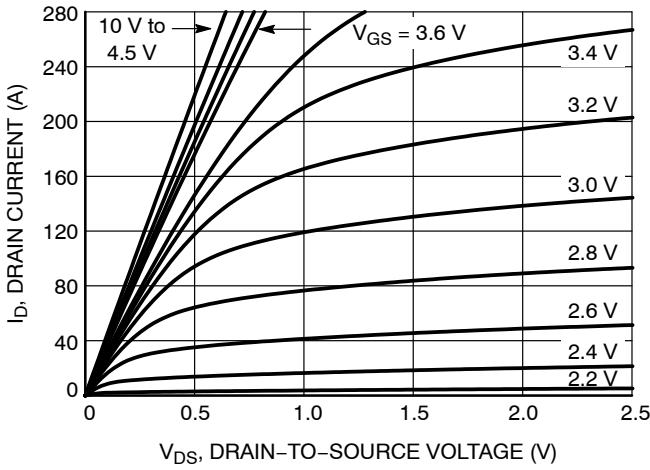# NVD5C632NL

TYPICAL CHARACTERISTICS
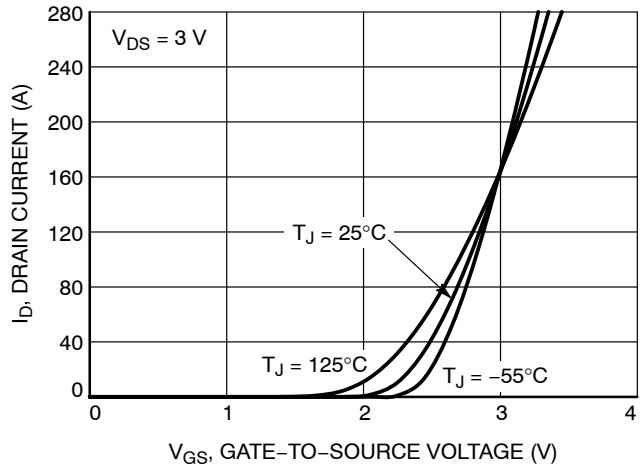

Figure 1. On−Region Characteristics

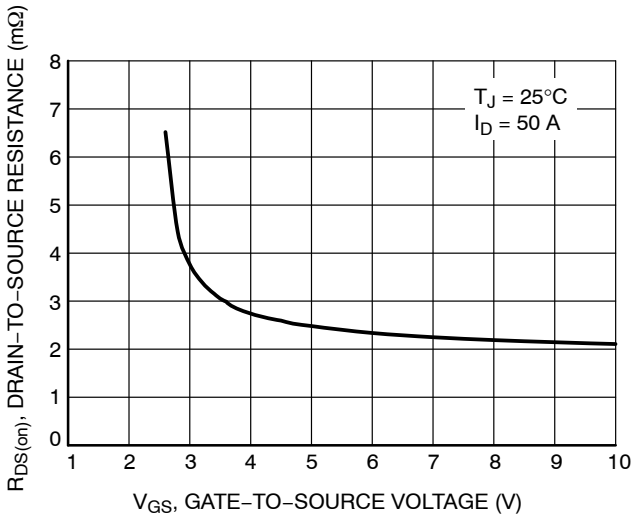Figure 2. Transfer Characteristics

Figure 3. On−Resistance vs. Gate−to−Source Voltage
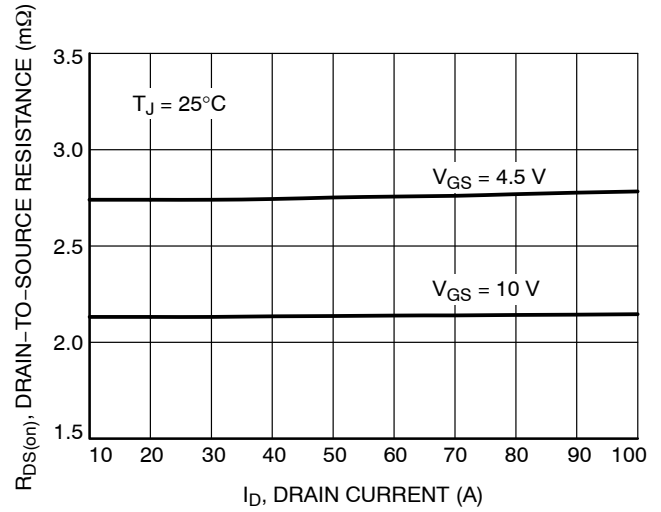

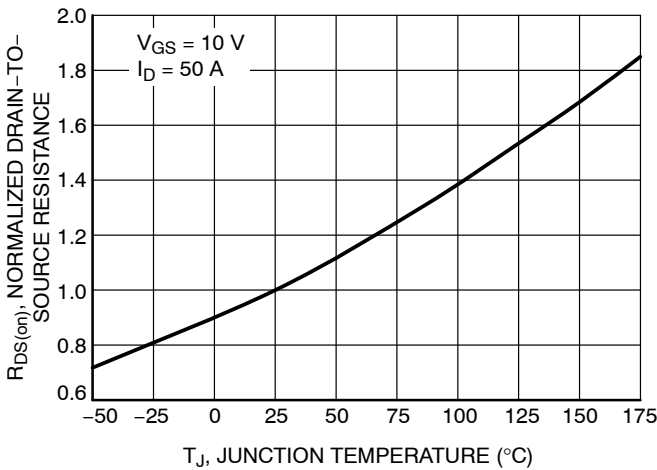
Figure 4. On−Resistance vs. Drain Current and Gate Voltage

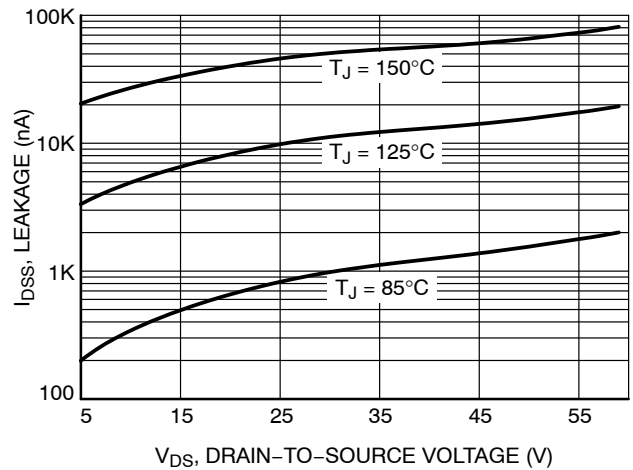Figure 5. On−Resistance Variation with Temperature

Figure 6. Drain−to−Source Leakage Current vs. Voltage

NVD5C632NL

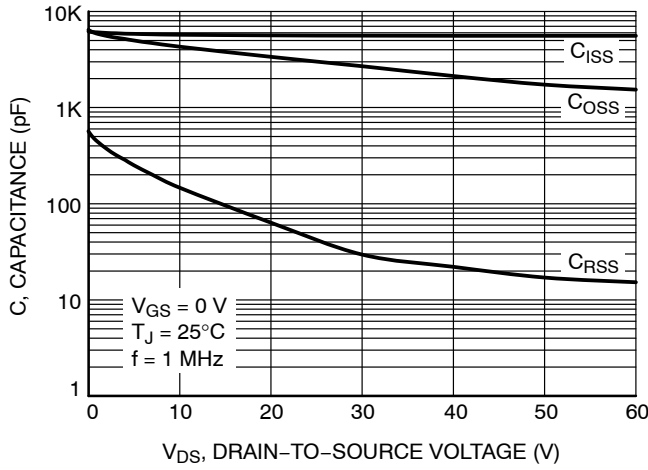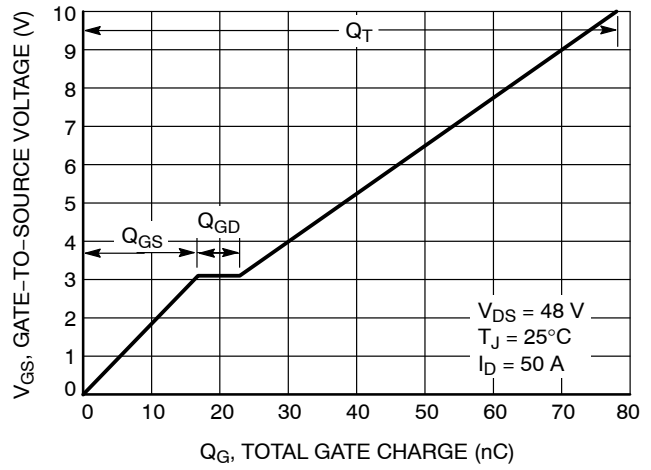## TYPICAL CHARACTERISTICS

Figure 7. Capacitance Variation
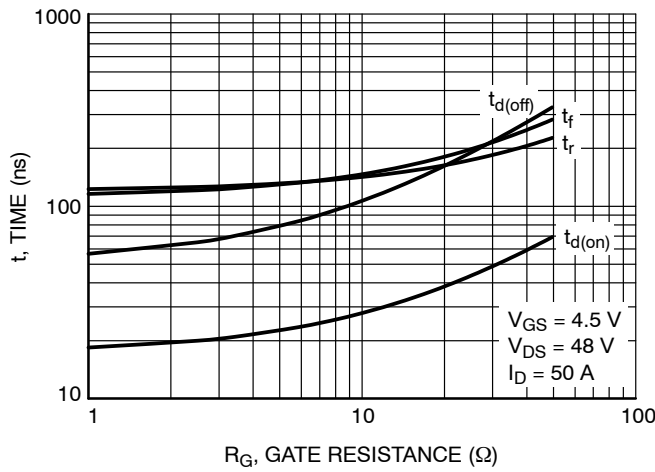

Figure 8. Gate−to−Source Voltage vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance
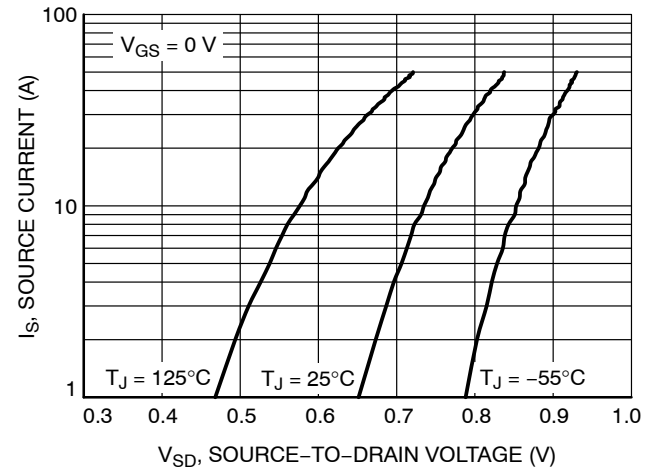
Figure 10. Diode Forward Voltage vs. Current
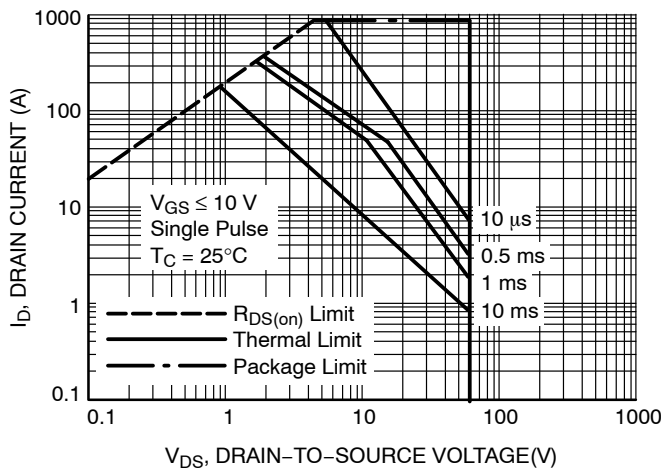
Figure 11. Maximum Rated Forward Biased Safe Operating Area
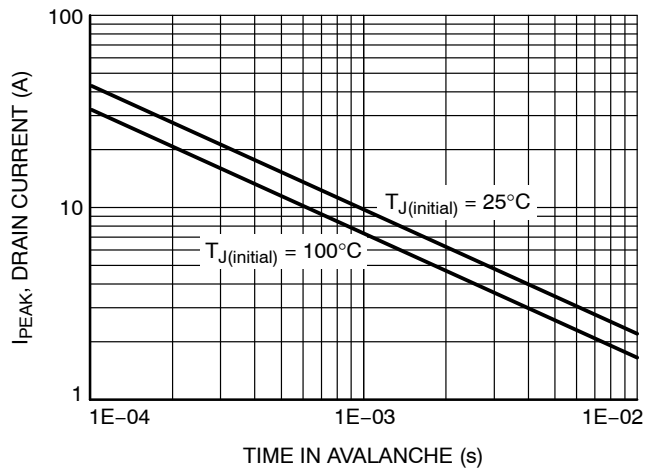
Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS
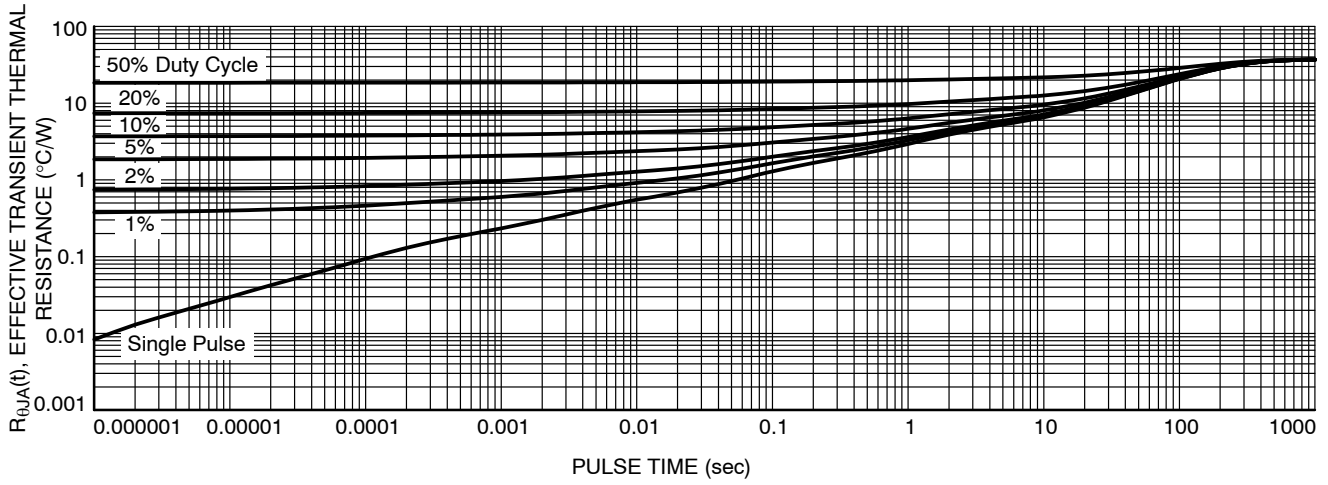
Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping[†]
NVD5C632NLT4G	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

onsemi
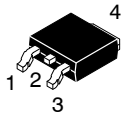
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

DATE 21 JUL 2015

SCALE 1:1

NOTE 7

TOP VIEW

$\oplus$ | 0.005 (0.13) Ⓜ | C

DETAIL A

SIDE VIEW

BOTTOM VIEW

GAUGE PLANE
SEATING PLANE

DETAIL A
ROTATED 90° CW

BOTTOM VIEW
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

XXXXXXG
ALYWW

IC

AYWW
XXX
XXXXXG

Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*

6.20 / 0.244

3.00 / 0.118

2.58 / 0.102

5.80 / 0.228

1.60 / 0.063

6.17 / 0.243

SCALE 3:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON10527D	
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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PUBLICATION ORDERING INFORMATION

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