NTLGD3502N

MOSFET – Power, Dual, N-Channel, DFN6 3X3 mm
20 V, 5.8 A/4.6 A

Features

- Exposed Drain Package
- Excellent Thermal Resistance for Superior Heat Dissipation
- Low Threshold Levels
- Low Profile (< 1 mm) Allows It to Fit Easily into Extremely Thin Environments
- This is a Pb−Free Device

Applications

- DC−DC Converters (Buck and Boost Circuits)
- Power Supplies
- Hard Disk Drives

MOSFET I MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	4.3	A
		T_A = 85°C		3.0	
	t ≤ 5.0 s	T_A = 25°C		5.8	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.74	W
Pulsed Drain Current		t ≤10 μs	I_{DM}	17.2	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	1.6	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

MOSFET II MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	3.6	A
		T_A = 85°C		2.5	
	t ≤ 5.0 s	T_A = 25°C		4.6	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.74	W
Pulsed Drain Current		t ≤10 μs	I_{DM}	13.8	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	1.7	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)

ON Semiconductor®

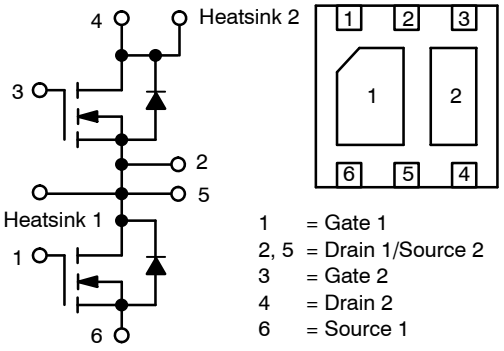
http://onsemi.com

MOSFET I

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
20 V	60 mΩ @ 4.5 V	5.8 A

MOSFET II

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
20 V	90 mΩ @ 4.5 V	4.6 A



1 = Gate 1
2, 5 = Drain 1/Source 2
3 = Gate 2
4 = Drain 2
6 = Source 1

MARKING DIAGRAMS

DFN6
CASE 506AG

3502 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTLGD3502NT1G	DFN6 (Pb−free)	3000/Tape & Reel
NTLGD3502NT2G	DFN6 (Pb−free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm^2, 1 oz. Cu

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	72	°C/W
Junction–to–Ambient – t ≤ 5 s (Note 1)	$R_{\theta JA}$	40	
Junction–to–Ambient – Steady State min Pad (Note 2)	$R_{\theta JA}$	110	
Junction–to–Ambient – Pulsed (25% duty cycle) min Pad (Note 2)	$R_{\theta JA}$	60	

MOSFET I ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Off Characteristics							
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		20			V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			10		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate–to–Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
On Characteristics (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0	1.7	2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				–4.4		mV/°C
Drain–to–Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.3 A			50	60	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 4.0 A			5.9		S
Charges, Capacitances & Gate Resistance							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 10 V			250	480	pF
Output Capacitance	C_{OSS}				138	200	
Reverse Transfer Capacitance	C_{RSS}				52	90	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V; I_D = 4.3 A (Note 3)			2.9	4.0	nC
Gate–to–Source Charge	Q_{GS}				1.0		
Gate–to–Drain Charge	Q_{GD}				1.1		
Gate Resistance	R_G				1.5		Ω
Switching Characteristics, V_{GS} = 4.5 V (Note 4)							
Turn–On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 4.3 A, R_G = 10 Ω			7.0	12	ns
Rise Time	t_r				17.5	25	
Turn–Off Delay Time	$t_{d(OFF)}$				8.6	15	
Fall Time	t_f				3.3	5.0	
Drain–Source Diode Characteristics							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.6 A	T_J = 25°C		0.78	1.2	V
			T_J = 125°C		0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{ISD}/d_t = 100 A/μs, I_S = 1.0 A			16.7		ns
Charge Time	t_a				8.2		
Discharge Time	t_b				8.5		
Reverse Recovery Charge	Q_{RR}				7.0		nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
4. Switching characteristics are independent of operating junction temperatures

MOSFET II ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Off Characteristics							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			22		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25°C			1	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V				±100	nA
On Characteristics (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		0.6		2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−2.8		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 3.4 A			70	90	mΩ
		V_{GS} = 2.5 V, I_D = 1.7 A			95	120	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 3.4 A			6.7		S
Charges, Capacitances & Gate Resistance							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 10 V			144	275	pF
Output Capacitance	C_{OSS}				67	125	
Reverse Transfer Capacitance	C_{RSS}				22	40	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V; I_D = 3.4 A			2.1	5.0	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.11		
Gate−to−Source Charge	Q_{GS}				0.42		
Gate−to−Drain Charge	Q_{GD}				0.7		
Switching Characteristics, V_{GS} = 4.5 V (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 16 V, I_D = 3.4 A, R_G = 10 Ω			4.8	10	ns
Rise Time	t_r				13.6	25	
Turn−Off Delay Time	$t_{d(OFF)}$				9.0	20	
Fall Time	t_f				1.9	5.0	
Drain−Source Diode Characteristics							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.7 A	T_J = 25°C		0.8	1.15	V
			T_J = 150°C		0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{ISD}/d_t = 100 A/μs, I_S = 1.0 A			12		ns
Charge Time	t_a				8.0		
Discharge Time	t_b				4.0		
Reverse Recovery Charge	Q_{RR}				5.0		nC

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

TYPICAL MOSFET I N−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

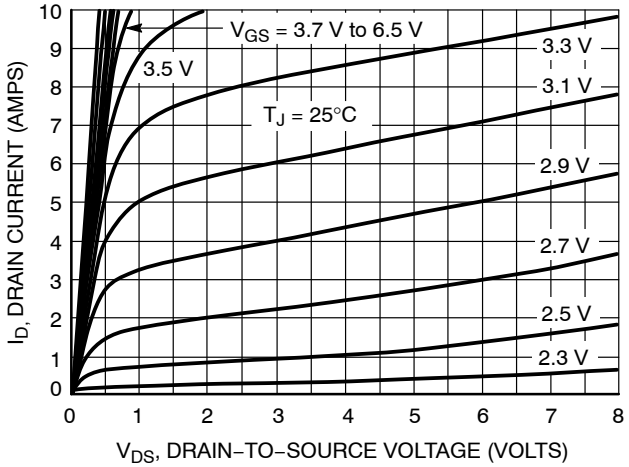


Figure 1. On−Region Characteristics

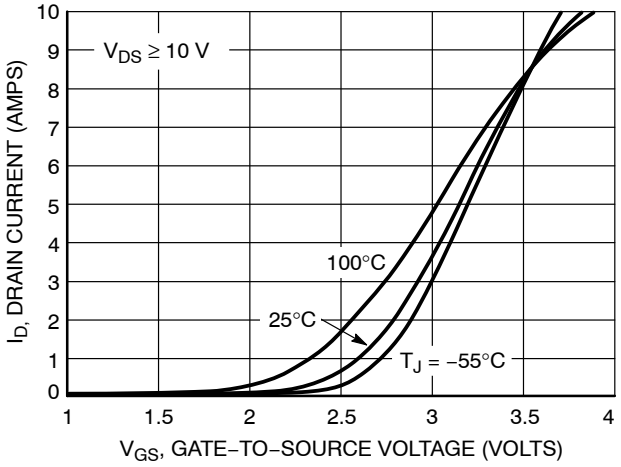


Figure 2. Transfer Characteristics

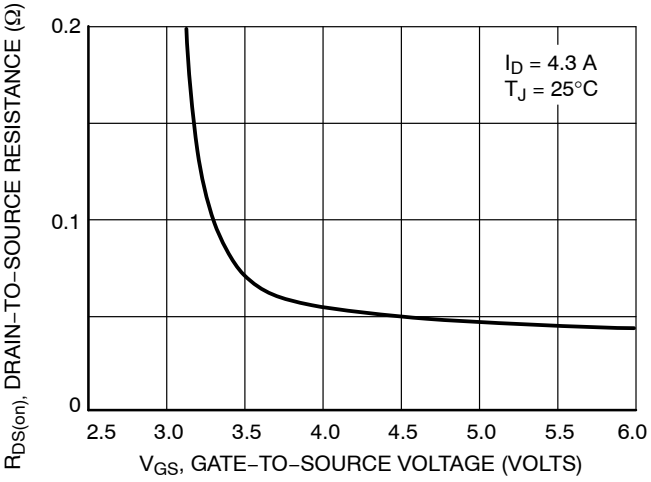


Figure 3. On−Resistance vs. Gate−to−Source Voltage

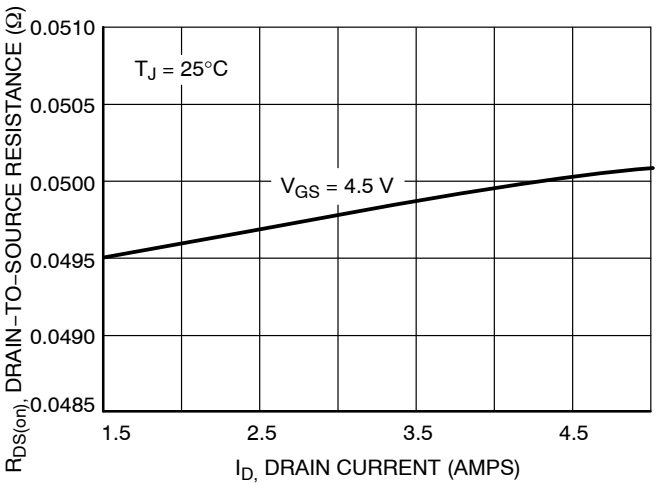


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

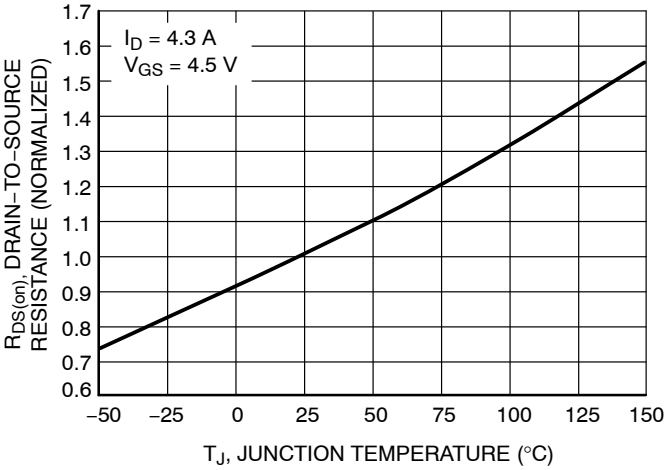


Figure 5. On−Resistance Variation with Temperature

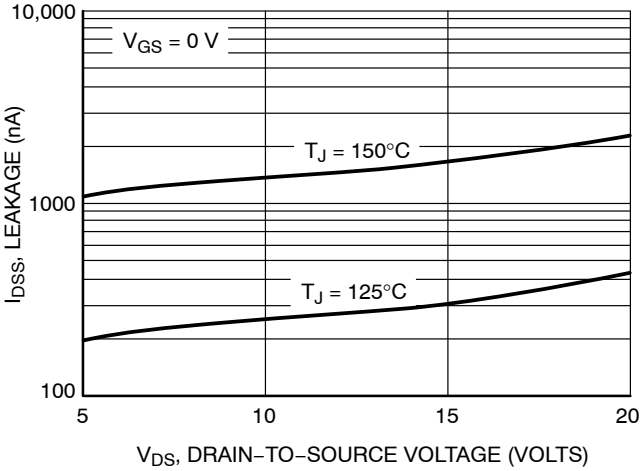


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL MOSFET I N−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

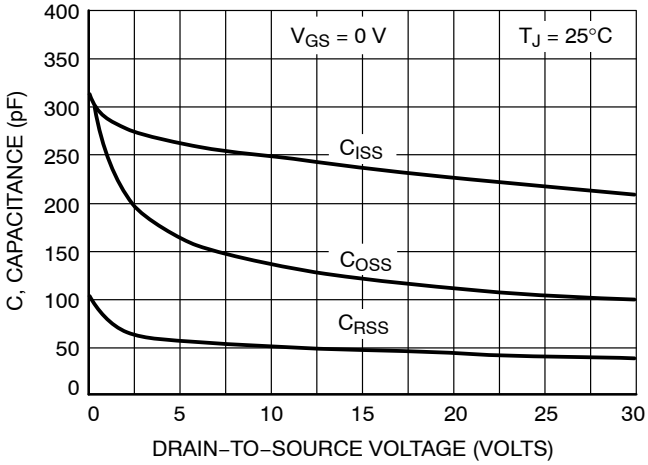


Figure 7. Capacitance Variation

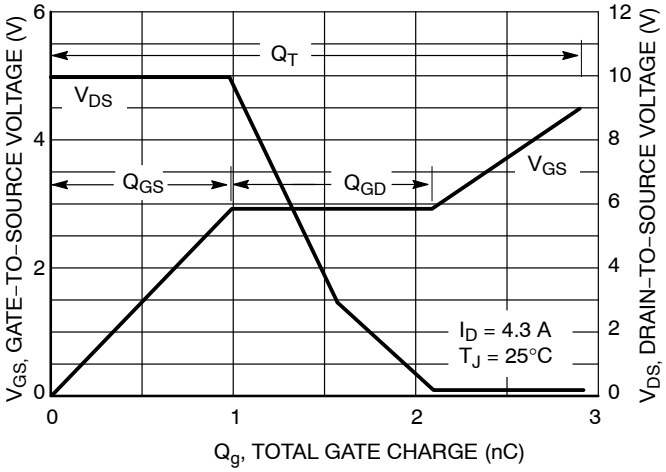


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

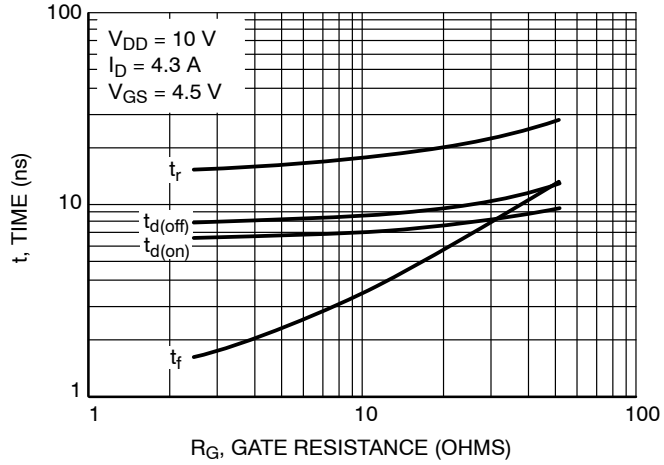


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

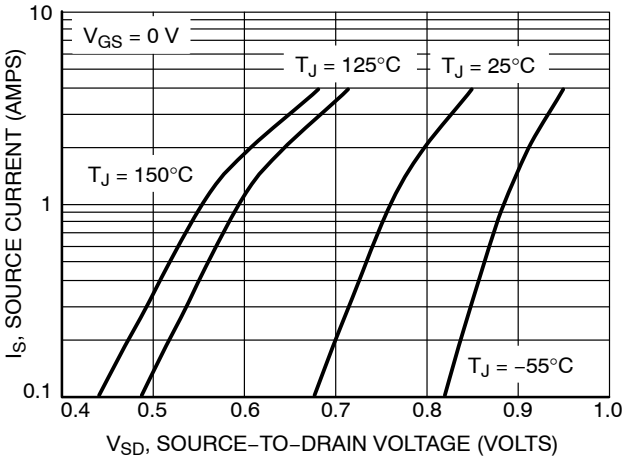


Figure 10. Diode Forward Voltage vs. Current

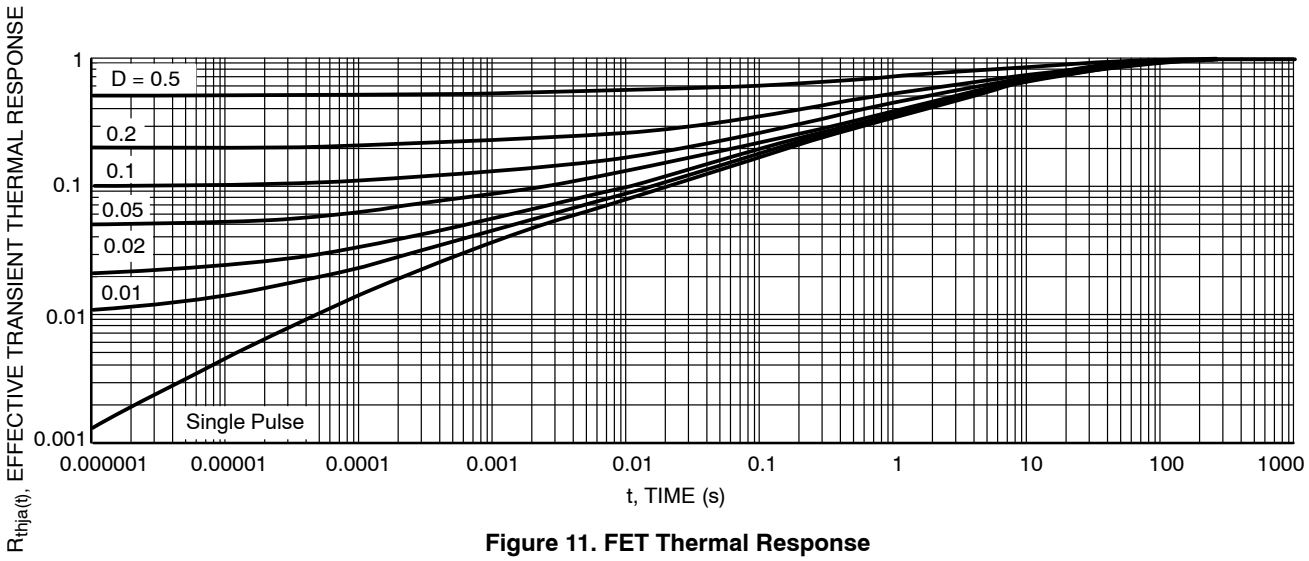


Figure 11. FET Thermal Response

TYPICAL MOSFET II N−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

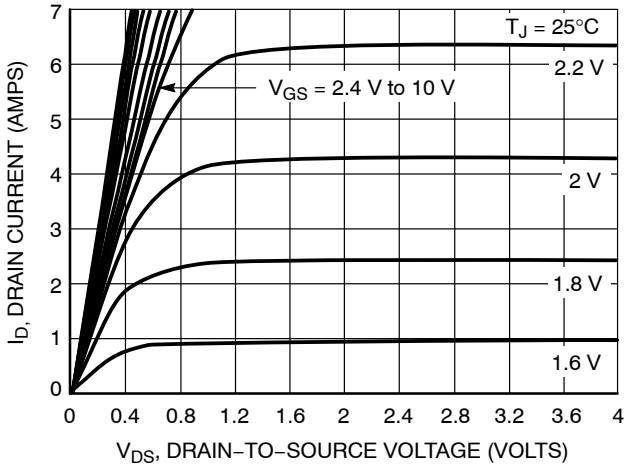


Figure 12. On−Region Characteristics

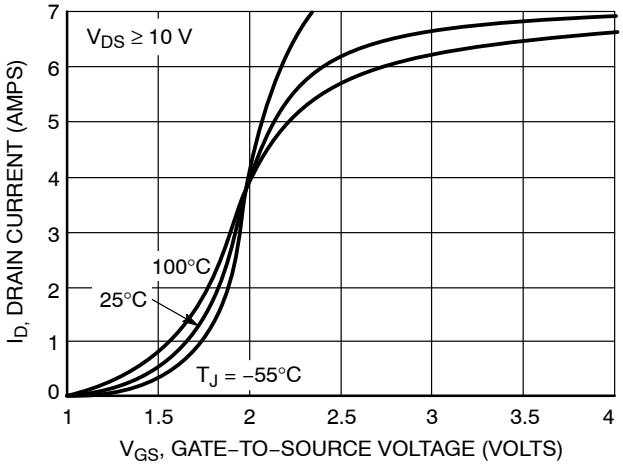


Figure 13. Transfer Characteristics

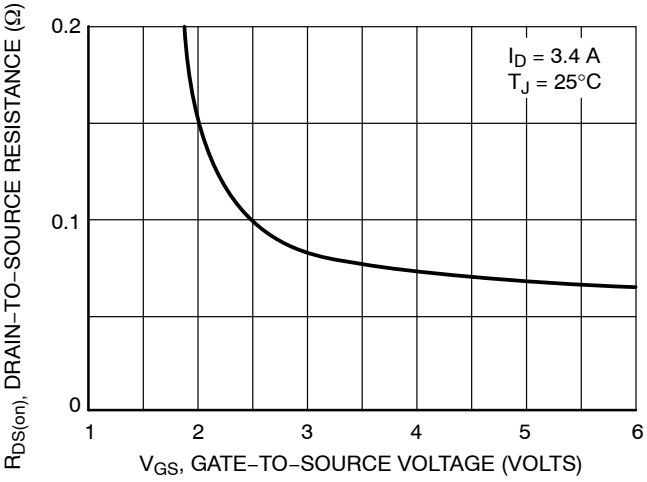


Figure 14. On−Resistance vs. Gate−to−Source Voltage

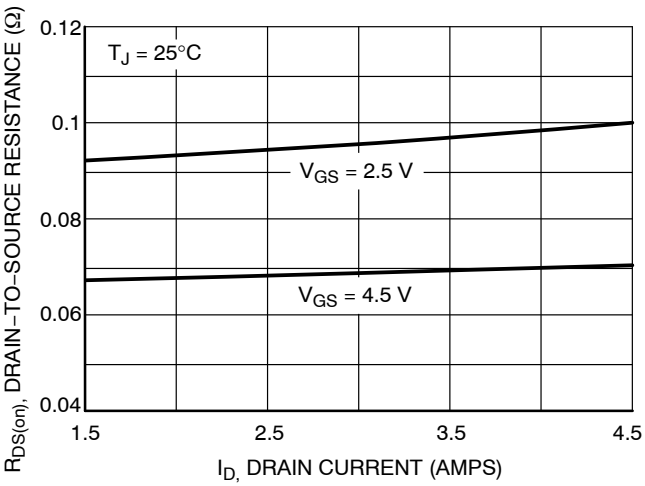


Figure 15. On−Resistance vs. Drain Current and Gate Voltage

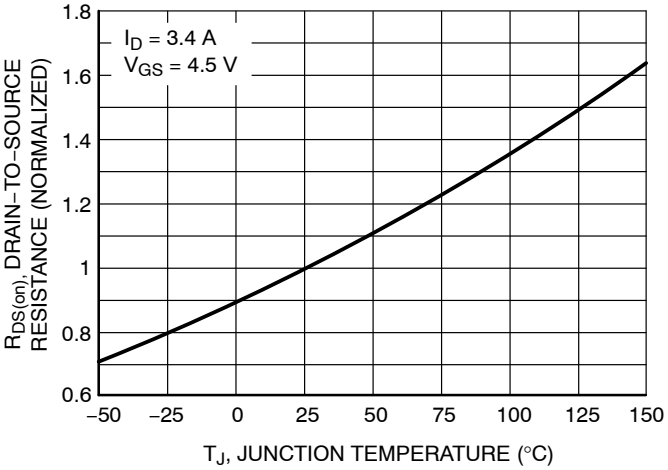


Figure 16. On−Resistance Variation with Temperature

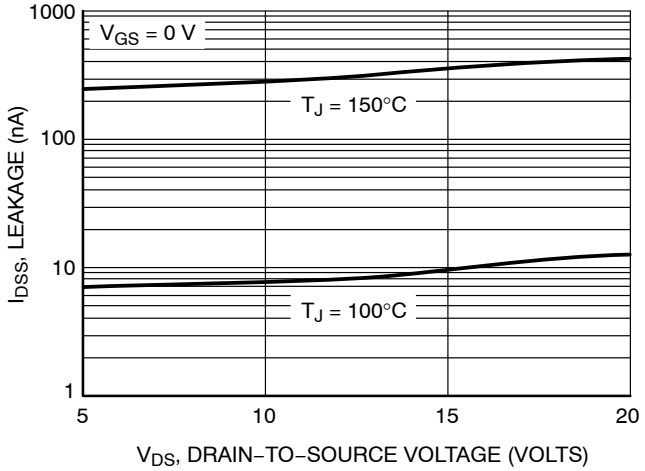


Figure 17. Drain−to−Source Leakage Current vs. Voltage

TYPICAL MOSFET II N−CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

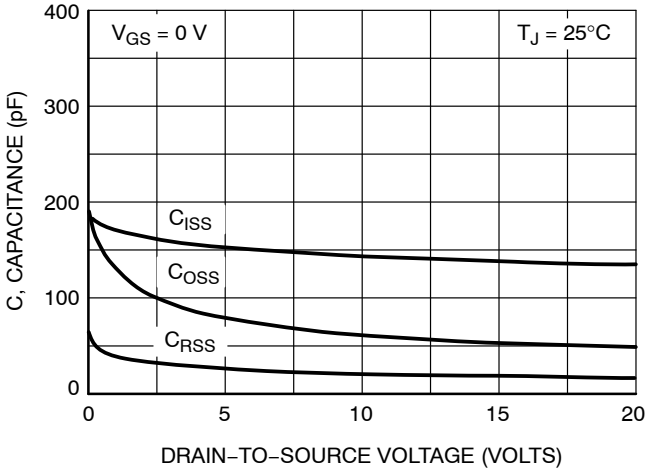


Figure 18. Capacitance Variation

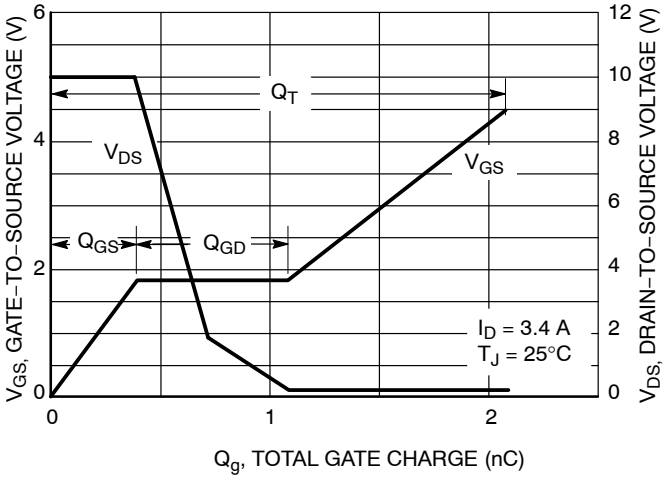


Figure 19. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

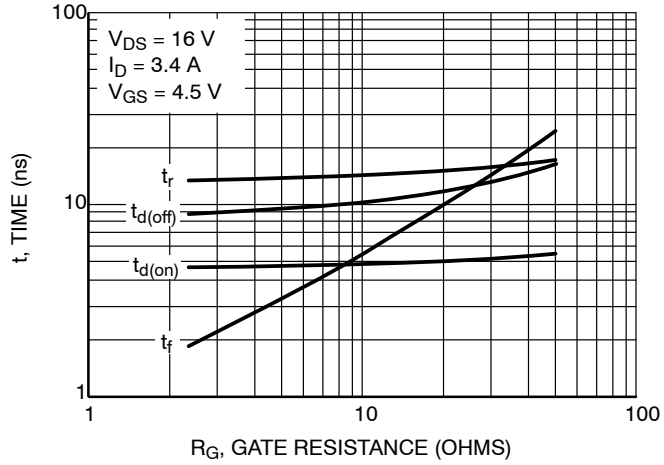


Figure 20. Resistive Switching Time Variation vs. Gate Resistance

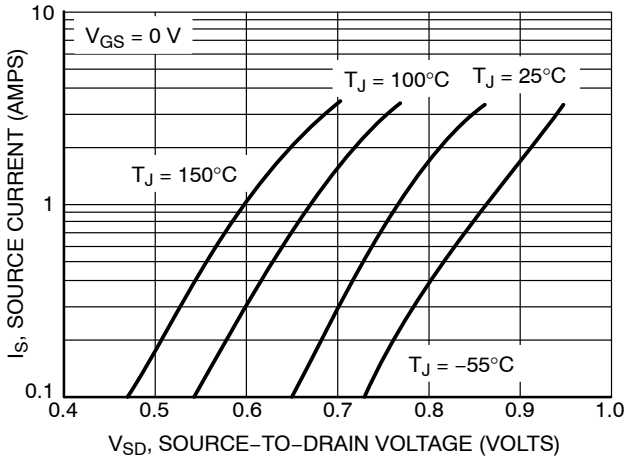


Figure 21. Diode Forward Voltage vs. Current

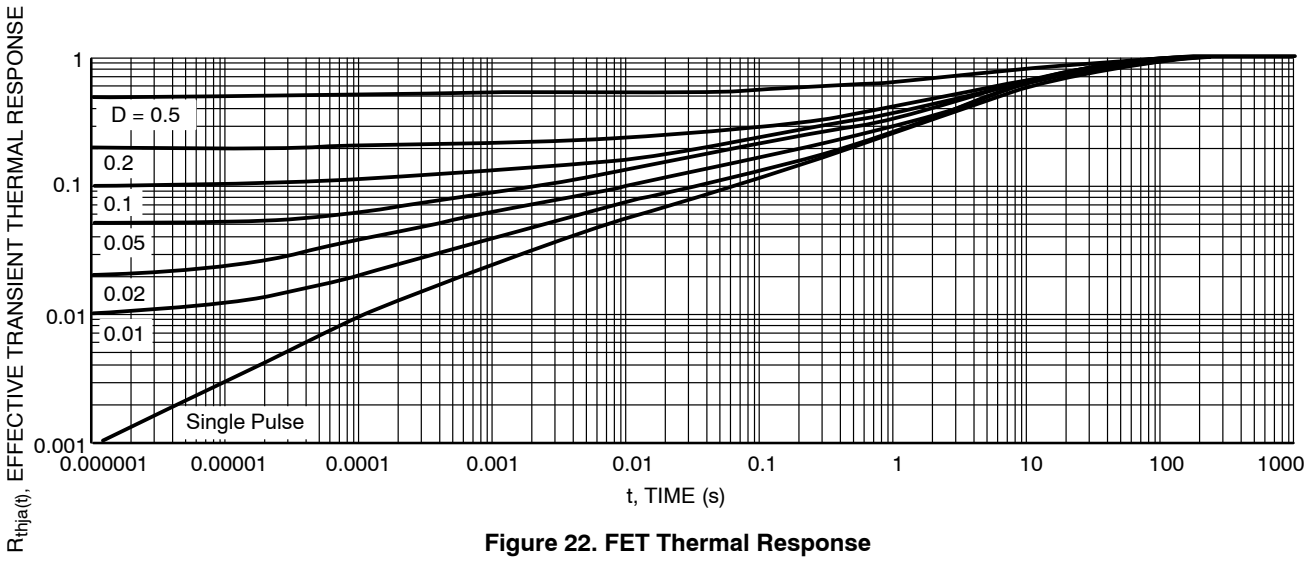


Figure 22. FET Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

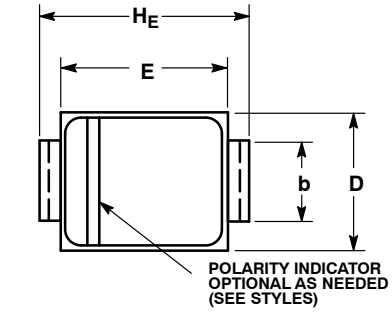
ON Semiconductor®

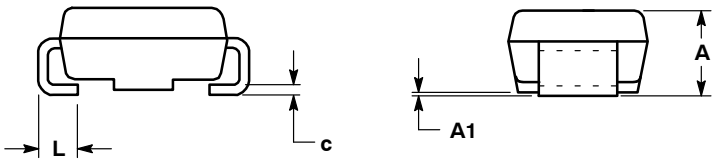
SMA
CASE 403D
ISSUE H

DATE 23 SEP 2015

STYLE 1 STYLE 2

SCALE 1:1

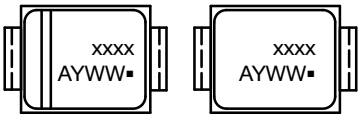




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION b SHALL BE MEASURED WITHIN DIMENSION L.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.97	2.10	2.20	0.078	0.083	0.087
A1	0.05	0.10	0.20	0.002	0.004	0.008
b	1.27	1.45	1.63	0.050	0.057	0.064
c	0.15	0.28	0.41	0.006	0.011	0.016
D	2.29	2.60	2.92	0.090	0.103	0.115
E	4.06	4.32	4.57	0.160	0.170	0.180
H_E	4.83	5.21	5.59	0.190	0.205	0.220
L	0.76	1.14	1.52	0.030	0.045	0.060

GENERIC MARKING DIAGRAM*

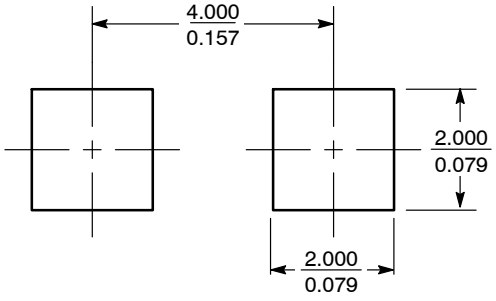


STYLE 1 STYLE 2

xxxx = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



SCALE 8:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

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DESCRIPTION:	SMA		PAGE 1 OF 1

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