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November 2013

### FQD6N50C

# N-Channel QFET<sup>®</sup> MOSFET 500 V, 4.5 A, 1.2 $\Omega$

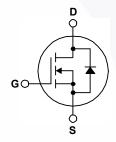
#### **Features**

- 4.5 A, 500 V,  $R_{DS(on)}$  = 1.2  $\Omega$  (Max.) @ $V_{GS}$  = 10 V,  $I_D$  = 2.25 A
- Low Gate Charge (Typ. 19 nC)
- Low Crss (Typ.15 pF)
- · 100% avalanche tested

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.





### **Absolute Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQD6N50CTM	Unit	
$V_{DSS}$	Drain-Source Voltage		500	V	
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		4.5	Α	
	- Continuous (T <sub>C</sub> = 100°C)		2.7	Α	
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	18	Α	
V <sub>GSS</sub>	Gate-Source Voltage		± 30	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note		300	mJ	
I <sub>AR</sub>	Avalanche Current	(Note 1)	4.5	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	6.1	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns	
	Power Dissipation (T <sub>A</sub> = 25°C)*		2.5	W	
$P_D$	Power Dissipation (T <sub>C</sub> = 25°C)		61	W	
	- Derate above 25°C		0.49	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C	
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C		

### **Thermal Characteristics**

Symbol	Parameter	FQD6N50CTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max. 2.05		
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (minimum pad of 2 oz copper), Max.	110	°C/W
	Thermal Resistance, Junction-to-Ambient (* 1 in² pad of 2 oz copper), Max.	50	

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### **Package Marking and Ordering Information**

Device Marking Device		Package	Package Reel Size		Quantity	
FQD6N50C	FQD6N50CTM	D-PAK	330 mm	16 mm	2500 units	

### $\textbf{Electrical Characteristics} \quad \textbf{T}_{C} = 25^{\circ} \text{C unless otherwise noted}.$

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.8		V/°C
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>DSS</sub>		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu\text{A}$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.25A		1.0	1.2	Ω
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_{D} = 2.25 \text{A}$		4.5		S
C <sub>iss</sub> C <sub>oss</sub>	Input Capacitance Output Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		540 80	700 105	pF pF
				80		<u> </u>
C <sub>rss</sub>	Reverse Transfer Capacitance			15	20	pF
Switchi	ng Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 4.5A,		10	30	ns
t <sub>r</sub>	Turn-On Rise Time	$R_{G} = 250  \Omega$		35	80	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	11.G 20 32		55	120	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		45	100	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 4.5A,	/	19	25	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		2.8		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)		8.8		nC
Drain-S	ource Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				4.5	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode F	Forward Current			18	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.5 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.5 A,		260		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		1.6		μС

#### NOTES:

 $<sup>{\</sup>bf 1.}\ {\bf Repetitive}\ {\bf Rating: Pulse\ width\ limited\ by\ maximum\ junction\ temperature.}$ 

<sup>2.</sup> L = 26.6 mH,  $I_{AS}$  = 4.5A,  $V_{DD}$  = 50V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C.

 $<sup>3.~\</sup>text{I}_{SD} \leq~4.5\text{A},~\text{di/dt} \leq 200\text{A/}\mu\text{s},~\text{V}_{DD} \leq \text{BV}_{DSS,}~\text{starting}~\text{T}_{J} = 25^{\circ}\text{C}.$ 

<sup>4.</sup> Essentially independent of operating temperature.

### **Typical Characteristics**

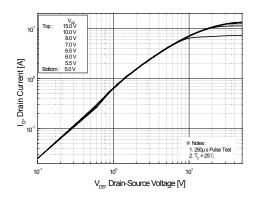


Figure 1. On-Region Characteristics

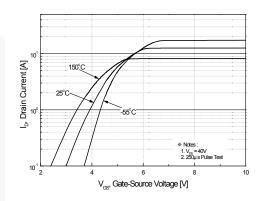


Figure 2. Transfer Characteristics

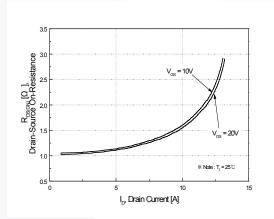


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

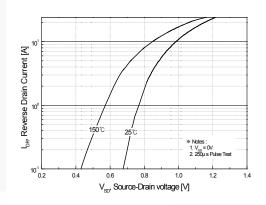


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

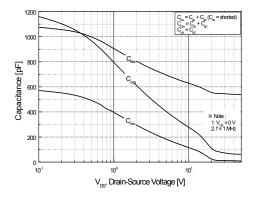


Figure 5. Capacitance Characteristics

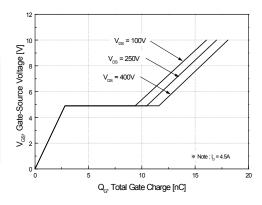


Figure 6. Gate Charge Characteristics

### Typical Characteristics (Continued)

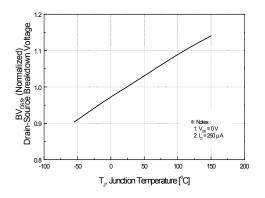
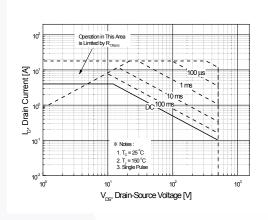


Figure 7. Breakdown Voltage Variation vs Temperature

Figure 8. On-Resistance Variation vs Temperature



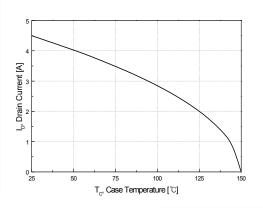


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs Case Temperature

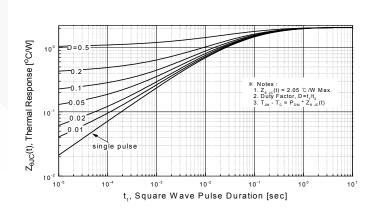


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

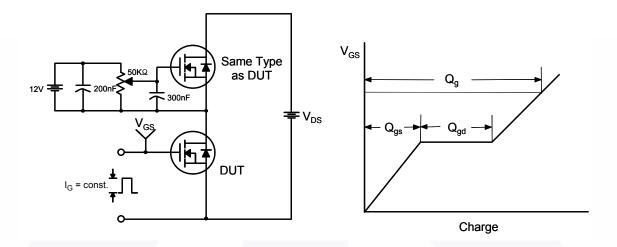


Figure 13. Resistive Switching Test Circuit & Waveforms

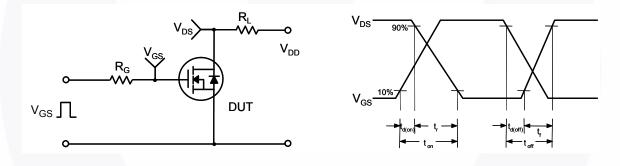
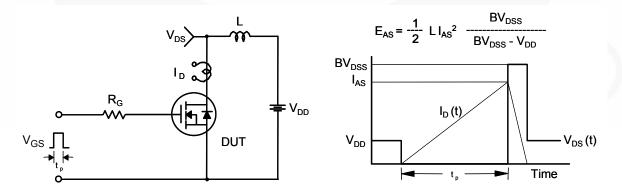
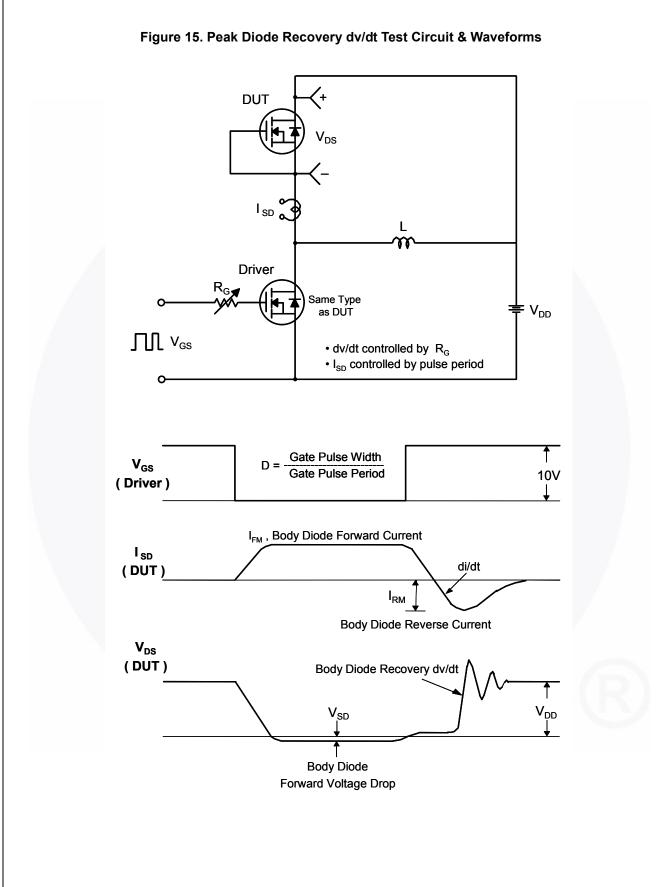


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms





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### **Mechanical Dimensions**

## TO-252 3L (DPAK)

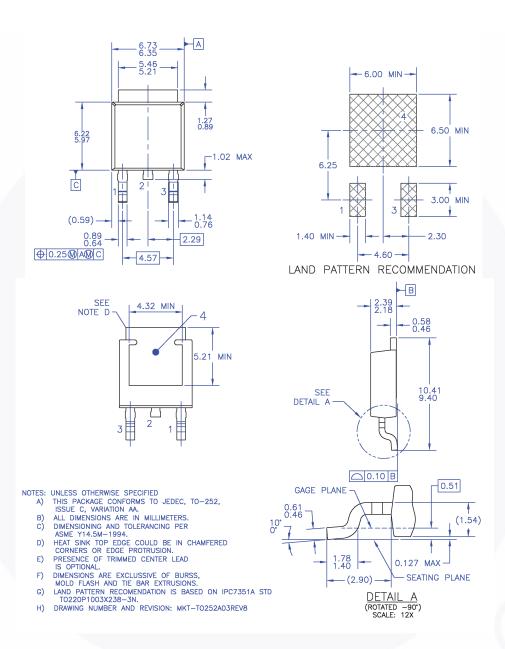


Figure 16. TO252 (D-PAK), Molded, 3 Lead, Option AA&AB

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Dimension in Millimeters





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