REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add post radiation assurance limits to I_{CC+} and I_{CC-} parameters under Table I. Make changes to conditions columns to $+V_{TRIP}$, $-V_{TRIP}$, V_{IO}, and V_{HYST} parameters under Table I. - ro	14-09-18	C. SAFFLE

REV																			
SHEET																			
REV	A	A	A	A															
SHEET	15	16	17	18															

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
14-05-21

REVISION LEVEL
A

MICROCIRCUIT, LINEAR, SINGLE, HIGH SPEED COMPARATOR AMPLIFIER, MONOLITHIC SILICON

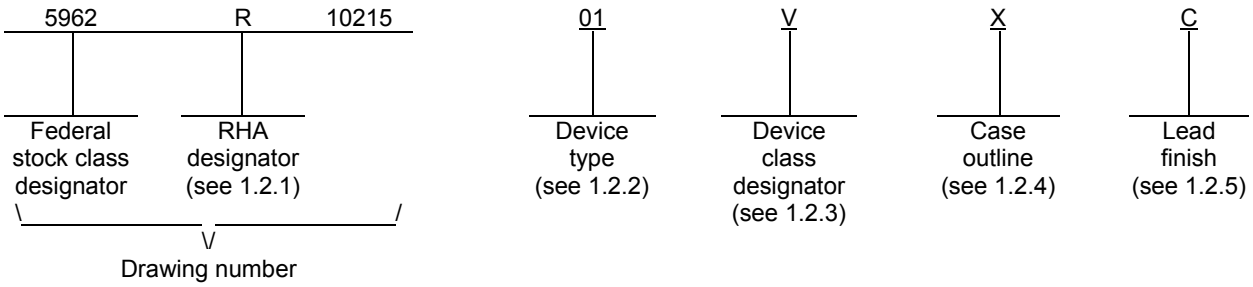
SIZE	CAGE CODE	
A	**67268**	**5962-10215**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RHR801	Radiation hardened, high speed comparator amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	8	Flat pack 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Al_2O_3 ceramic header with metalized bottom side and pullback of 0.01 inch x 0.02 inch.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage (V_{CC})	6 V
Differential input voltage (V_{ID})	2 V 4/
Input voltage (V_{IN})	V_{CC} – 1 V 5/
Storage temperature range (T_{stg})	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C
Thermal resistance, junction-to-ambient (θ_{JA})	125°C/W 6/
Thermal resistance, junction-to-case (θ_{JC})	40°C/W 6/
Lead temperature (soldering, 10 seconds)	+260°C 7/

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	3 V to 5 V
Common-mode input voltage range (V_{ICM})	$-V_{CC}$ + 0.5 V to $+V_{CC}$ - 1.2 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	100 krads(Si) 8/
Maximum total dose available (dose rate = 10 mrads(Si)/s)	30 krads(Si) 8/
Single event phenomenon (SEP) :	
No single event latch up (SEL) effective LET	≤ 120 MeV/(mg/cm^2)
Single event transient (SET) (σ_{sat} = 3.8 x 10^{-6} cm^2/device) at effective LET	60 MeV/(mg/cm^2)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltage values, except differential voltage are within respect to network ground terminal.
4/ Differential voltage are the non-inverting input terminal with respect to the inverting input terminal.
5/ The magnitude of input and output voltages must never exceed V_{CC} + 0.3 V.
6/ Short circuits can cause excessive heating and destructive dissipation. Values are normal.
7/ Distance of not less than 1.5 mm from the device body and the same lead shall not be re-soldered until three minutes have elapsed.
8/ For device type 01, this part has been tested at high dose rate, the radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition A. For low dose rate, the radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition D.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
$+V_{CC}$ = 3.3 V, $-V_{CC}$ = 0 V (unless otherwise specified)								
High output supply current	$+I_{CC}$	$+V_{IN}$ = 1 V, $-V_{IN}$ = 0 V, V_{OUT} = high level, no load		1	01	1.2	1.6	mA
				2		1.4	2.1	
				3		0.95	1.3	
			P, R	1		1.2	2.5	
Low output supply current	$-I_{CC}$	$+V_{IN}$ = 1 V, $-V_{IN}$ = 0 V, V_{OUT} = high level, no load		1	01	1.3	1.8	mA
				2		1.6	2.3	
				3		1	1.5	
			P, R	1		1.3	3	
High input threshold	$+V_{TRIP}$	V_{ICM} = 0.5 V,		1	01	-7	7	mV
		V_{ICM} = 1.65 V,		2		-8	8	
		V_{ICM} = 2.1 V		3		-8	8	
Low input threshold	$-V_{TRIP}$	V_{ICM} = 0.5 V,		1	01	-7	7	mV
		V_{ICM} = 1.65 V,		2		-8	8	
		V_{ICM} = 2.1 V		3		-8	8	
Input offset voltage	V_{IO}	V_{ICM} = 0.5 V,		1	01	-7	7	mV
		V_{ICM} = 1.65 V,		2		-8	8	
		V_{ICM} = 2.1 V		3		-8	8	
Hysteresis voltage	V_{HYST}	V_{ICM} = 0.5 V,		1	01	1.5	4	mV
		V_{ICM} = 1.65 V,		2		-	20	
		V_{ICM} = 2.1 V		3		-	20	
Non inverting input bias current	$+I_{IB}$	V_{ICM} = 1.65 V		1	01	-5	-	µA
				2		-4	-	
				3		-7	-	
Inverting input bias current	$-I_{IB}$	V_{ICM} = 1.65 V		1	01	-5	-	µA
				2		-4	-	
				3		-7	-	
High level output voltage	V_{OH}	V_{ID} =+1 V, I_{SOURCE} = +3.3 mA.		1	01	3.05	3.3	V
				2		3	3.3	
				3		3.1	3.3	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$+V_{CC}$ = 3.3 V, $-V_{CC}$ = 0 V (unless otherwise specified)							
Low level output voltage	V_{OL}	V_{ID} = -1 V, I_{SINK} = -3.3 mA	1	01	-	250	mV
			2		-	300	
			3		-	200	
Output sink current	I_{SINK}	V_{ID} = -500 mV, V_{OUT} = $+V_{CC}$	1	01	18	22	mA
			2		14	20	
			3		19	26	
Output source current	I_{SOURCE}	V_{ID} = +500 mV, V_{OUT} = $-V_{CC}$	1	01	20	25	mA
			2		17	23	
			3		22	29	
Propagation time logic “0” to logic “1”	t_{PLH}	50 mV overdrive, C_L = 30 pF, V_{ICM} = 1.65 V	9	01	6	9.5	ns
			10		7	12	
			11		6	9.5	
		100 mV overdrive, C_L = 30 pF, V_{ICM} = 1.65 V	9		5.5	9	
			10		6.5	10.5	
			11		5.5	9	
Propagation time logic “1” to logic “0”	t_{PHL}	50 mV overdrive C_L = 30 pF, V_{ICM} = 1.65 V	9	01	6	9.5	ns
			10		7	12	
			11		6	9.5	
		100 mV overdrive, C_L = 30 pF, V_{ICM} = 1.65 V	9		5.5	9	
			10		6.5	10.5	
			11		5.5	9	
Output rise time	t_R	50 mV overdrive, C_L = 30 pF	9	01	-	9	ns
			10		-	10	
			11		-	10	
Output fall time	t_F	50 mV overdrive, C_L = 30 pF	9	01	-	9	ns
			10		-	10	
			11		-	10	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$+V_{CC}$ = 3.3 V, $-V_{CC}$ = 0 V (unless otherwise specified)							
Maximum input frequency	F_{MAX}	V_{IN} = 1 Vp-p sine wave, C_L = 10 pF, output between 45% and 55%	4	01	55	-	MHz
			5		55	-	
			6		50	-	
Common-mode rejection 2/ ratio ($\Delta V_{IC}/\Delta V_{IO}$)	CMRR	V_{ICM} = 0.5 V to $+V_{CC}$ - 1.2 V	1	01	70	-	dB
			2		50	-	
			3		60	-	
Supply voltage rejection 2/ ratio ($\Delta V_{CC}/\Delta V_{IO}$)	SVR	$+V_{CC}$ = 3 V to 3.6 V, V_{ICM} = 1.65 V	1	01	55	-	dB
			2		42	-	
			3		45	-	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
$+V_{CC}$ = 5 V, $-V_{CC}$ = 0 V (unless otherwise specified)								
High output supply current	$+I_{CC}$	$+V_{IN}$ = 1 V, $-V_{IN}$ = 0 V, V_{OUT} = high level, no load		1	01	1.3	1.8	mA
				2		1.5	2.3	
				3		1	1.5	
			P, R	1		1.3	6	
Low output supply current	$-I_{CC}$	$+V_{IN}$ = 1 V, $-V_{IN}$ = 0 V, V_{OUT} = high level, no load		1	01	1.5	2	mA
				2		1.8	2.5	
				3		1.2	1.7	
			P, R	1		1.5	6	
High input threshold	$+V_{TRIP}$	V_{ICM} = 0.5 V,		1	01	-7	7	mV
		V_{ICM} = 2.5 V,		2		-8	8	
		V_{ICM} = 3.8 V		3		-8	8	
Low input threshold	$-V_{TRIP}$	V_{ICM} = 0.5 V,		1	01	-7	7	mV
		V_{ICM} = 2.5 V,		2		-8	8	
		V_{ICM} = 3.8 V		3		-8	8	
Input offset voltage	V_{IO}	V_{ICM} = 0.5 V,		1	01	-7	7	mV
		V_{ICM} = 2.5 V,		2		-8	8	
		V_{ICM} = 3.8 V		3		-8	8	
Hysteresis voltage	V_{HYST}	V_{ICM} = 0.5 V,		1	01	1.5	4	mV
		V_{ICM} = 2.5 V,		2		-	20	
		V_{ICM} = 3.8 V		3		-	20	
Non inverting input bias current	$+I_{IB}$	V_{ICM} = 2.5 V		1	01	-6	-	µA
				2		-5	-	
				3		-8	-	
Inverting input bias current	$-I_{IB}$	V_{ICM} = 2.5 V		1	01	-6	-	µA
				2		-5	-	
				3		-8	-	
High level output voltage	V_{OH}	V_{ID} = +1 V, I_{SOURCE} = +5 mA		1	01	4.7	5	V
				2		4.6	5	
				3		4.8	5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$+V_{CC}$ = 5 V, $-V_{CC}$ = 0 V (unless otherwise specified)							
Low level output voltage	V_{OL}	V_{ID} = -1 V, I_{SINK} = -5 mA	1	01	-	300	mV
			2		-	400	
			3		-	300	
Output sink current	I_{SINK}	V_{ID} = -500 mV, V_{OUT} = $+V_{CC}$	1	01	30	40	mA
			2		25	35	
			3		30	45	
Output source current	I_{SOURCE}	V_{ID} = +500 mV, V_{OUT} = $-V_{CC}$	1	01	40	50	mA
			2		35	45	
			3		45	55	
Propagation time logic “0” to logic “1”	t_{PLH}	50 mV overdrive, C_L = 30 pF, V_{ICM} = 2.5 V	9	01	6	9.5	ns
			10		6	10	
			11		5.5	10	
		100 mV overdrive, C_L = 30 pF, V_{ICM} = 2.5 V	9		5.5	9	
			10		5.5	9.5	
			11		5	9	
Propagation time logic “1” to logic “0”	t_{PHL}	50 mV overdrive, C_L = 30 pF, V_{ICM} = 2.5 V	9	01	6	9.5	ns
			10		6	10	
			11		5.5	10	
		100 mV overdrive, C_L = 30 pF, V_{ICM} = 2.5 V	9		5.5	9	
			10		5.5	9.5	
			11		5	9	
Output rise time	t_R	50 mV overdrive, C_L = 30 pF	9	01	-	6	ns
			10		-	7	
			11		-	7	
Output fall time	t_F	50 mV overdrive, C_L = 30 pF	9	01	-	6	ns
			10		-	7	
			11		-	7	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$+V_{CC}$ = 5 V, $-V_{CC}$ = 0 V (unless otherwise specified)							
Maximum input frequency	f_{MAX}	V_{IN} = 1 Vp-p sine wave, C_L = 10 pF, output between 45% and 55%	4	01	85	-	MHz
			5		90	-	
			6		80	-	
Common-mode rejection 2/ ratio ($\Delta V_{IC}/\Delta V_{IO}$)	CMRR	V_{ICM} = 0.5 V to $+V_{CC}$ - 1.2 V	1	01	70	-	dB
			2		60	-	
			3		60	-	
Supply voltage rejection 2/ ratio ($\Delta V_{CC}/\Delta V_{IO}$)	SVR	$+V_{CC}$ = 4.5 V to 5 V, V_{ICM} = 2.375 V	1	01	60	-	dB
			2		50	-	
			3		50	-	

1/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is tested only at the “P” level for low dose and at the “R” level for high dose rate. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C. The radiation end points limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method D for low dose rate and condition A for high dose rate.

2/ Parameter tested in go-no-go mode only.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = temperature ±10°C 3/	V_{CC} = ±1.5 V and ±2.5 V		Bias for latch-up test, V_{CC} = ±2.6 V, no latch up LET = 3/ 4/
		Effective LET no transient [MeV/(mg/cm^2)]	Maximum device cross section	
01	+25°C for SET +125°C for SEL	LET ≤ 3	3.8 x 10^{-6} cm^2/device	≤ 120

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemental by in line data may be used in lieu of end of line testing. Test plan must be approved by technical review board (TRB) and qualifying activity.
3/ Worst case temperature is T_A = +125°C ±10°C for SEL test and T_A = +25°C ±10°C for SET test.
4/ Tested to a LET of ≤120 MeV/(mg/cm^2) for device type 01 with no latch up (SEL).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

Case X

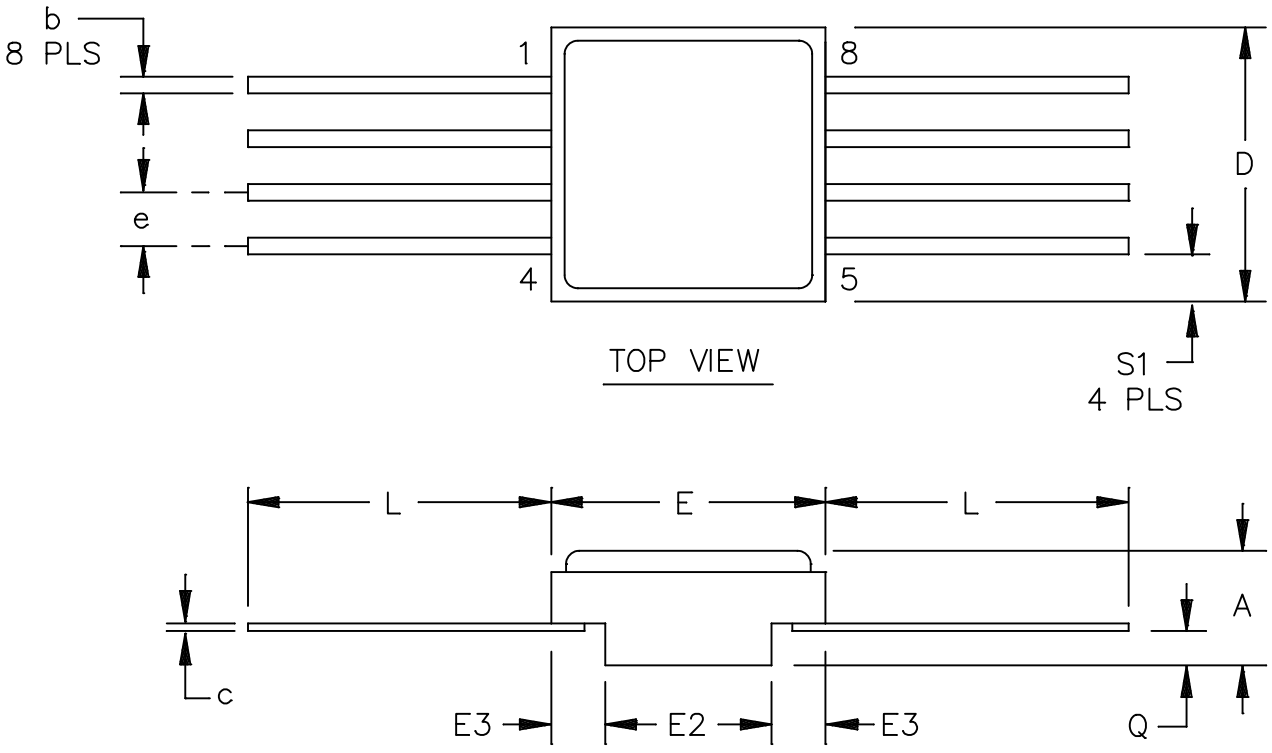


FIGURE 1. Case outline.

Symbol	Dimensions					
	Inches			Millimeters		
	Min	Med	Max	Min	Med	Max
A	.088	.096	.104	2.24	2.44	2.64
b	.015	.017	.019	0.38	0.43	0.48
c	.004	.005	.006	0.10	0.13	0.16
D	.250	.255	.260	6.35	6.48	6.61
E	.250	.255	.260	6.35	6.48	6.61
E2	.170	.175	.180	4.32	4.45	4.58
E3	.035	.040	.045	0.88	1.01	1.14
e	.050 BSC			1.27 BSC		
L	.256	---	.291	6.51	---	7.38
Q	.026	.031	.036	0.66	0.79	0.92
S1	.036	.044	.052	0.92	1.12	1.32
n	8			8		

NOTES:
1. The US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch pound units, the inch pound units shall take precedence.
2. N is the maximum number of terminal positions.

FIGURE 1. Case outline.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	NC
2	-INPUT
3	+INPUT
4	$-V_{CC}$
5	NC
6	OUT
7	$+V_{CC}$
8	NC

FIGURE 2. Terminal connections.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,9	1,9
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3,4, 1/ 2/ 5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4, 2/ 5,6,9,10,11
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9
Group E end-point electrical parameters (see 4.4)	1,9	1,9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous electrical parameters.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIB. Burn-in and operating life test delta parameters.

Parameters	Symbol	Test conditions	Delta limits	Units
Change high output supply current	$\Delta+I_{CC}$	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, $+V_{IN}$ = 1 V, $-V_{IN}$ = 0 V, V_{OUT} = high level, no load	± 20	µA
Change low output supply current	$\Delta-I_{CC}$	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, $+V_{IN}$ = 0 V, $-V_{IN}$ = 1 V, V_{OUT} = low level, no load	± 20	µA
Change input offset voltage	ΔV_{IO}	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, $V_{ICM} = V_{CC/2}$	± 1	mV
Change hysteresis voltage	ΔV_{HYST}	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, $V_{ICM} = V_{CC/2}$	± 400	µV
Change non inverting input bias current	$\Delta+I_B$	$+V_{CC}$ = 5 V, $-V_{CC}$ = 0 V, $V_{ICM} = V_{CC/2}$	± 500	nA
Change inverting input bias current	$\Delta-I_B$	$+V_{CC}$ = 5 V, $-V_{CC}$ = 0 V, $V_{ICM} = V_{CC/2}$	± 500	nA
Change high level output voltage	ΔV_{OH}	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, V_{ID} = +1 V, I_{SOURCE} = 3.3 mA or 5 mA	± 5	mV
Change low level output voltage	ΔV_{OL}	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, V_{ID} = -1 V, I_{SINK}= 3.3 mA or 5 mA	± 10	mV
Change output sink current	ΔI_{SINK}	$+V_{CC}$ = 3.3 V, $-V_{CC}$ = 0 V, V_{ID} = -500 mV, $V_{OUT} = +V_{CC}$	± 100	µA
		$+V_{CC}$ = 3.3 V, $-V_{CC}$ = 0 V, V_{ID} = -500 mV, $V_{OUT} = +V_{CC}$	± 200	µA
Change output source current	ΔI_{SOURCE}	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, V_{ID} = +500 mV $V_{OUT} = -V_{CC}$	± 800	µA
Change propagation time logic “0” to “1”	Δt_{PLH}	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, 100 mV overdrive, C_L = 30 pF	± 200	ps
Change propagation time logic “1” to “0”	Δt_{PHL}	$+V_{CC}$ = 3.3 V or 5 V, $-V_{CC}$ = 0 V, 100 mV overdrive, C_L = 30 pF	± 200	ps

1/ Deltas are performed at room temperature, T_A = +25°C.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and condition D as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (for example: 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C for the transient measurements and the maximum rated operating temperature ±10°C for the latchup measurements.

f. Bias conditions shall be V_{CC} = V_{CC} maximum for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of transients (SEP).

d. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-09-18

Approved sources of supply for SMD 5962-10215 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1021501VXC	F8859	RHR801K01V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.