

DDR4 SDRAM VLP RDIMM Addendum

MTA18ADF4G72PZ – 32GB

Introduction

Information provided here is in addition to or supersedes information provided in the Micron DDR4 RDIMM Core data sheet.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR4 RDIMM core data sheet
- 288-pin, very low profile registered dual in-line memory module (VLP RDIMM)
- Fast data transfer rate: PC4-3200, PC4-2933
- 32GB (4 Gig x 72)
- Single-rank
- 16 internal banks; 4 groups of 4 banks each

Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Package
 - 288-pin DIMM (Green)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)
 - 0.682ns @ CL = 21 (DDR4-2933)

Marking

None
Z
-3G2
-2G9

Figure 1: 288-Pin VLP RDIMM (MO-309, R/C-F1, PCB 2718)

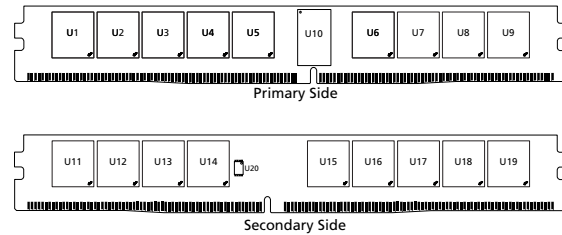


Figure 2: 288-Pin VLP RDIMM (MO-309, R/C-F2, PCB 2954)

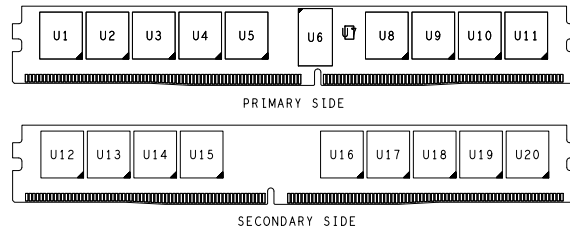


Table 1: Addressing

Parameter	32GB
Row address	256K A[17:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (4 Gig x 4), 16 banks
Module rank address	1 CS_n[0]



Table 2: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT40A4G4,¹ 16Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-nRCD-nRP)
MTA18ADF4G72PZ-3G2__	32GB	4 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA18ADF4G72PZ-2G9__	32GB	4 Gig x 72	23.47 GB/s	0.625ns/2933 MT/s	21-21-21

- Notes:
1. The data sheet for the base device can be found on micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA18ADF4G72PZ-3G2B1.

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DQ Map

Table 3: Component-to-Module DQ Map - PCB 2718

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	7	155	U2	0	15	166
	1	5	148		1	13	159
	2	6	10		2	14	21
	3	4	3		3	12	14
U3	0	23	177	U4	0	31	188
	1	21	170		1	29	181
	2	22	32		2	30	43
	3	20	25		3	28	36
U5	0	CB7	199	U6	0	39	247
	1	CB5	192		1	37	240
	2	CB6	54		2	38	102
	3	CB4	47		3	36	95
U7	0	47	258	U8	0	55	269
	1	45	251		1	53	262
	2	46	113		2	54	124
	3	44	106		3	52	117
U9	0	63	280	U11	0	56	130
	1	60	128		1	58	137
	2	62	135		2	57	275
	3	61	273		3	59	282
U12	0	48	119	U13	0	40	108
	1	50	126		1	42	115
	2	49	264		2	41	253
	3	51	271		3	43	260
U14	0	32	97	U15	0	CB1	194
	1	34	104		1	CB3	201
	2	33	242		2	CB0	49
	3	35	249		3	CB2	56
U16	0	25	183	U17	0	17	172
	1	27	190		1	19	179
	2	24	38		2	16	27
	3	26	45		3	18	34
U18	0	9	161	U19	0	1	150
	1	11	168		1	3	157
	2	8	16		2	0	5
	3	10	23		3	2	12



Table 4: Component-to-Module DQ Map - PCB 2954

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	6		U2	0	14	
	1	4			1	13	
	2	7			2	15	
	3	5			3	12	
U3	0	22		U4	0	30	
	1	21			1	28	
	2	23			2	31	
	3	20			3	29	
U5	0	CB6		U8	0	39	
	1	CB4			1	37	
	2	CB7			2	38	
	3	CB5			3	36	
U9	0	47		U10	0	55	
	1	45			1	53	
	2	46			2	54	
	3	44			3	52	
U11	0	62		U12	0	56	
	1	61			1	59	
	2	63			2	57	
	3	60			3	58	
U13	0	48		U14	0	41	
	1	51			1	43	
	2	49			2	40	
	3	50			3	42	
U15	0	33		U16	0	CB0	
	1	35			1	CB2	
	2	32			2	CB1	
	3	34			3	CB3	
U17	0	24		U18	0	16	
	1	26			1	18	
	2	25			2	17	
	3	27			3	19	
U19	0	8		U20	0	0	
	1	10			1	3	
	2	9			2	1	
	3	11			3	2	

I_{DD} Specifications

Table 5: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 32GB (Die Revision B)

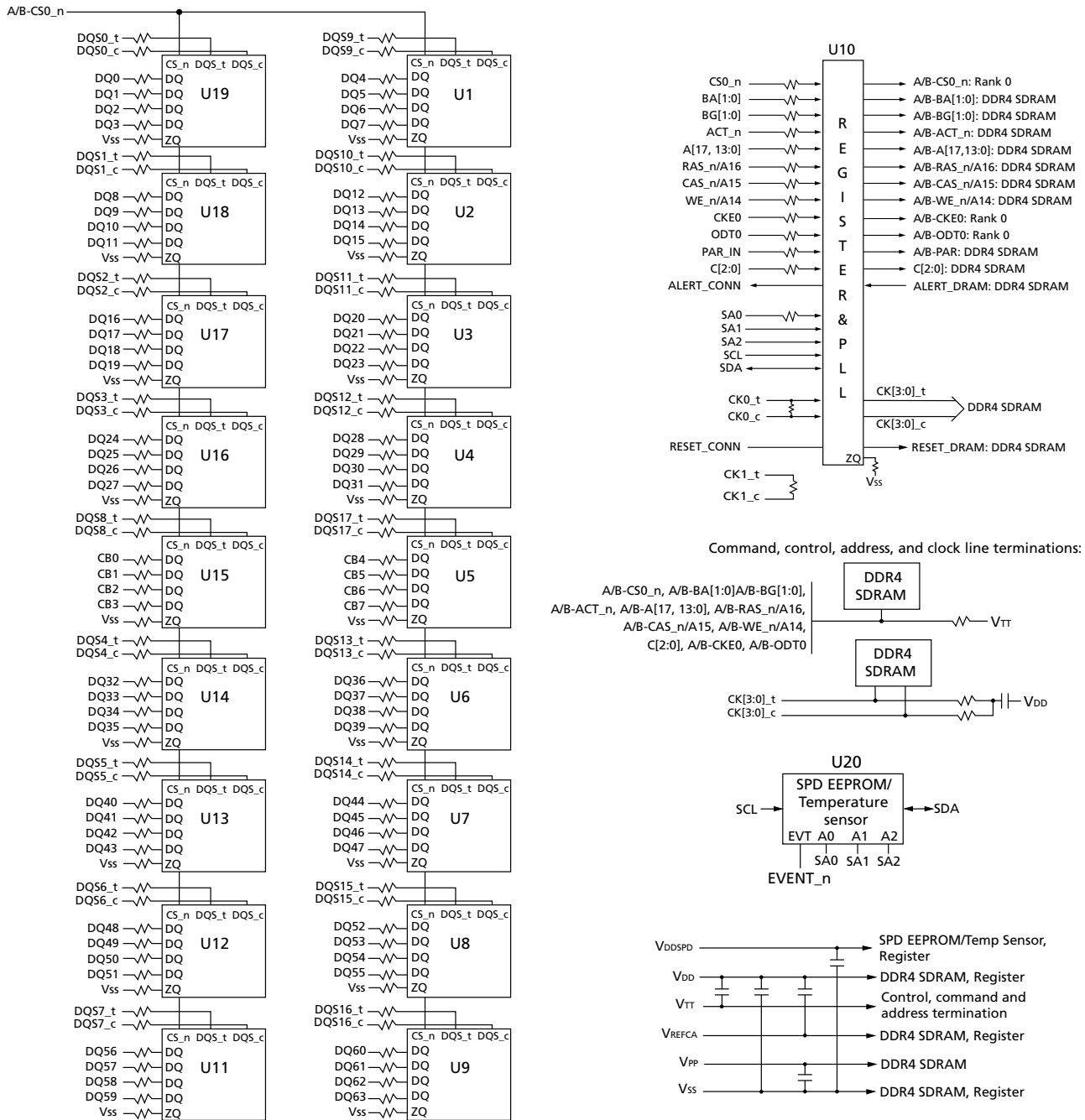
Values are for the MT40A4G4 DDR4 SDRAM only and are computed from values specified in the 16Gb (4 Gig x 4) component data sheet

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	1080	1062	mA
One bank ACTIVATE-PRECHARGE, word line boost, I _{pp} current	I _{PP0}	72	72	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	1260	1242	mA
Precharge standby current	I _{DD2N}	936	918	mA
Precharge standby ODT current	I _{DD2NT}	1008	990	mA
Precharge power-down current	I _{DD2P}	774	774	mA
Precharge quiet standby current	I _{DD2Q}	846	846	mA
Active standby current	I _{DD3N}	1404	1386	mA
Active standby I _{pp} current	I _{PP3N}	54	54	mA
Active power-down current	I _{DD3P}	1242	1224	mA
Burst read current	I _{DD4R}	3096	2952	mA
Burst write current	I _{DD4W}	2952	2826	mA
Burst refresh current (1x REF)	I _{DD5R}	1458	1404	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R}	90	90	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N (0-85°C)}	1206	1206	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E (0-95°C)}	2178	2178	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R (0-45°C)}	522	522	mA
Auto self refresh current (25°C)	I _{DD6A (25°C)}	180	180	mA
Auto self refresh current (45°C)	I _{DD6A (45°C)}	522	522	mA
Auto self refresh current (75°C)	I _{DD6A (75°C)}	1098	1098	mA
Auto self refresh current (95°C)	I _{DD6A (95°C)}	2178	2178	mA
Auto self refresh I _{pp} current	I _{PP6X}	198	198	mA
Bank interleave read current	I _{DD7}	4284	4158	mA
Bank interleave read I _{pp} current	I _{PP7}	198	198	mA
Maximum power-down current	I _{DD8}	720	720	mA

Note: 1. When T_C > 85°C, the I_{DD} and I_{pp} values must be derated. Refer to the base device data sheet I_{DD} and I_{pp} specification tables for derating values for the applicable die-revision.

Functional Block Diagram

Figure 3: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



32GB (x72, ECC, SR) 288-Pin DDR4 VLP RDIMM Functional Block Diagram

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Although considered final, these specifications are subject to change, as further product development and data characterization some-
times occur.