NB6N239SEVB/D

NB6N239S Evaluation Board

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Description

The NB6N239S Evaluation Board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of the NB6N239S. This user's manual provides detailed information on board contents, layout and its use. It should be used in conjunction with the NB6N239S data sheet: (www.onsemi.com).

The NB6N239S is a differential Receiver to differential LVDS Clock Divider. The board features Output Enable control of the Outputs.

Board Features

- Accommodates the electrical characterization of the NB6N239S
- Selectable Jumper for the V_T pin, minimizing cabling
- CLK/$\overline{\text{CLK}}$ input and QA/$\overline{\text{QA}}$ and QB/$\overline{\text{QB}}$ output pins are accessed via SMA connectors
- $\overline{\text{MR}}$, $\overline{\text{EN}}$ and Clock Divide Select pins are accessed via SMA Connectors or by the Logic Switches
- Convenient and Compact Board Layout
- 3.3 V Power Supply Operating Range

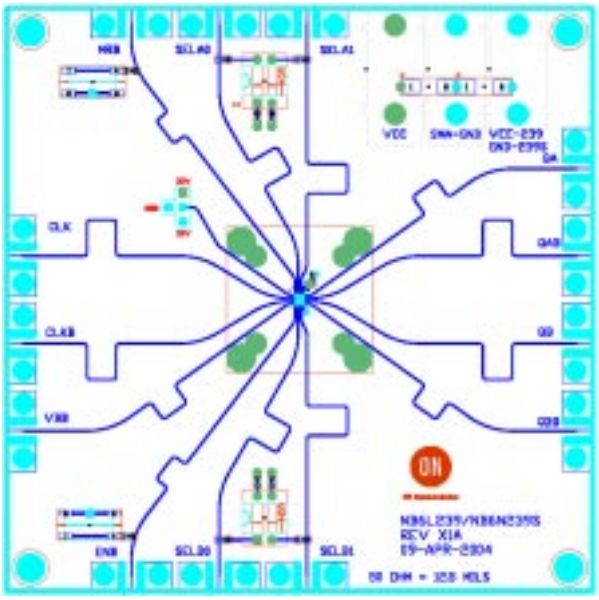


Figure 1. Evaluation Board

PROCEDURE

Lab Setup and Measurement Procedure

Equipment Used

- Agilent Signal Generator #8133A
- Tektronix TDS8000 Oscilloscope
- Agilent #6624A DC Power Supply
- Digital Voltmeter
- Matched High−Speed Cables with SMA Connectors

Power Supply Connections

The NB6N239S has a positive supply pin, V_{CC}, and a negative supply pin, GND.

Power supply terminals V_{CC}, GND and SMAGND are provided. The SMAGND terminal is primarily used for the NB6L239; for the NB6N239S, it can be connected to GND.

Table 1. Power Supply Configurations

Device Pin	Power Supply Connector Color	Single Power Supply
V_{CC}	RED	V_{CC} = +3.3 V
−	BLACK − SMAGND	
GND – 239S	BLACK	GND = 0 V

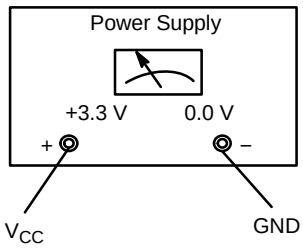


Figure 2. Power Supply Connections

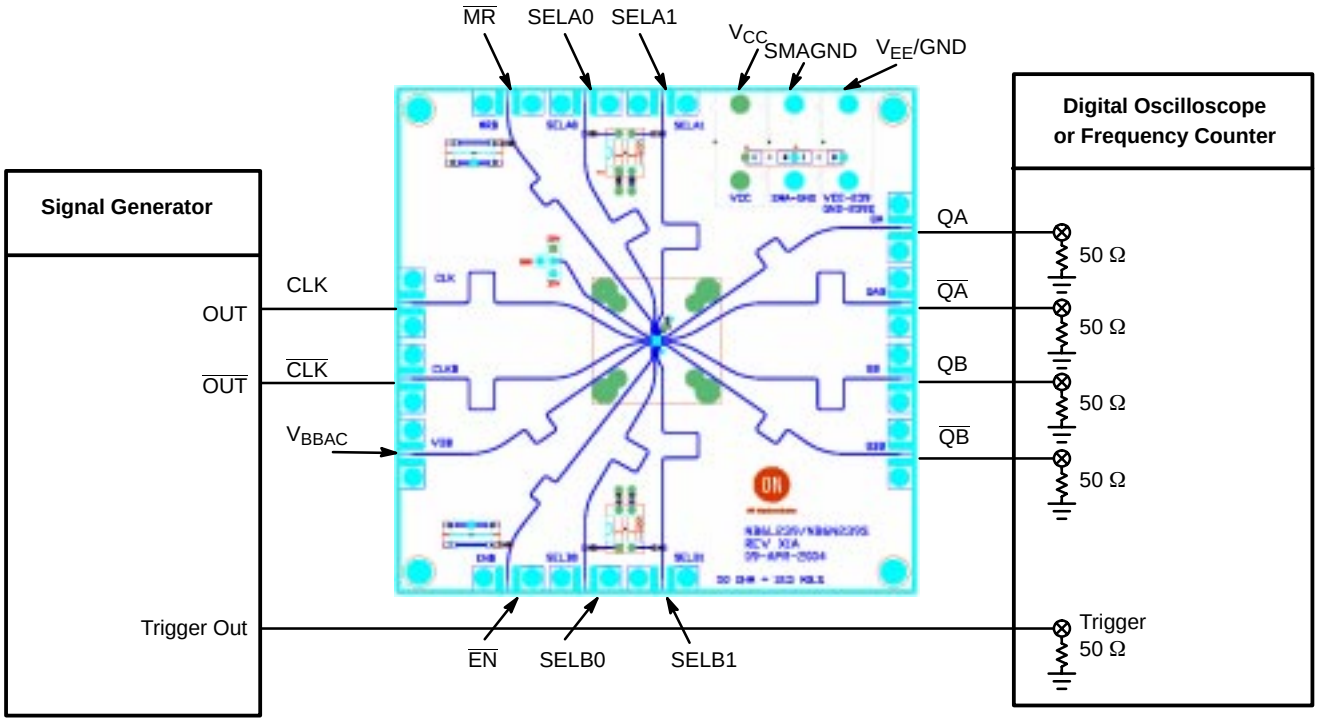


Figure 3. Evaluation Board

Board Layout

The evaluation board is constructed with Rogers material with 50 Ω trace impedances designed to minimize noise, achieve high bandwidth and minimize crosstalk.

Layer Stack

L1 Signal (top) (Rogers)
L2 SMA Ground
L3 V_{CC} and GND (positive and negative power supply)
L4 Signal (bottom)

Control and Select Pins

The Control / Select pins, $\overline{MR}$, SELXn and $\overline{EN}$, can be accessed via the appropriate SMA connector. These pins can also be manually controlled by using the H/L switch. When using the switch, the SMA connector should be left open. When using the SMA connector, the switch must be in the "OPEN" position.

The SELXn and $\overline{EN}$ device pins have internal pulldown resistors. The NB6N239S evaluation board was designed to take advantage of this attribute. When the SELXn and $\overline{EN}$ switch is in the logic LOW position, the input pin "floats" to a logic LOW owing to the pulldown resistor; a logic LOW voltage is not forced on the pin. In the HIGH position, the switch forces the SELXn and $\overline{EN}$ pin to the positive power supply rail, a logic HIGH.

The $\overline{MR}$ device pin has an internal pullup resistor. When the $\overline{MR}$ switch is in the logic HIGH position, the input pin "floats" to a logic HIGH owing to the pullup resistor; a logic HIGH voltage is not forced on the pin. In the LOW position, the switch forces the $\overline{MR}$ pin to the negative power supply rail, a logic LOW.

V_{BB} = V_{BBAC}

V_{BB} labeled on the board is actually V_{BBAC} per the data sheet.

V_T

The V_T pin can be set to V_{CC}, V_{EE} (239) GND (239S), V_{BB} or SMAGND by using a jumper.

V_{EE} / GND

V_{EE} is the negative supply for the NB6L239. GND is the negative supply for the NB6N239S.

Table 2. PIN DESCRIPTION (refer to data sheet, NB6N239S/D)

Pin # 16−QFN	Pin Name	I/O	Open Pin Default	Type	Function
1	VT				Internal 100 Ω Center
2	CLK	Input		LVPECL, CML, LVDS, HSTL	Noninverted Differential CLOCK Input.
3	$\overline{CLK}$	Input		LVPECL, CML, LVDS, HSTL	Inverted Differential CLOCK Input.
4	V_{BBAC}	Output		Reference Voltage	Output Voltage Reference for Capacitor Coupled Inputs, Only.
5	$\overline{EN}$	Input	L	LVCMOS/LVTTL Input	Synchronous Output Enable
6	SELB0	Input	L	LVCMOS/LVTTL Input	Clock Divide Select Pin
7	SELB1	Input	L	LVCMOS/LVTTL Input	Clock Divide Select Pin
8	GND	Negative Power Supply			Negative Supply Voltage
9	$\overline{QB}$	Output		LVDS	Inverted Differential Output. Typically terminated with 100 Ω resistor across outputs.
10	QB	Output		LVDS	Noninverted Differential Output. Typically terminated with 100 Ω resistor across outputs.
11	$\overline{QA}$	Output		LVDS	Inverted Differential Output. Typically terminated with 100 Ω resistor across outputs.
12	QA	Output		LVDS	Noninverted Differential Output. Typically terminated with 100 Ω resistor across outputs.
13	V_{CC}	Positive Power Supply			Positive Power Supply
14	SELA1	Input	L	LVCMOS/LVTTL	Clock Divide Select Pin
15	SELA0	Input	L	LVCMOS/LVTTL Input	Clock Divide Select Pin
16	$\overline{MR}$	Input	H	LVCMOS/LVTTL Input	Master Reset Asynchronous, Default Open High, Asserted LOW
	EP	Negative Power Supply (opt)			The Exposed Pad on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

Evaluation Board Application Information

Table 3. Evaluation Board Bill of Materials

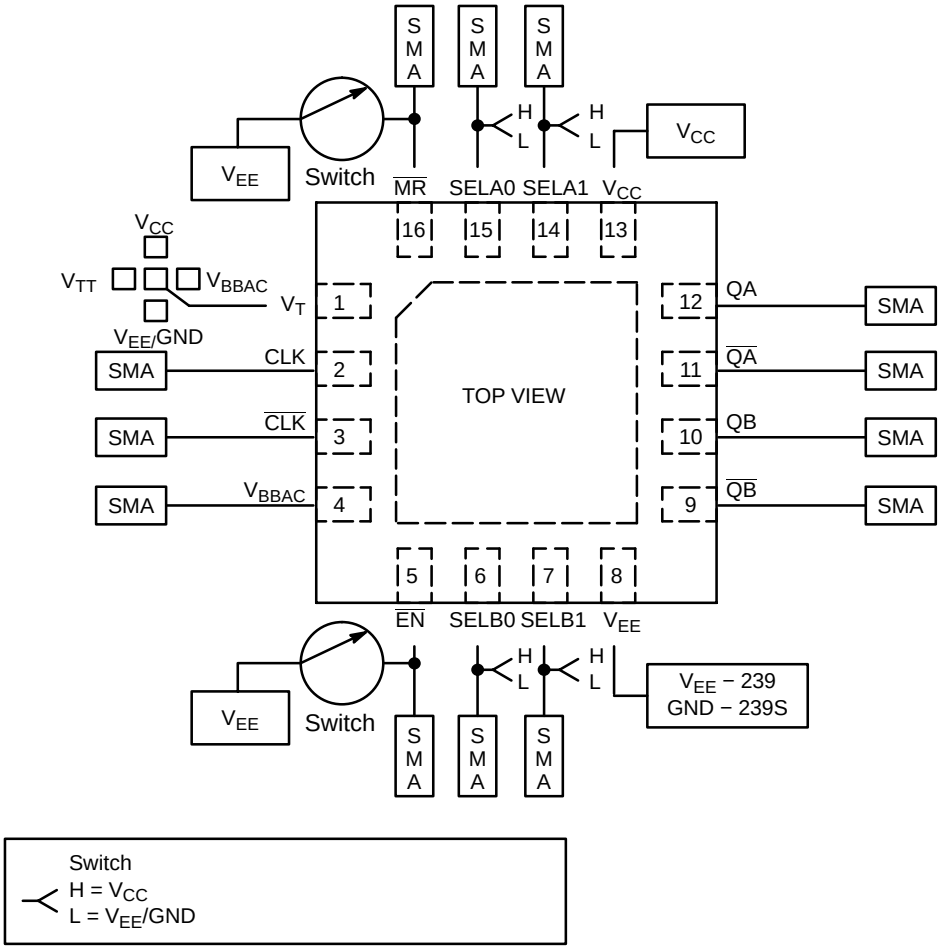
Component	Description	Qty
Connectors	Rosenberger SMA #32K243−40ME3	6
Capacitors	22 μF	2
Capacitors	0.01 μF	4
Switches	Grayhill #78B02	4
Jumper Header		5
Jumper		1
Resistor	1 kΩ	6
Banana Jack	Deltron #EF681 150−039 Red	1
Banana Jack	Deltron #EF681 150−040 Black	1
Banana Jack	Deltron #EF681 150−043 Yellow	1
Stand−offs w/screws		4
NB6N239S	QFN−16 part mounted on board	1

Table 4. Bill of Materials

Type	Description	Tolerance (%)	Wattage	Manufacturer	Part Number	Qty
Capacitor	0.1 μF	10	0.062	KEMET	C060C104K5RAC	2
Capacitor	22 μF	10	0.062	KEMET	T491D226K016AS	2
Connector	SMA	−	−	Johanson	142−0701−801	6
Jumper Header	100 mil	−	−	Berg	−	6
Resistor	50	0.1	0.25	DALE	−	2
Socket	16 LD QFN	−	−	M&M	50−000−00350	1

Table 5.

Pin	Description
C1, C3	0.1 μF Surface Mount, 0603
C2, C4	22 μF Surface Mount Electrolytic, Case 0603
R1, R2	50 Surface Mount, 0603



Standoffs
Rosenberger connectors with matched trace launches
Switch for $\overline{MR}$
Normally open switch for $\overline{EN}$
CLK & $\overline{CLK}$ traces – equal length
All Q Output traces – equal length
"Side−mount" banana jacks for power supplies (can be located on backside of board)
V_T pin has a jumper capability to V_{CC}, V_{EE} / GND, V_{TT} (SMAGND), or V_{BBAC}.

Figure 4. Evaluation Demo Board

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
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