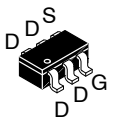
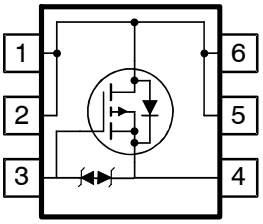
MOSFET – P-Channel, POWERTRENCH®

2.5 V Specified

FDC608PZ, FDC608PZ-F171



TSOT–23–6
CASE 419BL



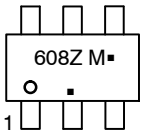
Description

This P–Channel 2.5 V specified MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on–state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for battery power applications: load switching and power management, battery power circuits, and dc–dc conversions.

Features

- –5.8 A, –20 V. $R_{DS(ON)}$ = 30 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 43 mΩ @ V_{GS} = –2.5 V
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SuperSOT ™ –6 Package: Small Footprint (72% Smaller than Standard SO–8) Low Profile (1 mm Thick)
- These Devices are Pb–Free and Halide Free

MARKING DIAGRAM



608Z = Specific Device Code
M = Date Code
▪ = Pb–Free Package

(Note: Microdot may be in either location)

ABSOLUTE MAXIMUM RATINGS

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain–Gate Voltage	–20	V
V_{GSS}	Gate–Source Voltage	±12	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	–5.8 –20	A
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	1.6 0.8	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case (Note 1)	30	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
FDC608PZ	TSOT–23–6 (Pb-Free/ Halide Free)	3000 / Tape & Reel
FDC608PZ–F171	TSOT–23–6 (Pb-Free/ Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	−10	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16 V, V_{GS} = 0 V	–	–	−1	μA
I_{GSS}	Gate−Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−0.4	−1.0	−1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	3	–	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −4.5 V, I_D = −5.8 A	–	26	30	mΩ
		V_{GS} = −2.5 V, I_D = −5.0 A	–	38	43	
		V_{GS} = −4.5 V, I_D = −5.8 A, T_J = 125°C	–	35	–	
$I_{D(on)}$	On−State Drain Current	V_{GS} = −4.5 V, V_{DS} = −5 V	−20	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = −10 V, I_D = −5.8 A	–	22	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −10 V, V_{GS} = 0 V, f = 1.0 MHz	–	1330	–	pF
C_{oss}	Output Capacitance		–	270	–	pF
C_{rss}	Reverse Transfer Capacitance		–	230	–	pF
R_G	Input Capacitance	V_{GS} = 15 mV, f = 1.0 MHz	–	12	–	Ω
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −10 V, I_D = −1 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω	–	13	24	ns
t_r	Turn−On Rise Time		–	8	16	ns
$t_{d(off)}$	Turn−Off Delay Time		–	91	145	ns
t_f	Turn−Off Fall Time		–	60	96	ns
Q_g	Total Gate Charge	V_{DS} = −10 V, I_D = −5.8 A, V_{GS} = −4.5 V	–	17	23	nC
Q_{gs}	Gate−Source Charge		–	3	–	nC
Q_{gd}	Gate−Drain Charge		–	6	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	−1.3	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −1.3 A (Note 2)	–	−0.7	−1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = −5.8 A, d_{iF}/d_t = 100 A/μs	–	40	60	ns
Q_{rr}	Diode Reverse Recovery Charge	I_F = −5.8 A, d_{iF}/d_t = 100 A/μs	–	15	23	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
   a. 78°C/W when mounted on a 1 in^2 pad of 2oz copper on FR−4 board.
   b. 156°C/W when mounted on a minimum pad.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤2.0%.

TYPICAL CHARACTERISTICS

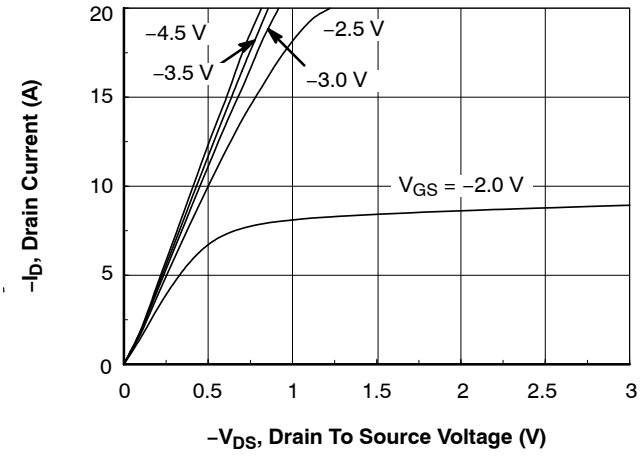


Figure 1. On−Region Characteristics

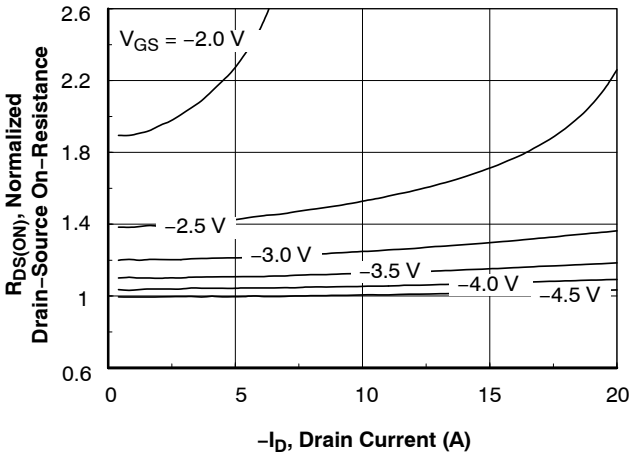


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

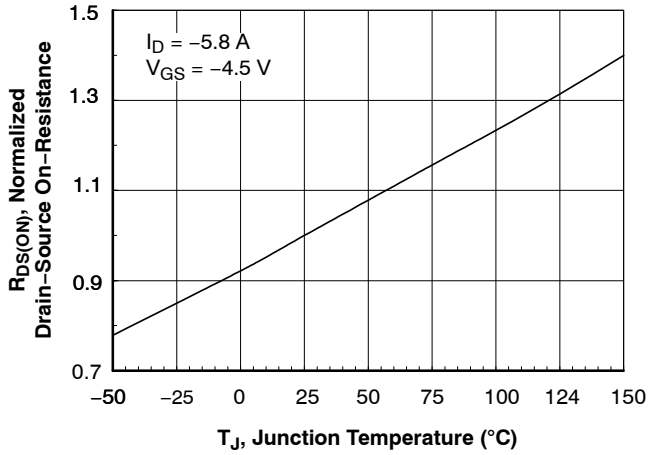


Figure 3. On-Resistance Variation With Temperature

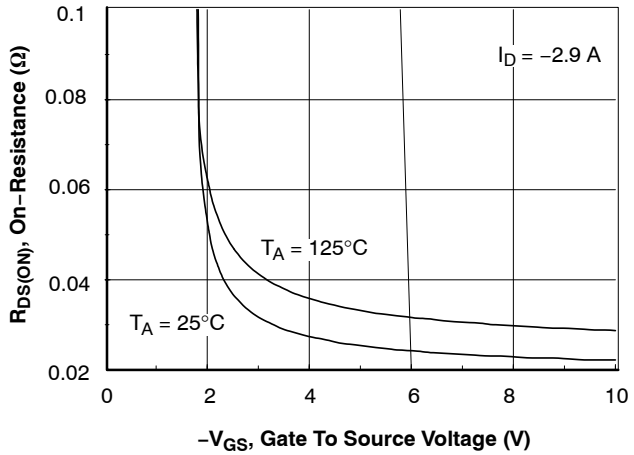


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

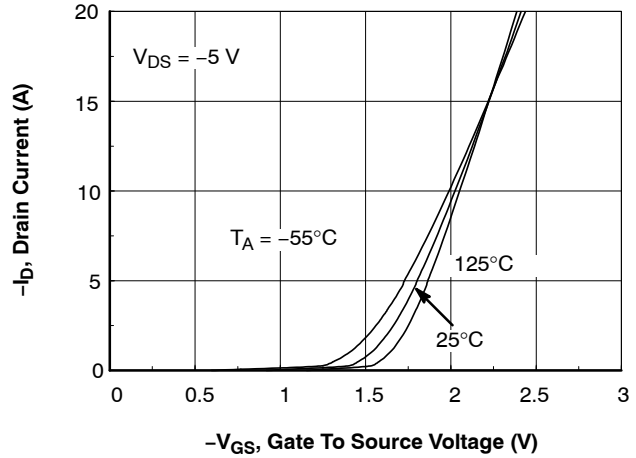


Figure 5. Transfer Characteristics

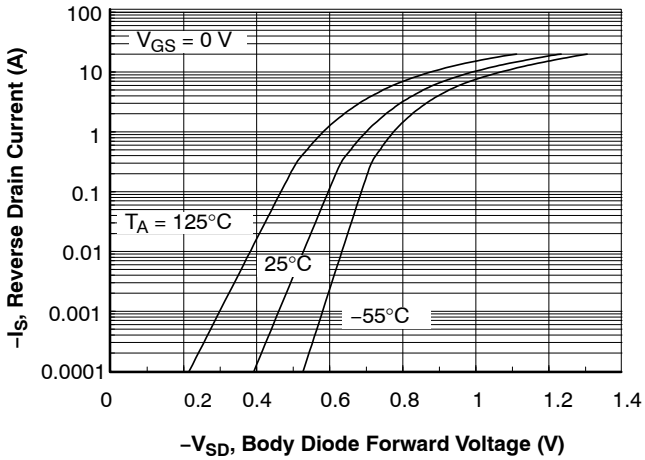


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

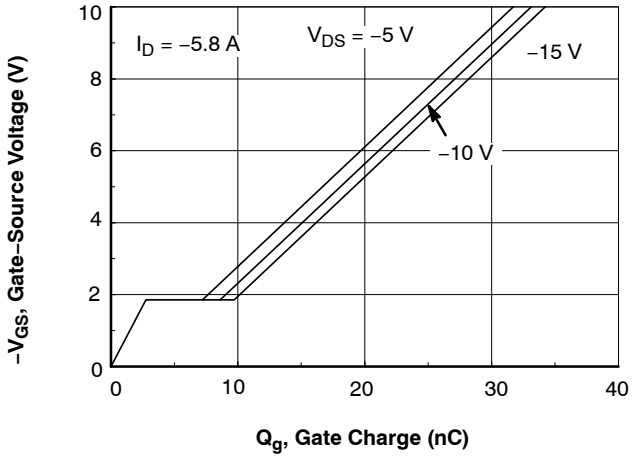


Figure 7. Gate Charge Characteristics

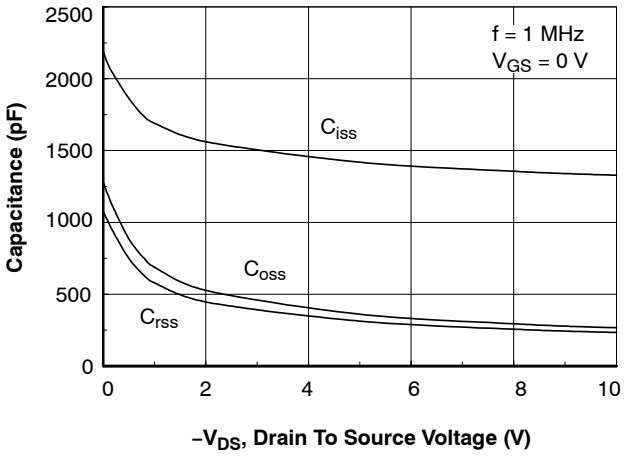


Figure 8. Capacitance Characteristics

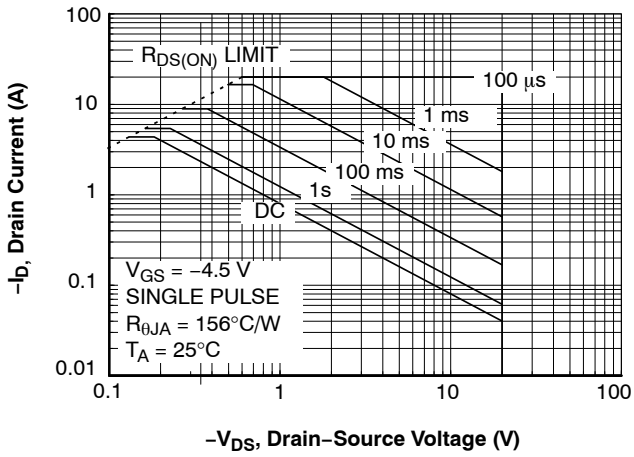


Figure 9. Maximum Safe Operating Area

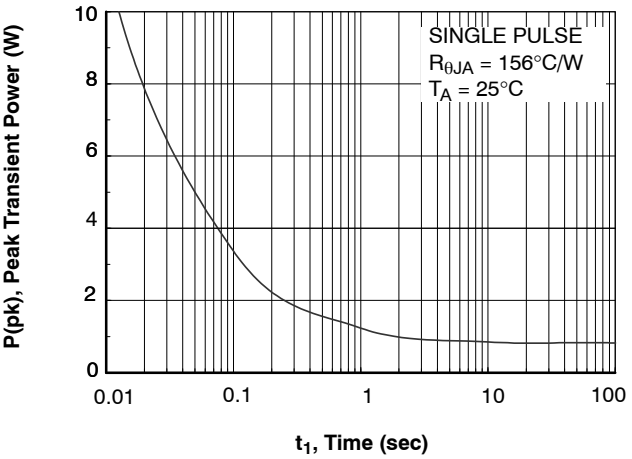


Figure 10. Single Pulse Maximum Power Dissipation

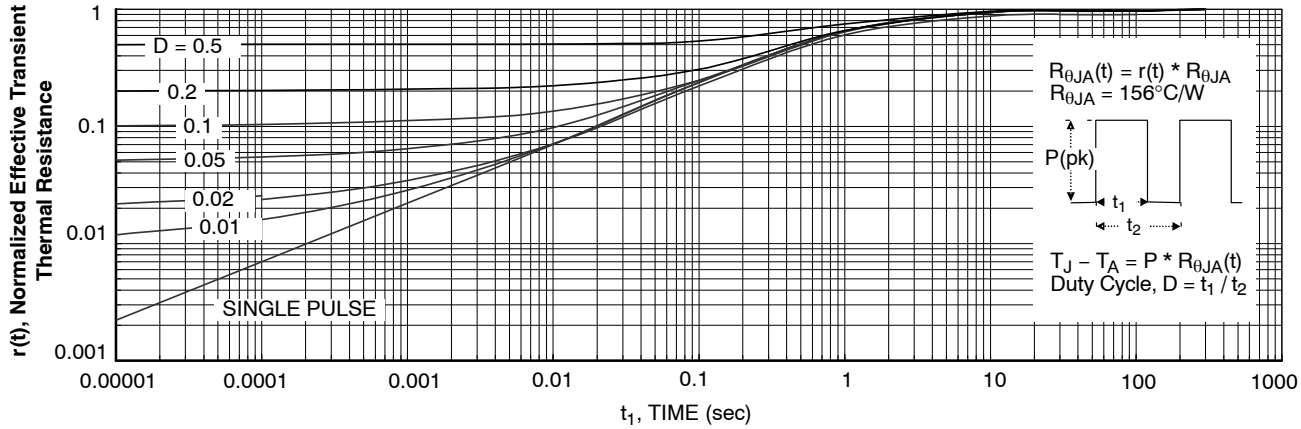


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

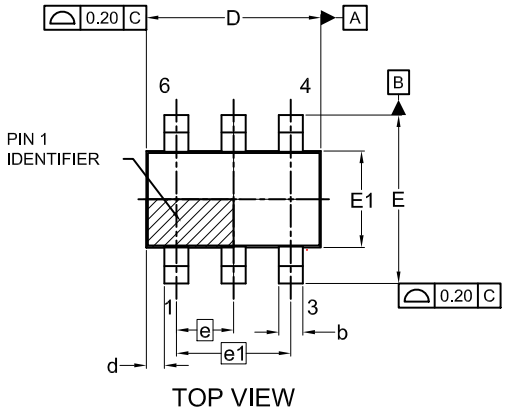
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

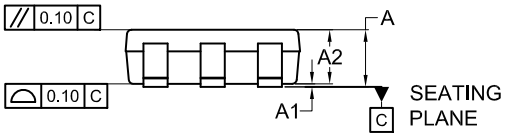
TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

SCALE 2:1

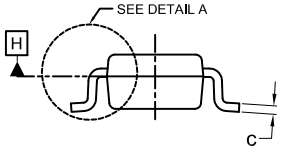


TOP VIEW

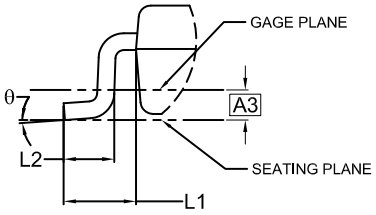


FRONT VIEW

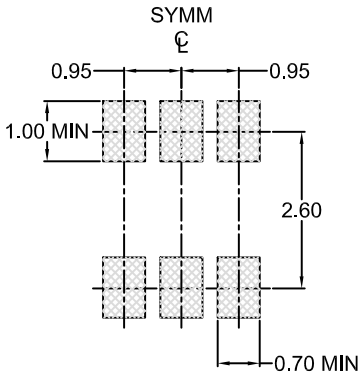
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

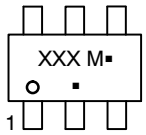
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6−Lead	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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