Ordering number : ENN7549

N-Channel and P-Channel Silicon MOSFETs

FW359

Ultrahigh-Speed Switching Applications

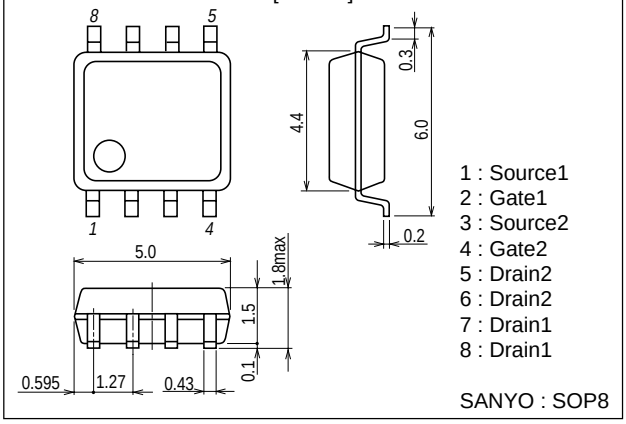
Features

- The FW359 in corporates a N-channel MOSFET and a P-channel MOSFET that feature low ON-resistance, ultrahigh-speed switching, and 4V drive, thereby enabling high-density mounting.
- Excellent ON-resistance characteristic.

Package Dimensions

unit : mm

2129



Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings		Unit
			N-channel	P-channel	
Drain-to-Source Voltage	V_{DSS}		60	−60	V
Gate-to-Source Voltage	V_{GSS}		±20	±20	V
Drain Current (DC)	I_D		3	−3	A
Drain Current (PW=10s)	I_D	duty cycle≤1%	3.5	−3.5	A
Drain Current (PW=100ms)	I_D	duty cycle≤1%	5.5	−5.5	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	14	−14	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (2000mm²X0.8mm)1unit, PW≤10s	1.8		W
Total Dissipation	P_T	Mounted on a ceramic board (2000mm²X0.8mm), PW≤10s	2.2		W
Channel Temperature	Tch		150		°C
Storage Temperature	Tstg		−55 to +150		°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[N-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0			1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	1.2		2.6	V

Marking : W359

Continued on next page.

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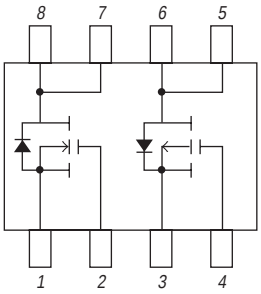
Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Forward Transfer Admittance	|yfs|	V_{DS}=10V, I_D=3A	2.8	4		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=3A, V_{GS}=10V		110	145	mΩ
	R_{DS}(on)2	I_D=1.5A, V_{GS}=4V		150	215	mΩ
Input Capacitance	Ciss	V_{DS}=20V, f=1MHz		300		pF
Output Capacitance	Coss	V_{DS}=20V, f=1MHz		54		pF
Reverse Transfer Capacitance	Crss	V_{DS}=20V, f=1MHz		34		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		8		ns
Rise Time	t_r	See specified Test Circuit.		23		ns
Turn-OFF Delay Time	t_d(off)	See specified Test Circuit.		30		ns
Fall Time	t_f	See specified Test Circuit.		40		ns
Total Gate Charge	Qg	V_{DS}=30V, V_{GS}=10V, I_D=3A		7.8		nC
Gate-to-Source Charge	Qgs	V_{DS}=30V, V_{GS}=10V, I_D=3A		2.4		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=30V, V_{GS}=10V, I_D=3A		1.7		nC
Diode Forward Voltage	V_{SD}	I_S=3A, V_{GS}=0		0.86	1.2	V
[P-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-1mA, V_{GS}=0	-60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V, V_{GS}=0			-1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=-10V, I_D=-1mA	-1.2		-2.6	V
Forward Transfer Admittance	|yfs|	V_{DS}=-10V, I_D=-3A	4	5.5		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=-3A, V_{GS}=-10V		110	145	mΩ
	R_{DS}(on)2	I_D=-1.5A, V_{GS}=-4V		145	205	mΩ
Input Capacitance	Ciss	V_{DS}=-20V, f=1MHz		990		pF
Output Capacitance	Coss	V_{DS}=-20V, f=1MHz		110		pF
Reverse Transfer Capacitance	Crss	V_{DS}=-20V, f=1MHz		76		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		12		ns
Rise Time	t_r	See specified Test Circuit.		70		ns
Turn-OFF Delay Time	t_d(off)	See specified Test Circuit.		100		ns
Fall Time	t_f	See specified Test Circuit.		70		ns
Total Gate Charge	Qg	V_{DS}=-30V, V_{GS}=-10V, I_D=-3A		22		nC
Gate-to-Source Charge	Qgs	V_{DS}=-30V, V_{GS}=-10V, I_D=-3A		4		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=-30V, V_{GS}=-10V, I_D=-3A		4		nC
Diode Forward Voltage	V_{SD}	I_S=-3A, V_{GS}=0		-0.86	-1.2	V

Electrical Connection

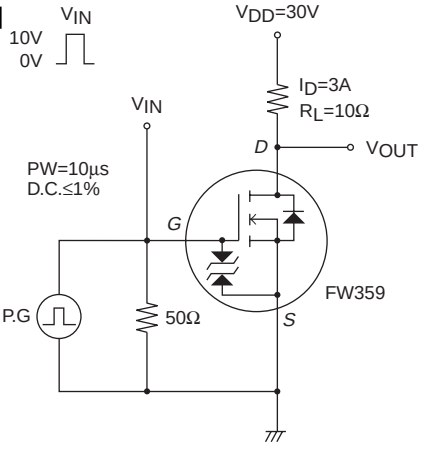


1 : Source1
2 : Gate1
3 : Source2
4 : Gate2
5 : Drain2
6 : Drain2
7 : Drain1
8 : Drain1

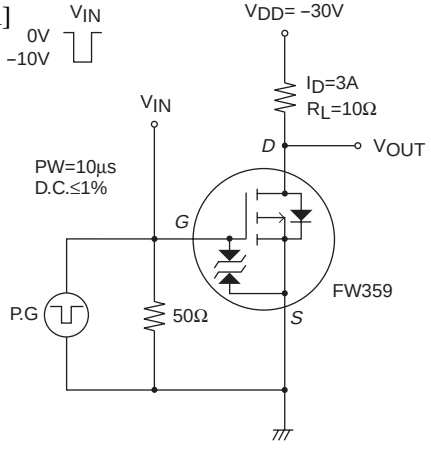
(Top view)

Switching Time Test Circuit

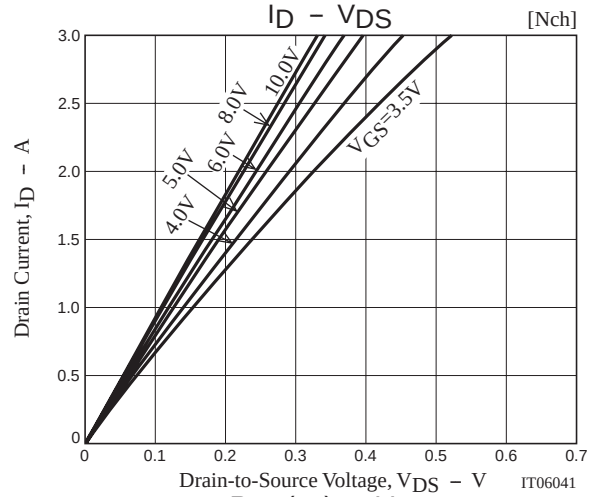
[N-channel]



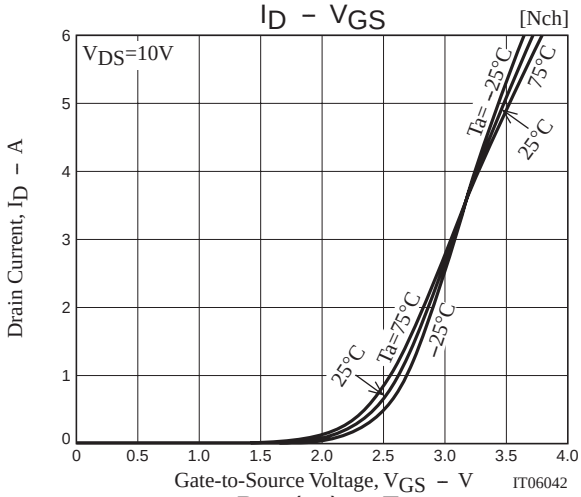
[P-channel]



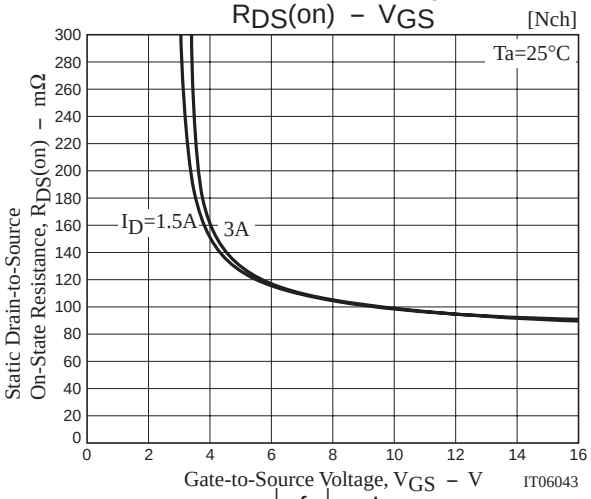
I_D – V_{DS} [Nch]



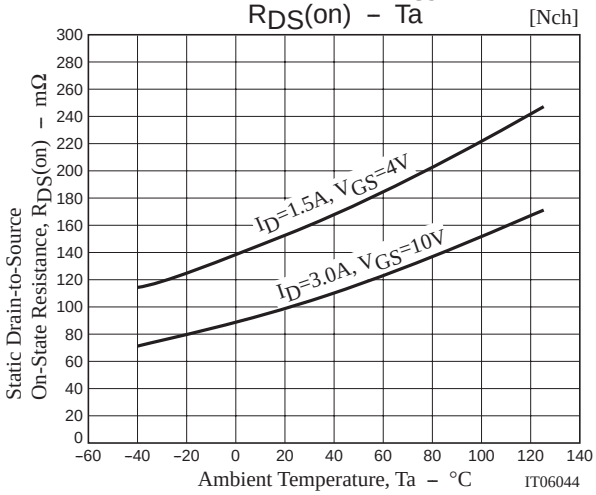
I_D – V_{GS} [Nch]



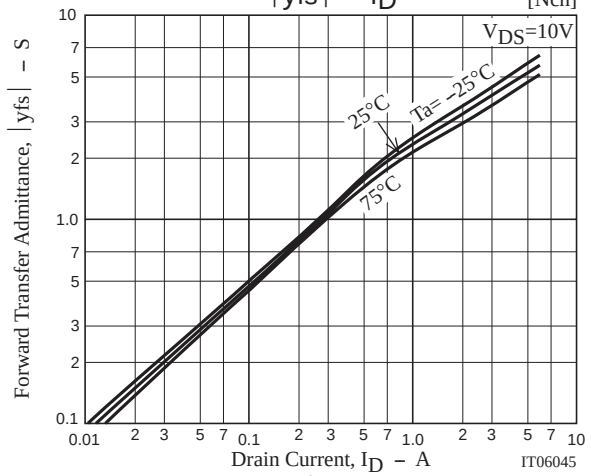
$R_{DS}(on)$ – V_{GS} [Nch]



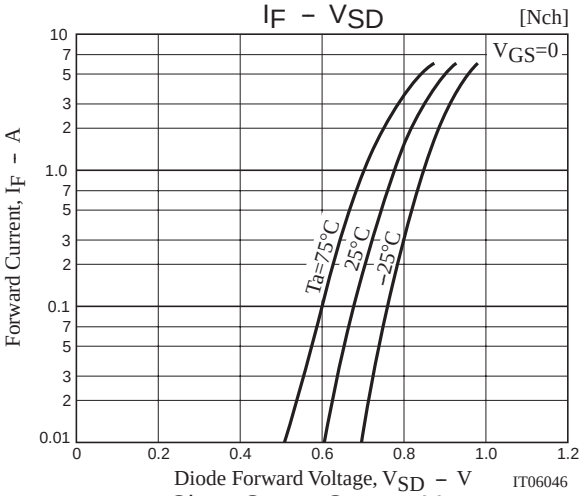
$R_{DS}(on)$ – Ta [Nch]



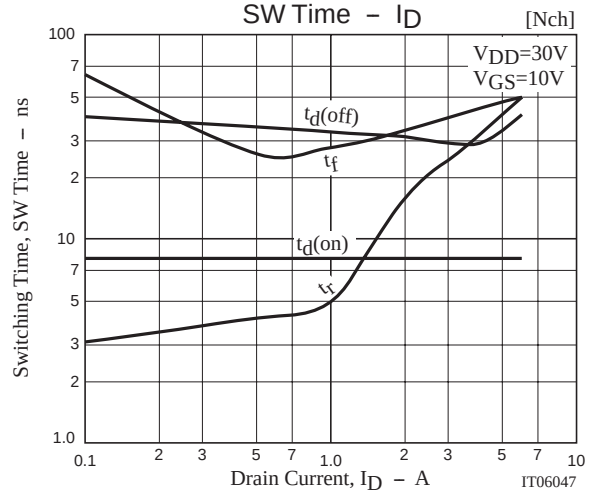
$|yfs|$ – I_D [Nch]



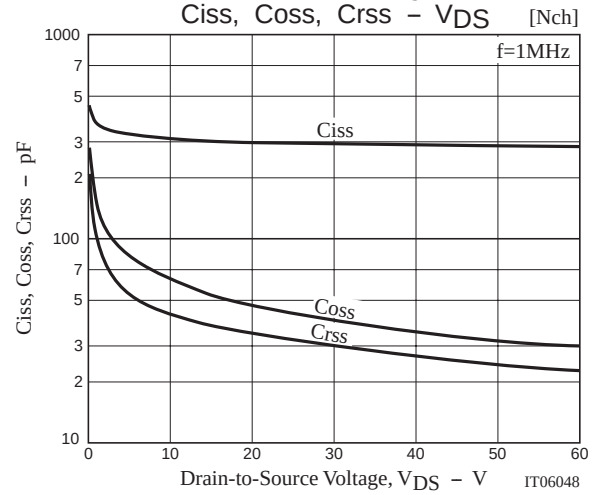
I_F – V_{SD} [Nch]

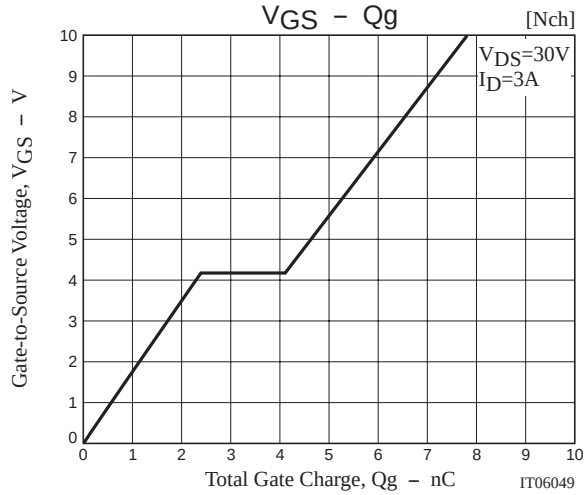


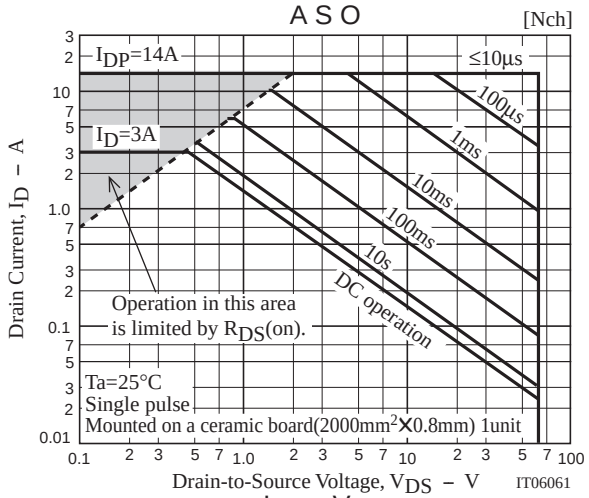
SW Time – I_D [Nch]

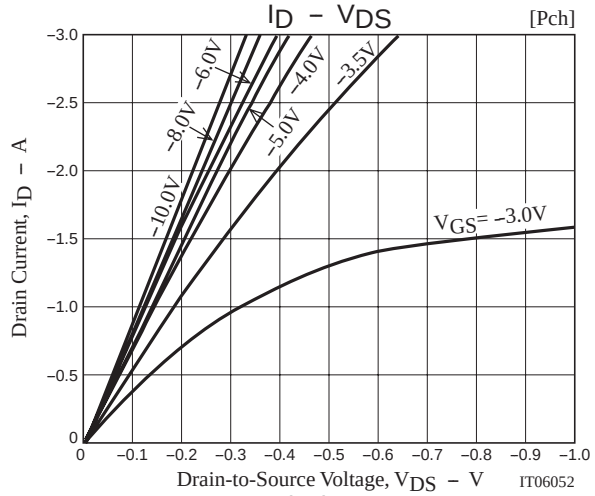


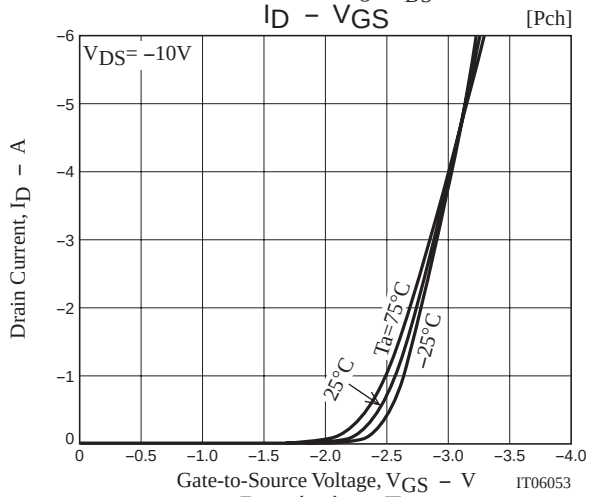
Ciss, Coss, Crss – V_{DS} [Nch]

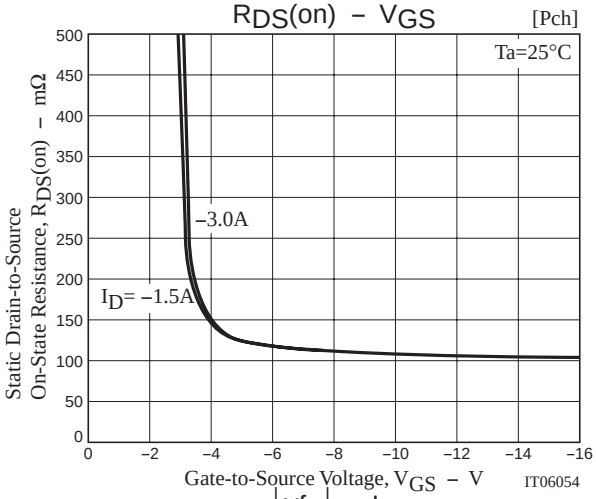


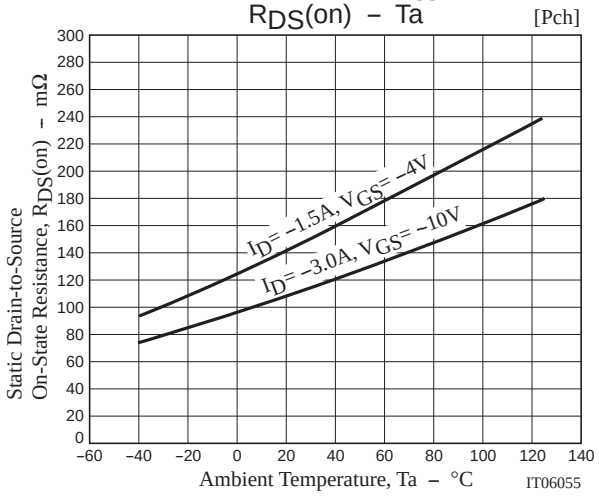


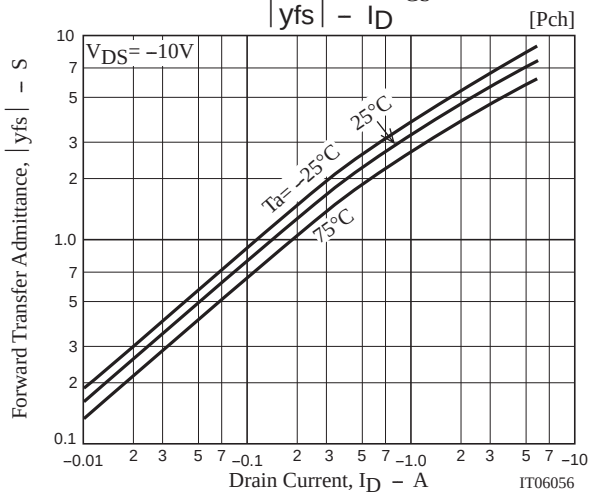


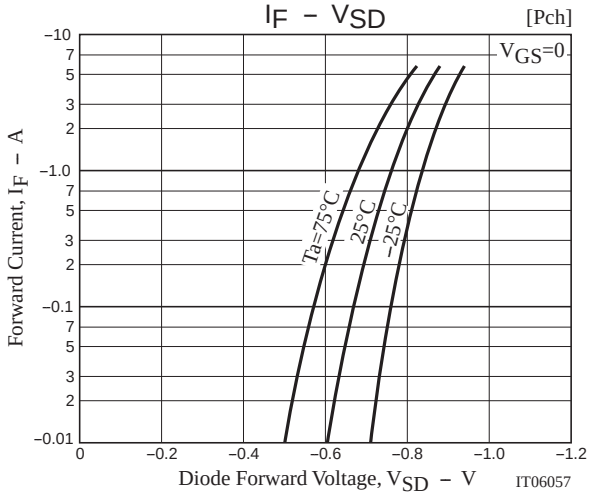




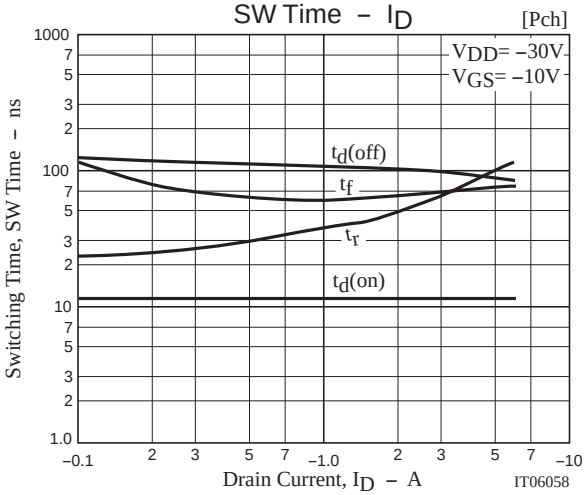




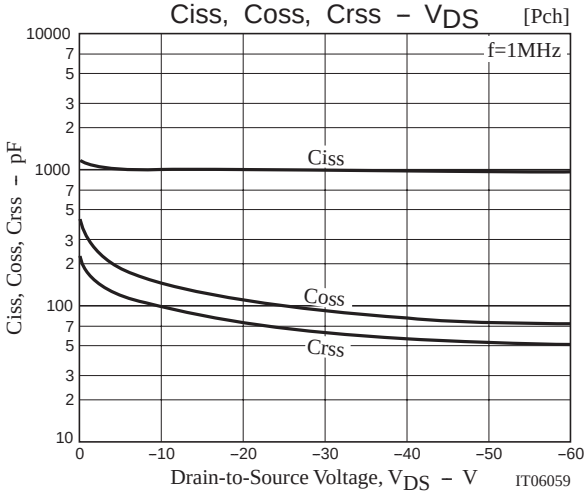




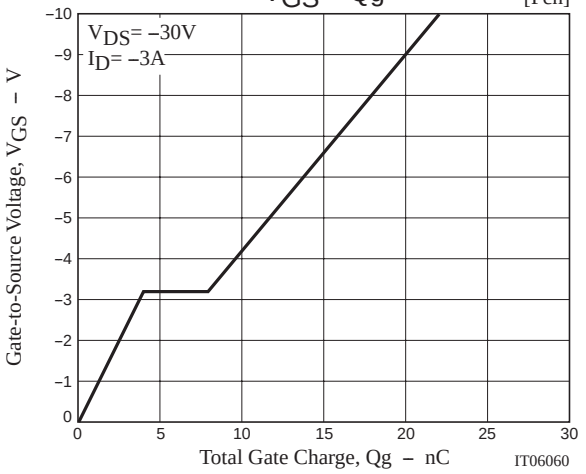
SW Time – I_D [Pch]



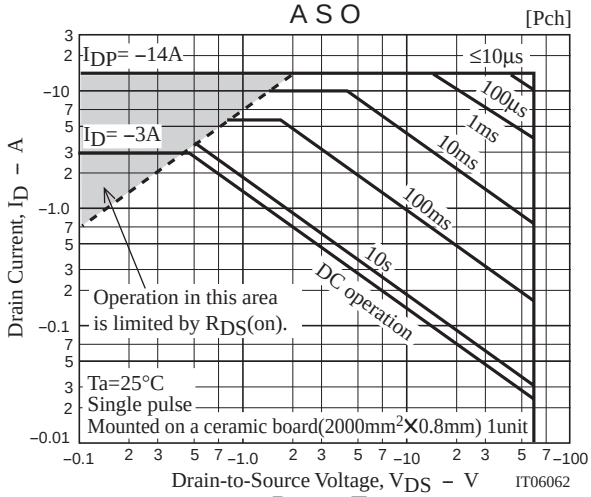
Ciss, Coss, Crss – V_{DS} [Pch]



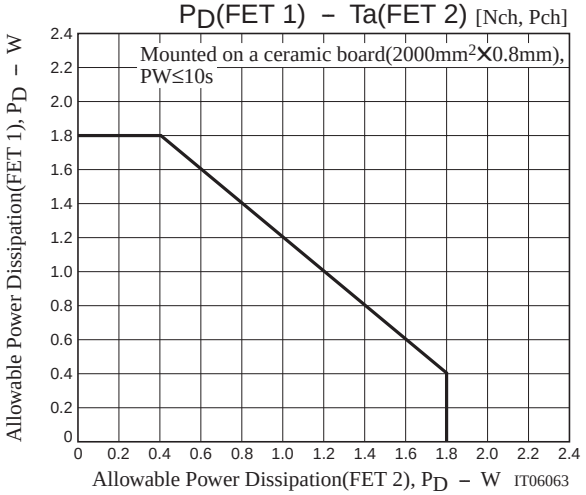
V_{GS} – Qg [Pch]



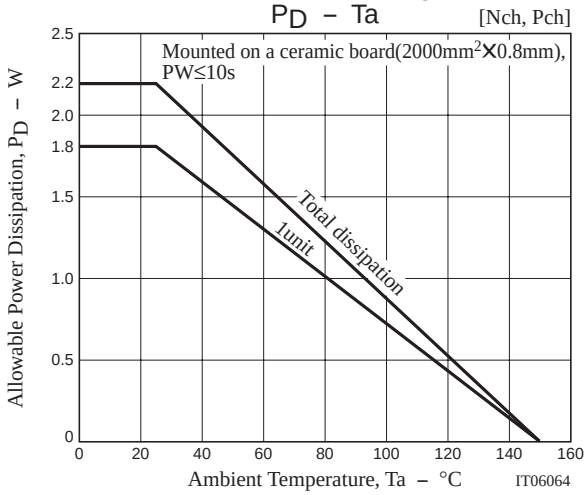
A S O [Pch]



P_D(FET 1) – Ta(FET 2) [Nch, Pch]



P_D – Ta [Nch, Pch]



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