MOSFET - Power, Single N-Channel, μ8FL
30 V, 17 mΩ, 22 A

NVTFS4C25N

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C25NWF – Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 5)	Steady State	T_A = 25°C	I_D	10.1	A
		T_A = 85°C		7.8	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3, 5)		T_A = 25°C	P_D	3.0	W
		T_A = 85°C		1.8	
Continuous Drain Current $R_{\psi JC}$ (Notes 1, 2, 4, 5)	Steady State	T_C = 25°C	I_D	22.1	A
		T_C = 85°C		17.1	
Power Dissipation $R_{\psi JC}$ (Notes 1, 2, 4, 5)		T_C = 25°C	P_D	14.3	W
		T_C = 85°C		8.6	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	90	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	14	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, I_L = 6.7 A_{pk}, L = 0.5 mH)			E_{AS}	11.2	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown; they are not constants and are valid for the specific conditions noted.
2. Psi (ψ) is used as required per JESD51−12 for packages in which substantially less than 100% of the heat flows to a single case surface.
3. Surface−mounted on FR4 board using 650 mm^2, 2 oz. Cu Pad.
4. Assumes heat−sink sufficiently large to maintain constant case temperature independent of device power.
5. Continuous DC current rating. Maximum current for pulses as long as one second is higher but dependent on pulse duration and duty cycle.

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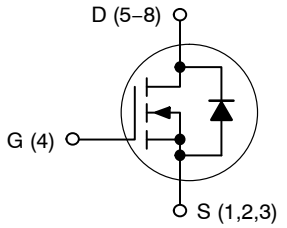
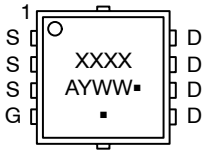
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	17 mΩ @ 10 V	22 A
	26.5 mΩ @ 4.5 V	

N−Channel MOSFET



WDFN8
(μ8FL)
CASE 511AB

MARKING DIAGRAM



4C25	= Specific Device Code for NVMTS4C25N
25WF	= Specific Device Code of NVTFS4C25NWF
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain) (Notes 6, 7 and 9)	$\Psi_{\theta JC}$	10.5	°C/W
Junction−to−Ambient − Steady State (Notes 6 and 8)	$R_{\theta JA}$	50	

6. The entire application environment impacts the thermal resistance values shown; they are not constants and are valid for the specific conditions noted.
7. Psi (ψ) is used as required per JESD51−12 for packages in which substantially less than 100% of the heat flows to a single case surface.
8. Surface−mounted on FR4 board using 650 mm^2, 2 oz. Cu Pad.
9. Assumes heat−sink sufficiently large to maintain constant case temperature independent of device power.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				15.3		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 10)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.3		2.2	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−4.5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 10 A		13	17	mΩ
		V_{GS} = 4.5 V	I_D = 9 A		21	26.5	
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 15 A			23		S
Gate Resistance	R_G	T_A = 25°C			1.0		Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V			500		pF
Output Capacitance	C_{OSS}				295		
Reverse Transfer Capacitance	C_{RSS}				85		
Capacitance Ratio	C_{RSS}/C_{ISS}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz			0.170		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 20 A			5.1		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.9		
Gate−to−Source Charge	Q_{GS}				1.7		
Gate−to−Drain Charge	Q_{GD}				2.7		
Gate Plateau Voltage	V_{GP}				3.3		V
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 20 A			10.3		nC
SWITCHING CHARACTERISTICS (Note 11)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 10 A, R_G = 3.0 Ω			8.0		ns
Rise Time	t_r				32		
Turn−Off Delay Time	$t_{d(OFF)}$				10		
Fall Time	t_f				3.0		
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			4.0		ns
Rise Time	t_r				25		
Turn−Off Delay Time	$t_{d(OFF)}$				13		
Fall Time	t_f				2.0		

10. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
11. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.87	1.2	V
			T_J = 125°C		0.75		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 30 A			18.2		ns
Charge Time	t_a				9.8		
Discharge Time	t_b				8.4		
Reverse Recovery Charge	Q_{RR}				5.7		nC

10. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
11. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

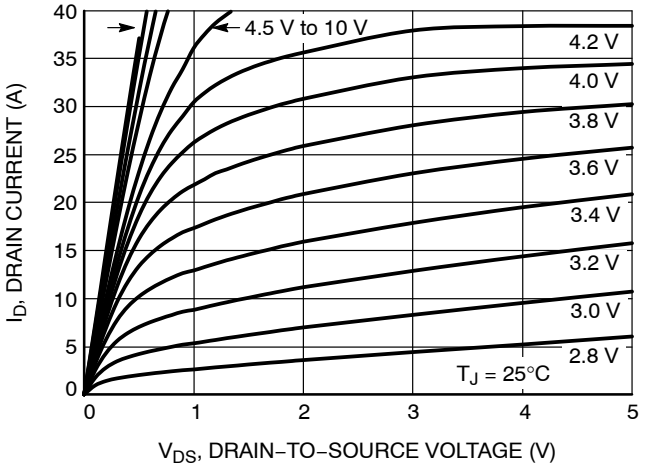


Figure 1. On−Region Characteristics

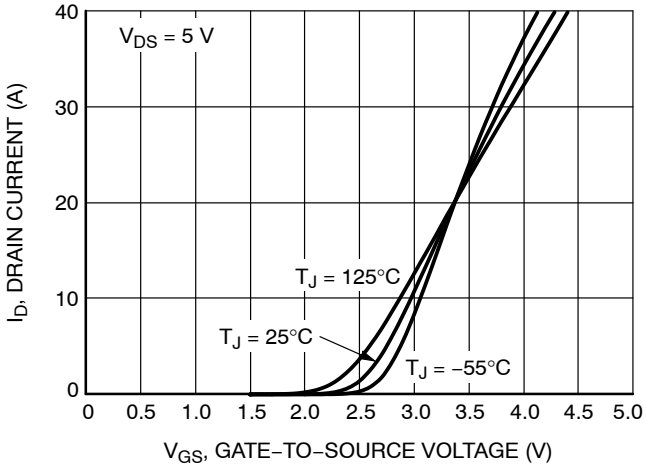


Figure 2. Transfer Characteristics

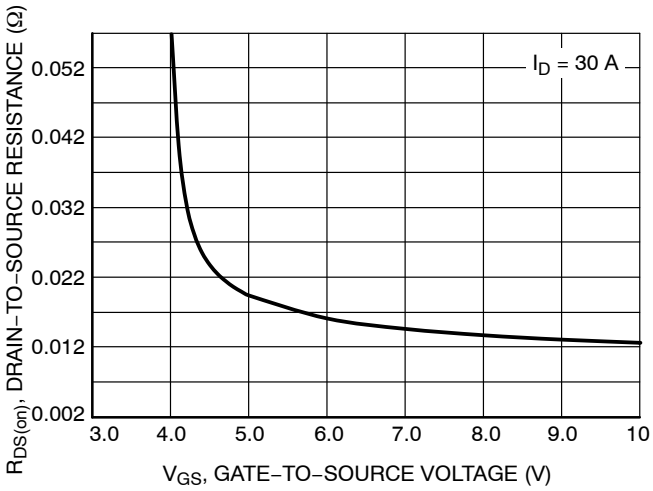


Figure 3. On−Resistance vs. V_{GS}

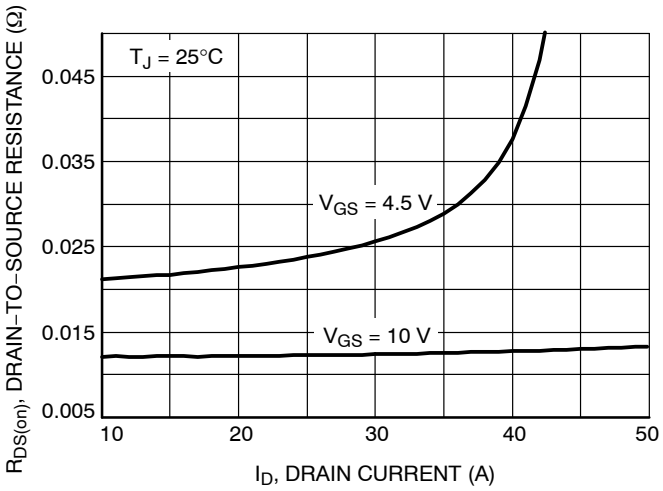


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

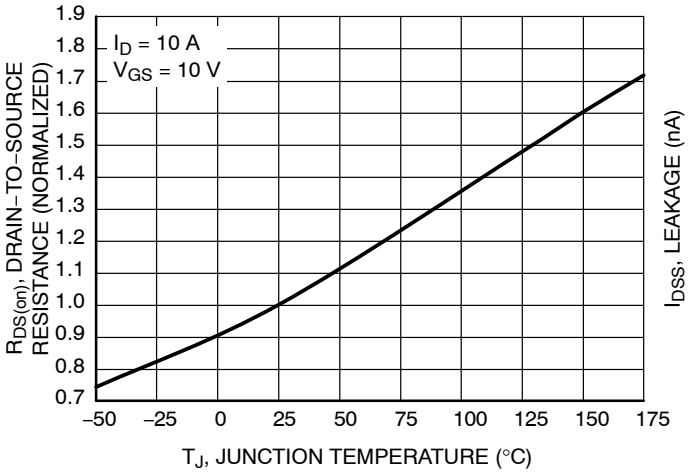


Figure 5. On−Resistance Variation with Temperature

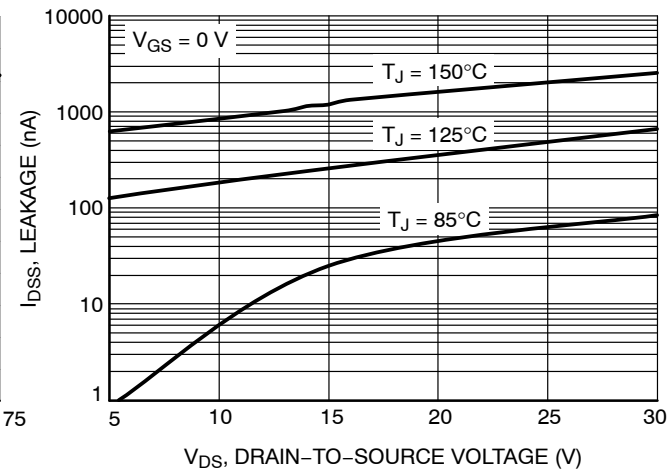


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

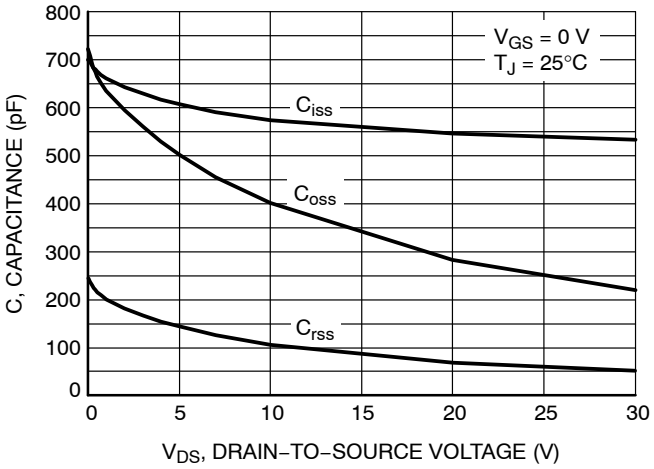


Figure 7. Capacitance Variation

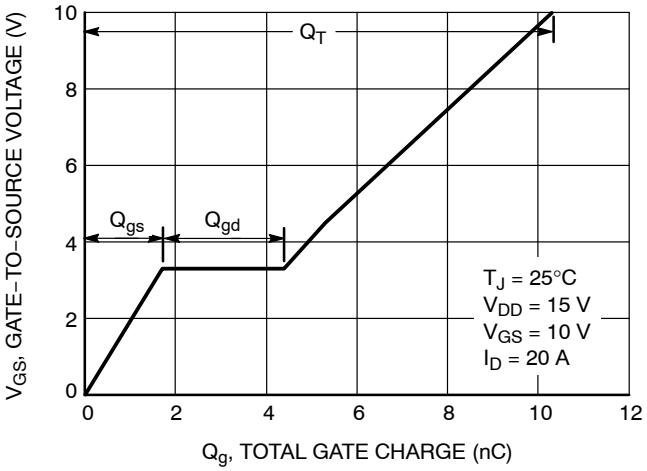


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

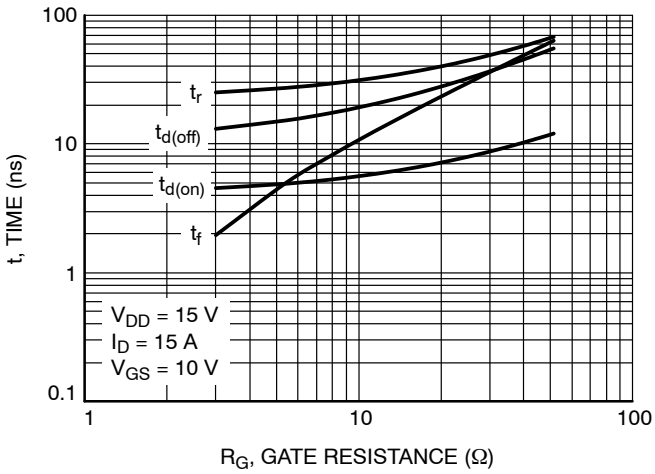


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

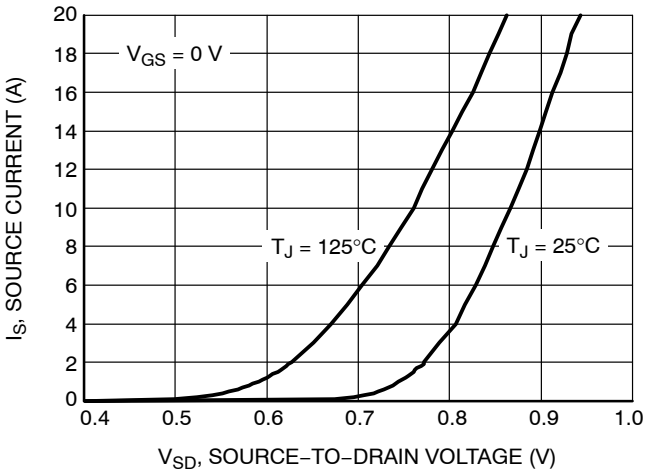


Figure 10. Diode Forward Voltage vs. Current

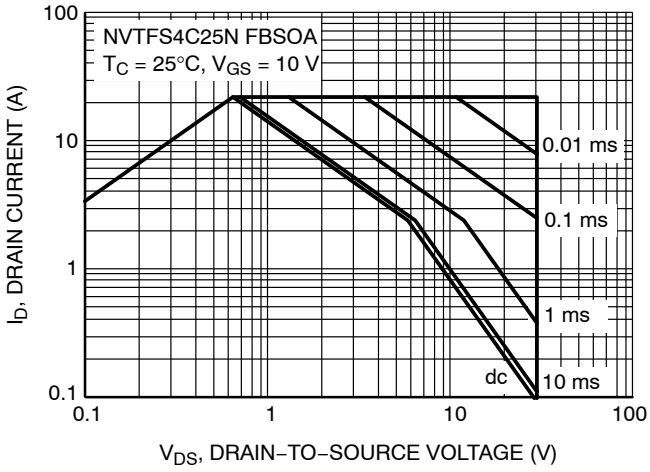


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

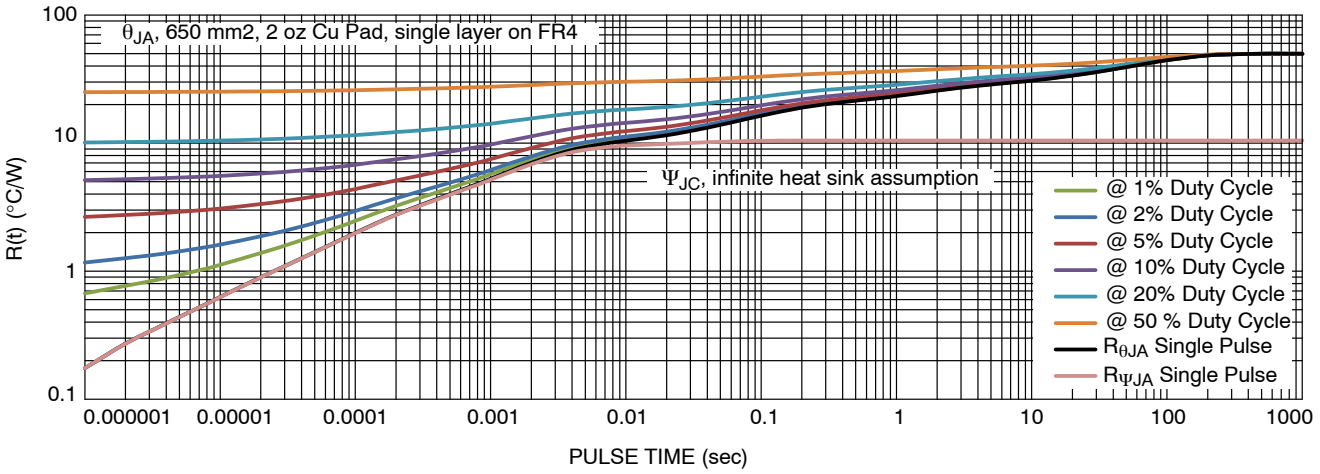


Figure 12. Thermal Response

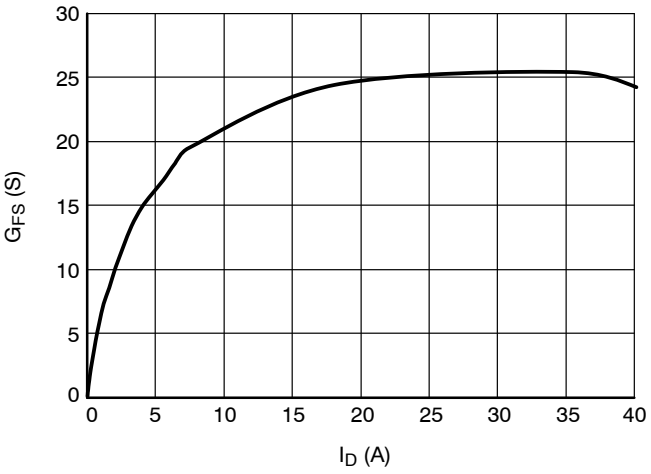


Figure 13. G_{FS} vs. I_D

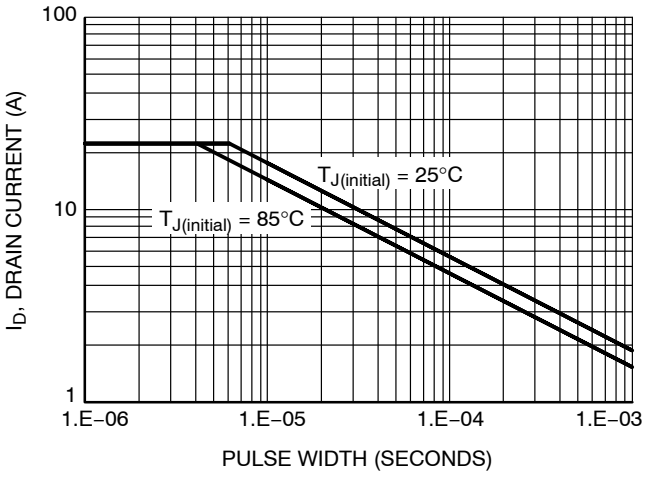


Figure 14. Avalanche Characteristics

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVTFS4C25NTAG	4C25	WDFN8 (Pb−Free)	1500 / Tape & Reel
NVTFS4C25NWFTAG	25WF	WDFN8 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

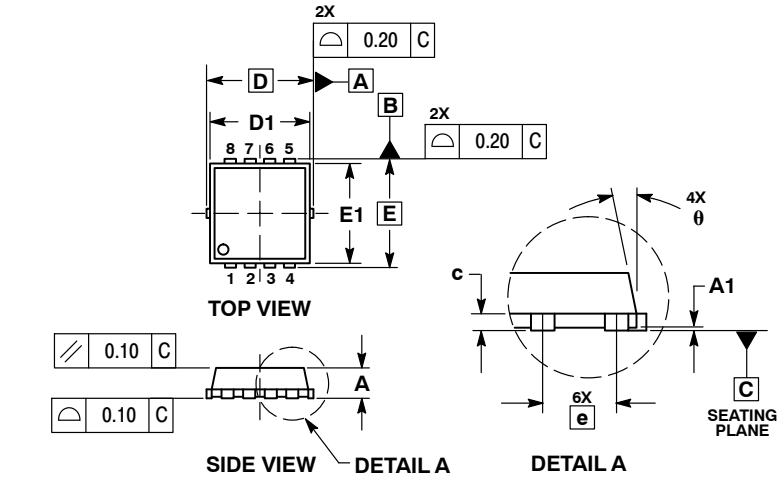
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

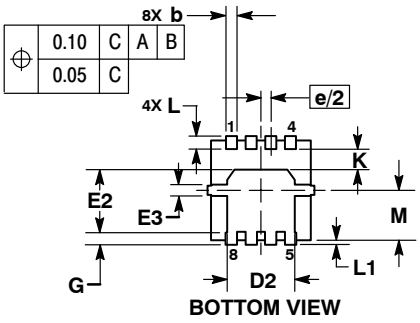
DATE 23 APR 2012

SCALE 2:1

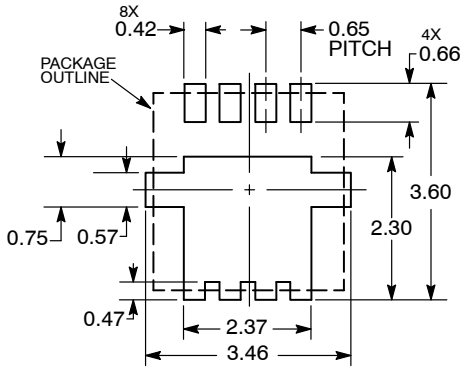


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D		3.30 BSC			0.130 BSC	
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E		3.30 BSC			0.130 BSC	
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e		0.65 BSC			0.026 BSC	
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °



SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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