

# MOSFET – N-Channel, POWERTRENCH®

**80 V, 80 A, 4.5 mΩ**

## FDWS86368-F085

### Features

- Typical  $R_{DS(on)}$  = 3.7 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 80 A
- Typical  $Q_{g(tot)}$  = 57 nC at  $V_{GS}$  = 10 V,  $I_D$  = 80 A
- UIS Capability
- Wettable Flanks for Automatic Optical Inspection (AOI)
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

### Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

### MOSFET MAXIMUM RATINGS ( $T_J$ = 25°C, Unless otherwise noted)

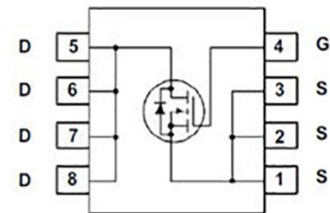
Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-to-Source Voltage	80	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Drain Current ( $T_C$ = 25°C) Continuous ( $V_{GS}$ = 10 V) (Note 1) Pulsed	80 (See Figure 4)	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	82	mJ
$P_D$	Power Dissipation Derate Above 25°C	214 1.43	W W/°C
$T_J, T_{STG}$	Operating and Storage Temperature	–55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.7	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	50	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

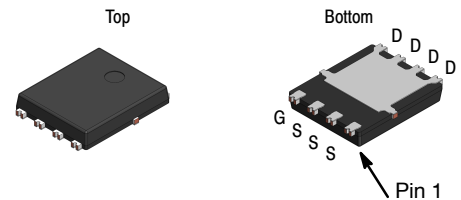
1. Current is limited by bondwire configuration.
2. Starting  $T_J$  = 25°C,  $L$  = 40 μH,  $I_{AS}$  = 64 A,  $V_{DD}$  = 80 V during inductor charging and  $V_{DD}$  = 0 V during time in avalanche.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2 oz copper.

$V_{DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
80 V	4.5 mΩ @ 10 V	80 A

### ELECTRICAL CONNECTION

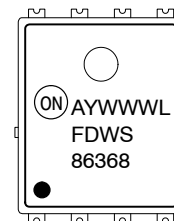


### N-Channel MOSFET



### DFNW8 CASE 507AU

### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
WW = Work Week  
WL = Assembly Lot  
FDWS = Device Code  
86368 = Device Code

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
FDWS86368-F085	DFNW8 (Power56) (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please

# FDWS86368–F085

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### OFF CHARACTERISTICS

$B_{VDSS}$	Drain-to-Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	80			V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{DS} = 80\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_J = 25^\circ\text{C}$			1	$\mu\text{A}$
		$V_{DS} = 80\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_J = 175^\circ\text{C}$ (Note 4)			1	mA
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $T_J = 25^\circ\text{C}$		3.7	4.5	m $\Omega$
		$I_D = 80\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $T_J = 175^\circ\text{C}$ (Note 4)		7.4	9.0	

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 40\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$			4350		pF
$C_{oss}$	Output Capacitance				636		pF
$C_{rss}$	Reverse Transfer Capacitance				20		pF
$R_g$	Gate Resistance	$f = 1\ \text{MHz}$			2.5		$\Omega$
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 64\ \text{V}$ , $I_D = 80\ \text{A}$		57	75	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0\ \text{V}$ to $2\ \text{V}$			8		nC
$Q_{gs}$	Gate-to-Source Gate Charge				23		nC
$Q_{gd}$	Gate-to-Drain "Miller" Charge				11		nC

### SWITCHING CHARACTERISTICS

$t_{on}$	Turn-On Time	$V_{DD} = 40\ \text{V}$ , $I_D = 80\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_{GEN} = 6\ \Omega$			60	ns
$t_{d(on)}$	Turn-On Delay			23		ns
$t_r$	Rise Time			22		ns
$t_{d(off)}$	Turn-Off Delay			32		ns
$t_f$	Fall Time			13		ns
$t_{off}$	Turn-Off Time				59	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Source-to-Drain Diode Voltage	$V_{GS} = 0\ \text{V}$ , $I_{SD} = 80\ \text{A}$ $V_{GS} = 0\ \text{V}$ , $I_{SD} = 40\ \text{A}$			1.25 1.2	V
$t_{rr}$	Reverse-Recovery Time	$I_F = 80\ \text{A}$ , $\Delta I_{SD}/\Delta t = 100\ \text{A}/\mu\text{s}$ , $V_{DD} = 64\ \text{V}$		58	75	ns
$Q_{rr}$	Reverse-Recovery Charge			49	67	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at  $T_J = 175^\circ\text{C}$ . Product is not tested to this condition in production.

## TYPICAL CHARACTERISTICS

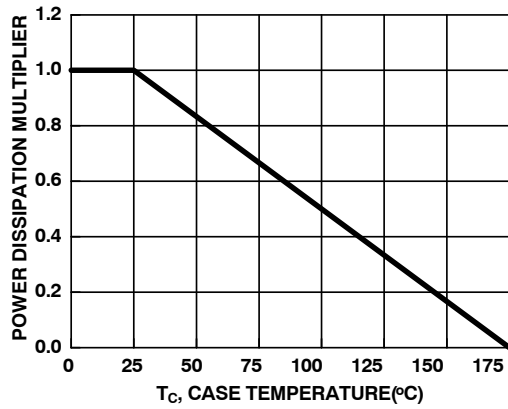


Figure 1. Normalized Power Dissipation vs. Case Temperature

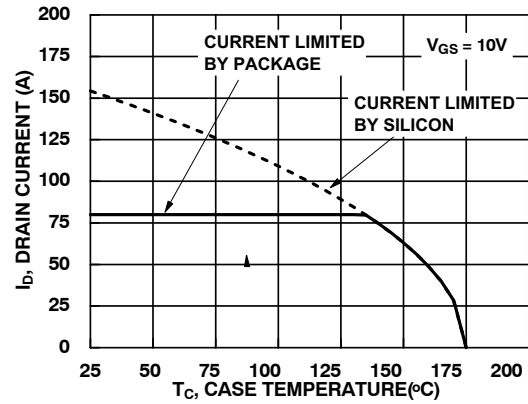


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

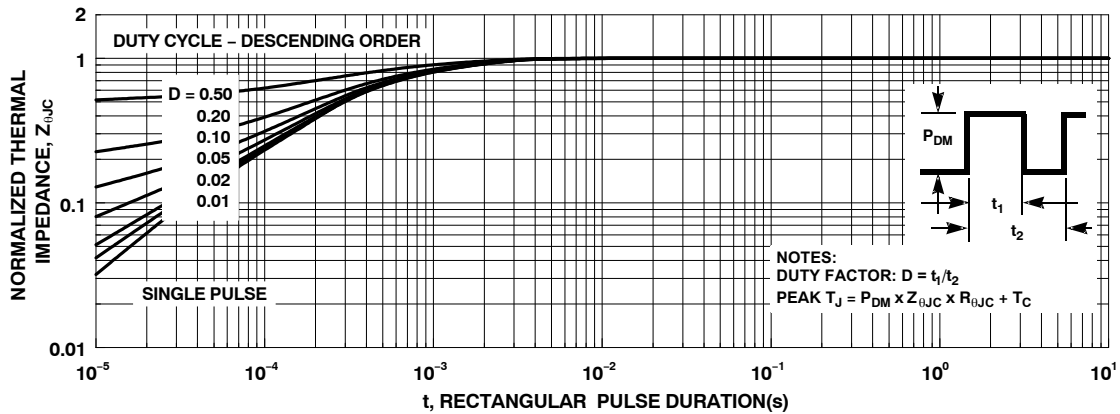


Figure 3. Normalized Maximum Transient Thermal Impedance

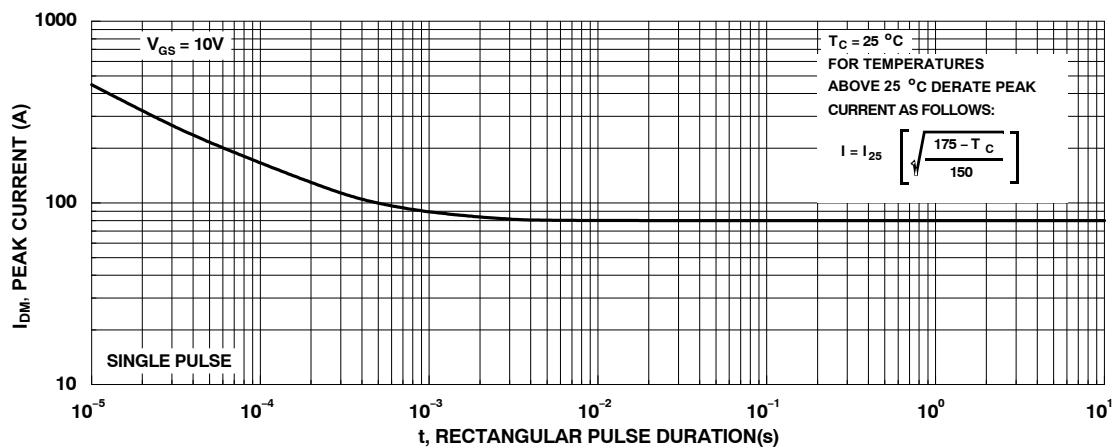


Figure 4. Peak Current Capability

## TYPICAL CHARACTERISTICS

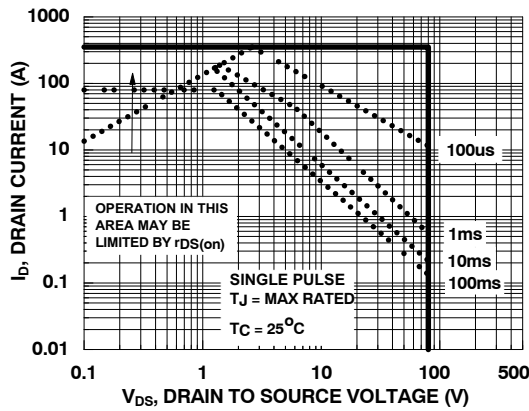
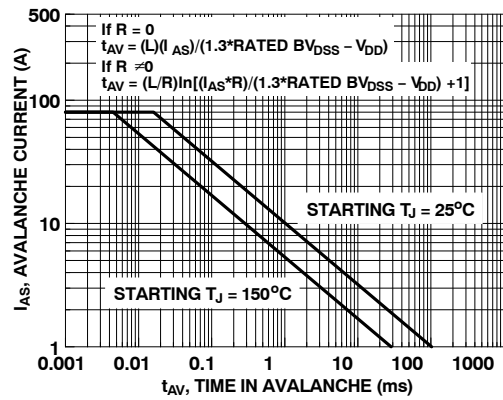


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to [onsemi](#) Application Notes [AN7514](#) and [AN7515](#)

Figure 6. Unclamped Inductive Switching Capability

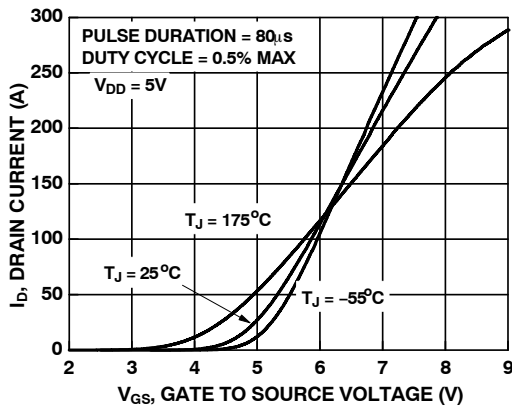


Figure 7. Transfer Characteristics

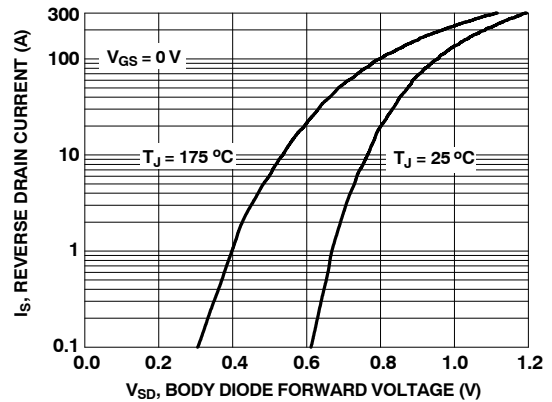


Figure 8. Forward Diode Characteristics

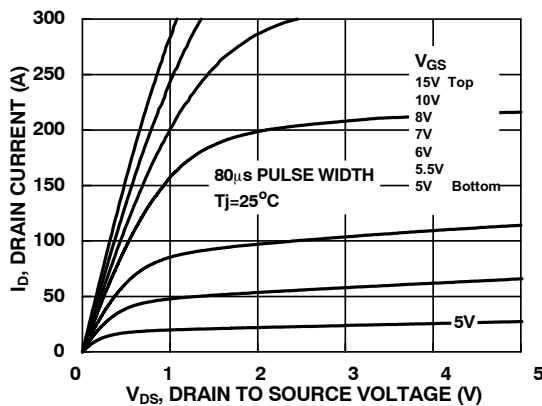


Figure 9. Saturation Characteristics

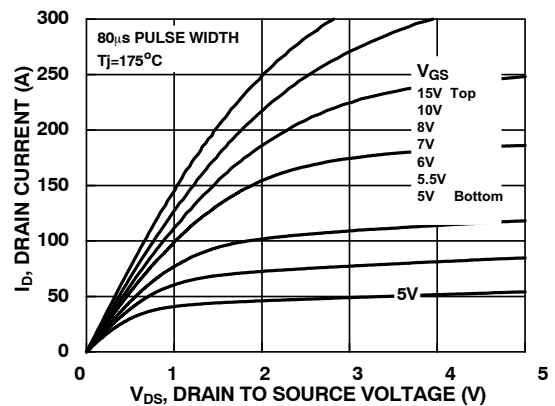


Figure 10. Saturation Characteristics

## TYPICAL CHARACTERISTICS

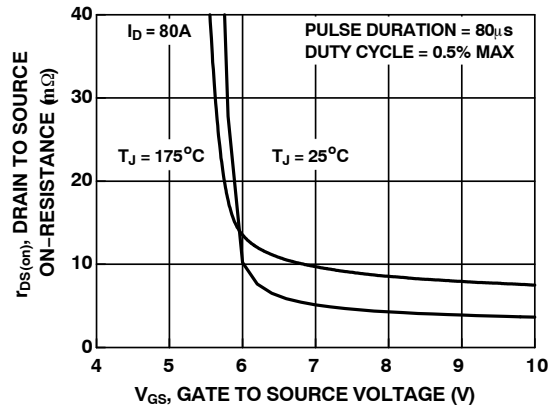
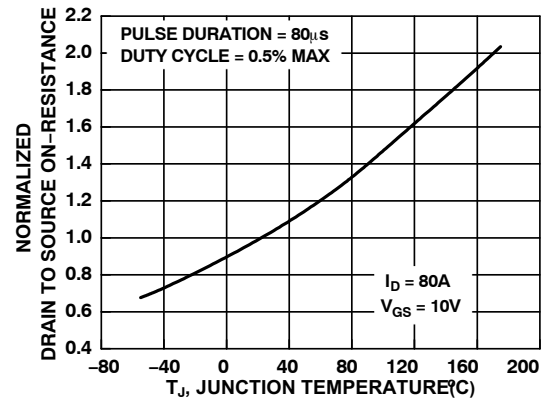
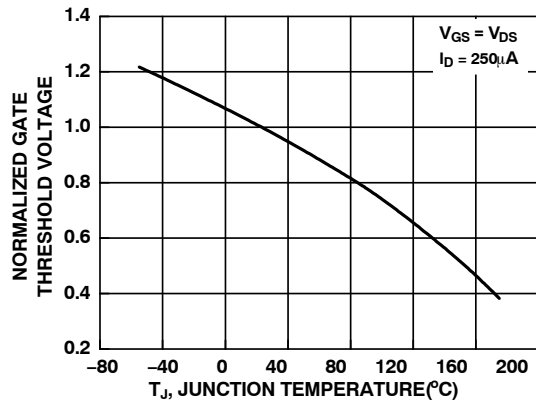
Figure 11.  $R_{DS(on)}$  vs. Gate VoltageFigure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

Figure 13. Normalized Gate Threshold Voltage vs. Temperature

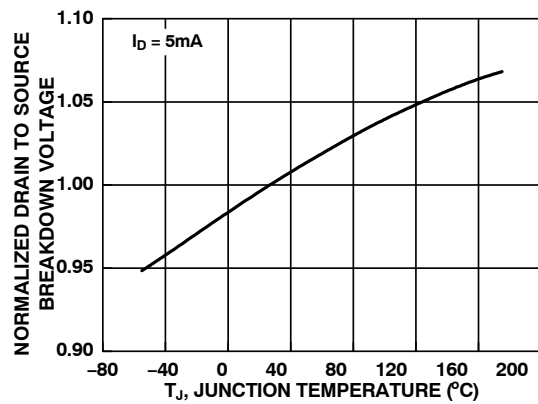


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

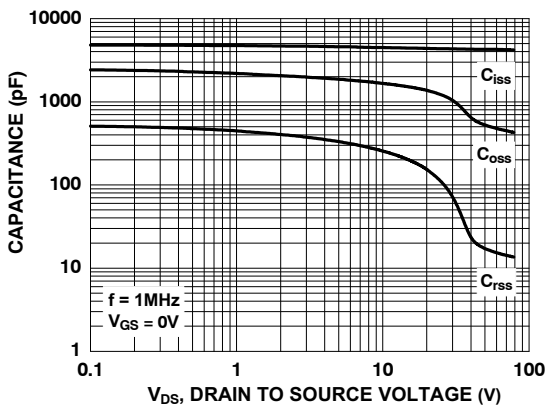


Figure 15. Capacitance vs. Drain to Source Voltage

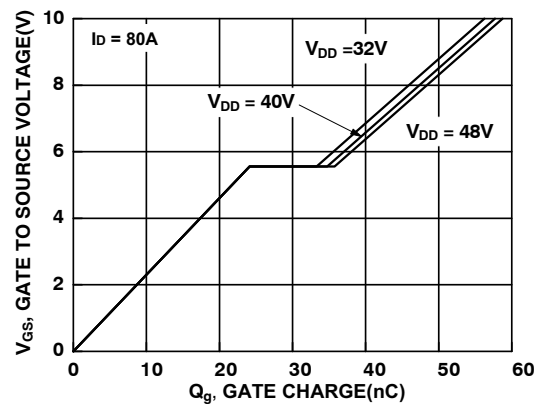


Figure 16. Single Pulse Maximum Power Dissipation



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