

STI175N4F6AG

Automotive-grade N-channel 40 V, 2.1 mΩ typ., 120 A STripFET™ F6 Power MOSFET in an I²PAK package

Datasheet - production data

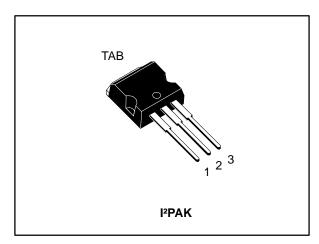
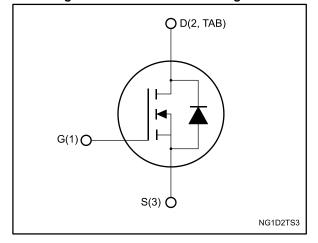


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	Ι _D	Ртот
STI175N4F6AG	40 V	2.7 mΩ	120 A	190 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications
- Power tools

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STI175N4F6AG	175N4F6	I²PAK	Tube

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STI175N4F6AG Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
Ip ⁽¹⁾	Drain current (continuous) at T _{case} = 25 °C	120	Δ.
ID ^(*)	Drain current (continuous) at T _{case} = 100 °C	120	Α
I _{DM} ⁽²⁾	Drain current (pulsed)	480	Α
Ртот	Total dissipation at T _{case} = 25 °C	190	W
T _{stg}	Storage temperature range	FF to 17F	°C
Tj	Operating junction temperature range		

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.79	°C/W
R _{thj-amb}	Thermal resistance junction-amb	62.5	C/VV

⁽¹⁾ Limited by package

 $[\]ensuremath{^{(2)}}\mbox{Pulse}$ width limited by safe operating area.

Electrical characteristics STI175N4F6AG

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	40			٧	
	Zaro goto voltago droin	$V_{GS} = 0 \text{ V}, V_{DS} = 40 \text{ V}$			1		
IDSS	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 40 V, T _{case} = 125 °C			100	μA	
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	3		4.5	V	
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 60 A		2.1	2.7	mΩ	

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	7735	ı	
Coss	Output capacitance	$V_{DS} = 20 \text{ V}, f = 1 \text{ MHz},$	-	745	ı	pF
Crss	Reverse transfer capacitance	Ves = 0 V	-	560	-	ρ.
Q_g	Total gate charge	$V_{DD} = 20 \text{ V}, I_D = 120 \text{ A},$	-	130	ı	
Q_{gs}	Gate-source charge	V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge	-	36	ı	nC
Q_{gd}	Gate-drain charge	behavior")	-	42	1	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 20 \text{ V}, I_D = 60 \text{ A R}_G = 4.7 \Omega,$	-	24	-	
tr	Rise time	V _{GS} = 10 V (see Figure 13: "Test	-	150	-	
t _{d(off)}	Turn-off delay time	circuit for resistive load switching times" and Figure 18: "Switching	-	106	-	ns
t _f	Fall time	time waveform")	-	57	-	

Table 7: Source-drain diode

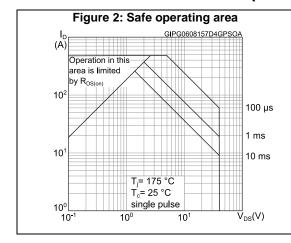
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} ⁽¹⁾	Source-drain current		ı		120	Α
I _{SDM} ⁽²⁾	Source-drain current (pulsed)		-		480	Α
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 120 A	-		1.3	V
t _{rr}	Reverse recovery time	I _{SD} = 120 A, di/dt = 100 A/μs,	ı	36		ns
Qrr	Reverse recovery charge	V _{DD} = 32 V (see Figure 15: "Test circuit for inductive load	-	40		nC
I _{RRM}	Reverse recovery current	switching and diode recovery times")	-	2.3		Α

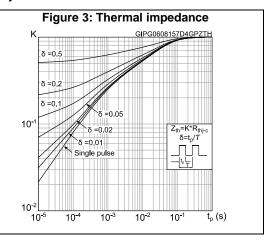
Notes:

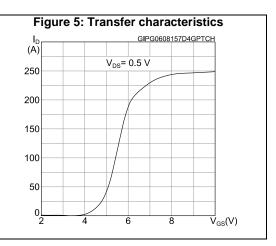
⁽¹⁾ Limited by package.

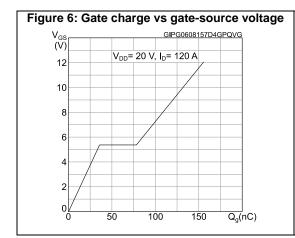
 $^{^{(2)}}$ Pulse test: pulse duration = 300 $\mu s,$ duty cycle 1.5%.

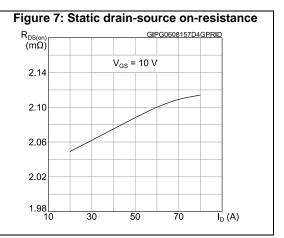
2.1 Electrical characteristics (curves)











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STI175N4F6AG Electrical characteristics

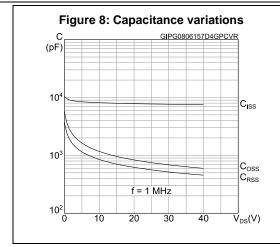


Figure 9: Normalized gate threshold voltage vs temperature

V_{GS(th)}
(norm.)

1.2

I_D= 250 μA

1.0

0.8

0.6

0.4

0.2

0

-75

-25

25

75

125

150 T_j(°C)

Figure 10: Normalized on-resistance vs temperature

R_{DS(on)} GIPG0806157D4GPRON

(norm.)

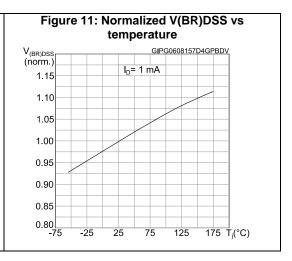
2.0

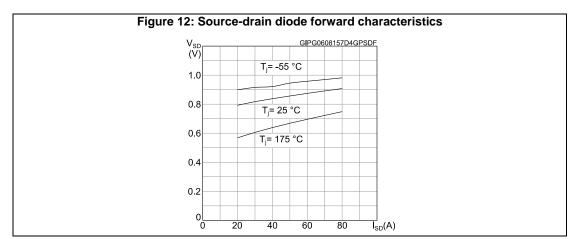
1.5

1.0

0.5

-75 -25 25 75 125 175 T_j(°C)





Test circuits STI175N4F6AG

3 Test circuits

Figure 13: Test circuit for resistive load switching times

Figure 14: Test circuit for gate charge behavior

12 V 47 KΩ 100 Ω D.U.T.

12 V 47 KΩ VGD

14 VGD

15 VGD

16 CONST 100 Ω VGD

17 VGD

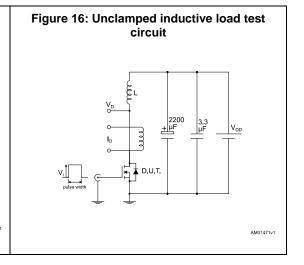
18 VGD

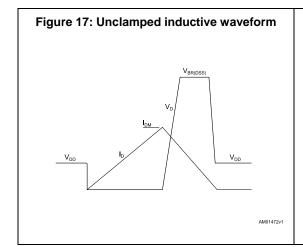
19 VGD

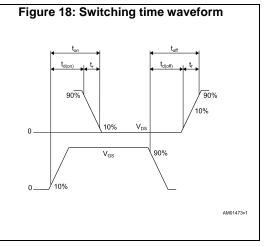
19 VGD

10 VGD

Figure 15: Test circuit for inductive load switching and diode recovery times







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STI175N4F6AG Package information

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 I²PAK package information

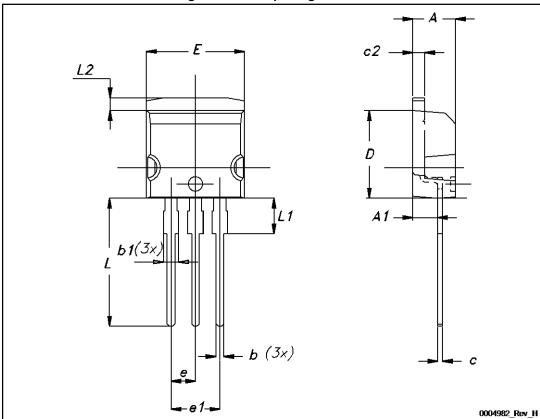


Figure 19: I²PAK package outline

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Table 8: I²PAK package mechanical data

Dim.	mm			
Dilli.	Min.	Тур.	Max.	
А	4.40	_	4.60	
A1	2.40	-	2.72	
b	0.61	_	0.88	
b1	1.14	_	1.70	
С	0.49	_	0.70	
c2	1.23	_	1.32	
D	8.95	_	9.35	
е	2.40	-	2.70	
e1	4.95	_	5.15	
Е	10	_	10.40	
L	13	_	14	
L1	3.50	_	3.93	
L2	1.27	_	1.40	

STI175N4F6AG Revision history

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Jan-2016	16 1 First release.	

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