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Energy Efficient Innovations

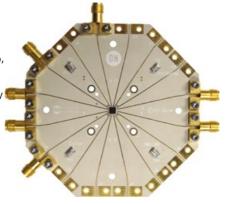
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NB7V32MMNGEVB: Differential Clock Divider Evaluation Border

The NB7V32M is a differential divide-by-2 Clock divider with asynchronous reset. The differential Clock inputs incorporate internal 50-ohm termination resistors and will accept LVPECL, CML and LVDS logic levels. The NB7V32M $\,$ produces a divide-by-2 output copy of an input Clock operating up to 10GHz with minimal jitter. The Reset pin is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the Reset allows for the synchronization of multiple NB7V32M's in a system. The 16mA differential CML output provides matching internal 50-ohm termination which guarantees 400mV output swing when externally receiver terminated with 50-ohm to VCC.



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Features and Applications

Features

- Test & Measurement, ATE
- Instrumentation, Networking

Evaluation/Development Tool Information						
Product	Status	Compliance	Short Description	Parts Used	Action	
NB7V32MMNGEVB	Active	Pb-free	Differential Clock Divider Evaluation Border	NB7V32MMNG	>> Contact Local Sales Office >> Inventory	

Technical Documents					
Туре	Document Title	Document ID/Size	Rev		
Eval Board: Manual	NB7V32MMNGEVB Manual	EVBUM2185/D - 621.0 KB	0		

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