

NTR4503N

Power MOSFET

30 V, 2.5 A, Single N-Channel, SOT-23

Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 4.5 V Rated for Low Voltage Gate Drive
- SOT-23 Surface Mount for Small Footprint (3 x 3 mm)
- These are Pb-Free Devices

Applications

- DC-DC Conversion
- Load/Power Switch for Portables
- Load/Power Switch for Computing

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V _{DSS}	30	V	
Gate-to-Source Voltage		V _{GS}	±20	V	
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	2.0	A
		T _A = 85°C		1.5	
	t ≤ 10 s	T _A = 25°C		2.5	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	0.73	W
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	1.5	A
		T _A = 85°C		1.1	
Power Dissipation (Note 2)		T _A = 25°C	P _D	0.42	W
Pulsed Drain Current	t _p = 10 μs	I _{DM}	10	A	
ESD Capability (Note 3)	C = 100 pF, RS = 1500 Ω	ESD	125	V	
Operating Junction and Storage Temperature		T _J , T _{stg}	-55 to 150	°C	
Source Current (Body Diode)		I _S	2.0	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	R _{θJA}	170	°C/W
Junction-to-Ambient - t < 10 s (Note 1)	R _{θJA}	100	
Junction-to-Ambient - Steady State (Note 2)	R _{θJA}	300	

1. Surface-mounted on FR4 board using 1 in sq pad size.
2. Surface-mounted on FR4 board using the minimum recommended pad size.
3. ESD Rating Information: HBM Class 0.

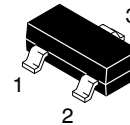
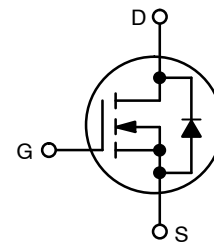


ON Semiconductor®

<http://onsemi.com>

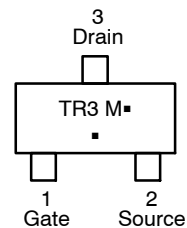
V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
30 V	85 mΩ @ 10 V	2.5 A
	105 mΩ @ 4.5 V	

N-Channel



SOT-23
CASE 318
STYLE 21

MARKING DIAGRAM/ PIN ASSIGNMENT



TR3 = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTR4503NT1G	SOT-23 (Pb-Free)	3000/Tape & Reel
NTR4503NT3G	SOT-23 (Pb-Free)	10000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTR4503N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30	36		V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V			1.0	μA
		V _{GS} = 0 V, V _{DS} = 24 V, T _J = 125°C			10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.75	3.0	V
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 2.5 A		85	110	mΩ
		V _{GS} = 4.5 V, I _D = 2.0 A		105	140	
Forward Transconductance	g _{FS}	V _{DS} = 4.5 V, I _D = 2.5 A		5.3		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 15 V		135		pF
Output Capacitance	C _{oss}			52		
Reverse Transfer Capacitance	C _{rss}			15		
Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 24 V		130	250	pF
Output Capacitance	C _{oss}			42	75	
Reverse Transfer Capacitance	C _{rss}			13	25	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 2.5 A		3.6	7.0	nC
Threshold Gate Charge	Q _{G(TH)}			0.3		
Gate-to-Source Charge	Q _{GS}			0.6		
Gate-to-Drain Charge	Q _{GD}			0.7		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 24 V, I _D = 2.5 A		1.9		nC
Threshold Gate Charge	Q _{G(TH)}			0.3		
Gate-to-Source Charge	Q _{GS}			0.6		
Gate-to-Drain Charge	Q _{GD}			0.9		

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 15 V, I _D = 1 A, R _G = 6 Ω		5.8	12	ns
Rise Time	t _r			5.8	10	
Turn-Off Delay Time	t _{d(off)}			14	25	
Fall Time	t _f			1.6	5.0	
Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 24 V, I _D = 2.5 A, R _G = 2.5 Ω		4.8		ns
Rise Time	t _r			6.7		
Turn-Off Delay Time	t _{d(off)}			13.6		
Fall Time	t _f			1.8		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2.0 A		0.85	1.2	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _S = 2.0 A, dI _S /dt = 100 A/μs		9.2		ns
Reverse Recovery Charge	Q _{RR}			4.0		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

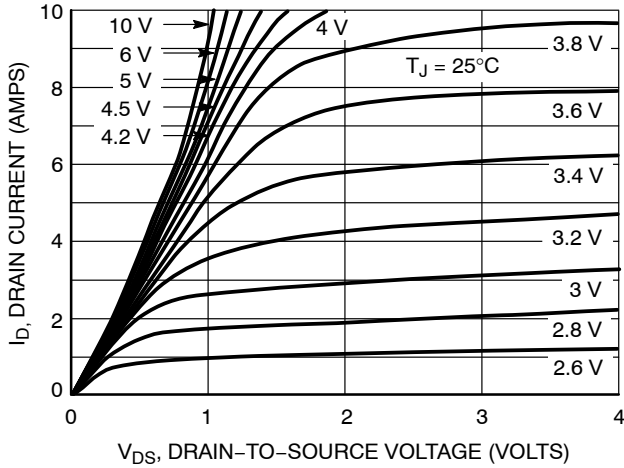


Figure 1. On-Region Characteristics

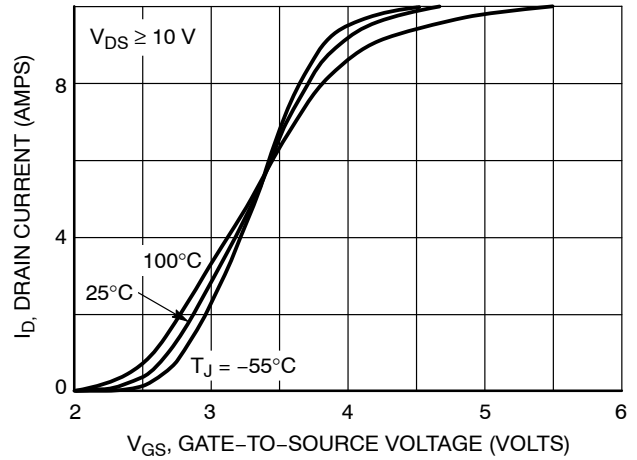


Figure 2. Transfer Characteristics

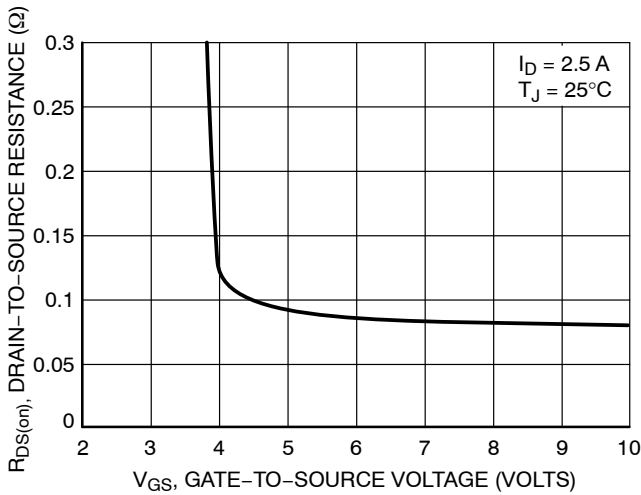


Figure 3. On-Resistance vs. Gate-to-Source Voltage

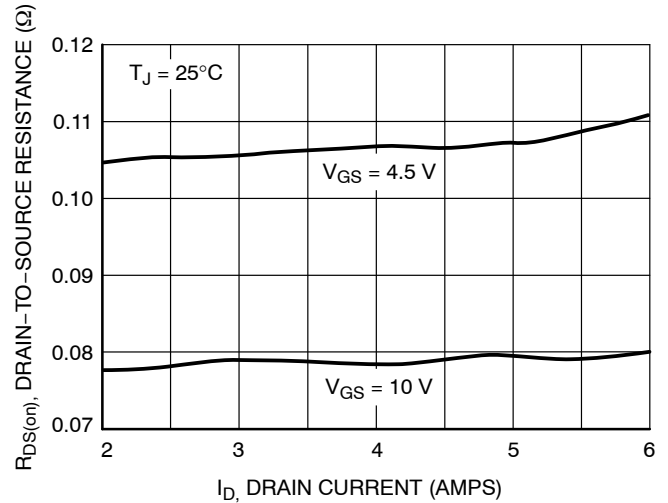


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

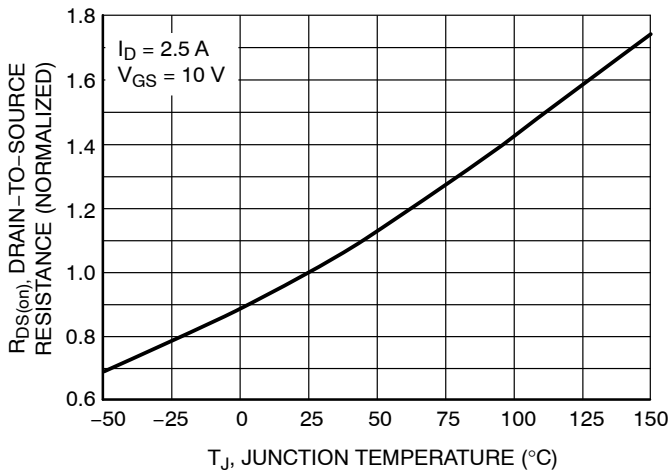


Figure 5. On-Resistance Variation with Temperature

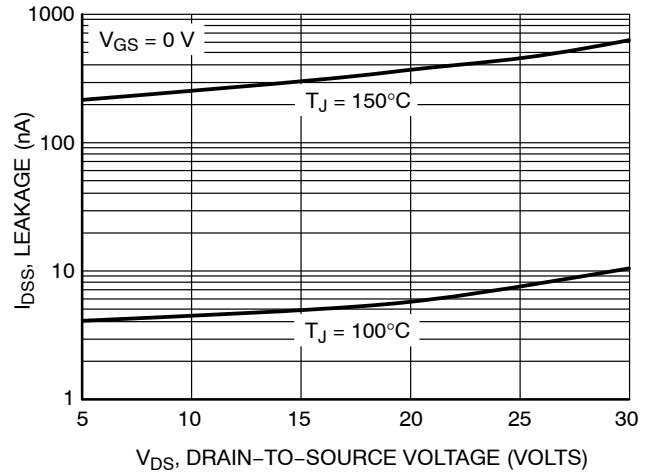
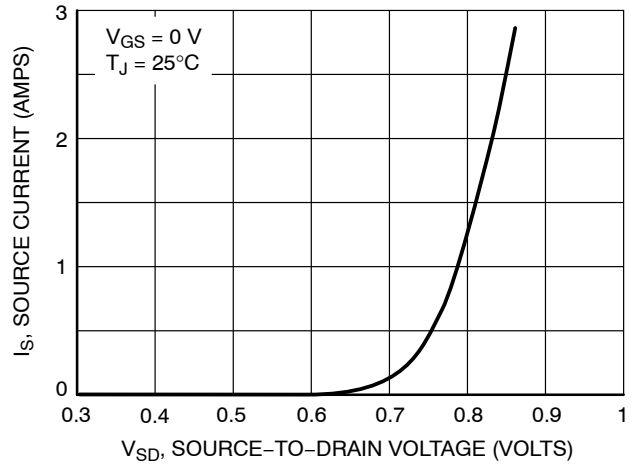
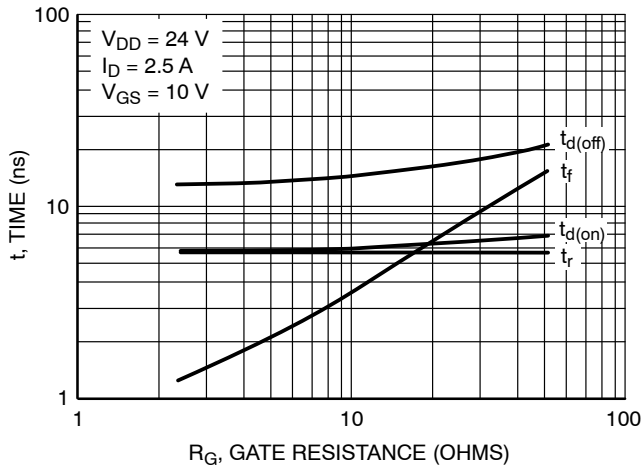
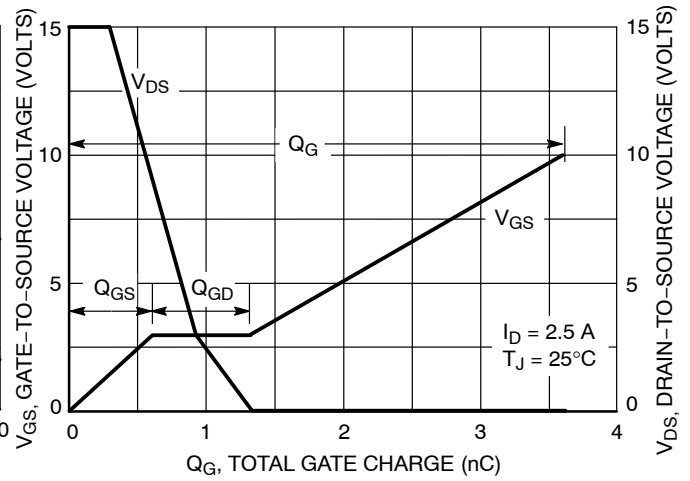
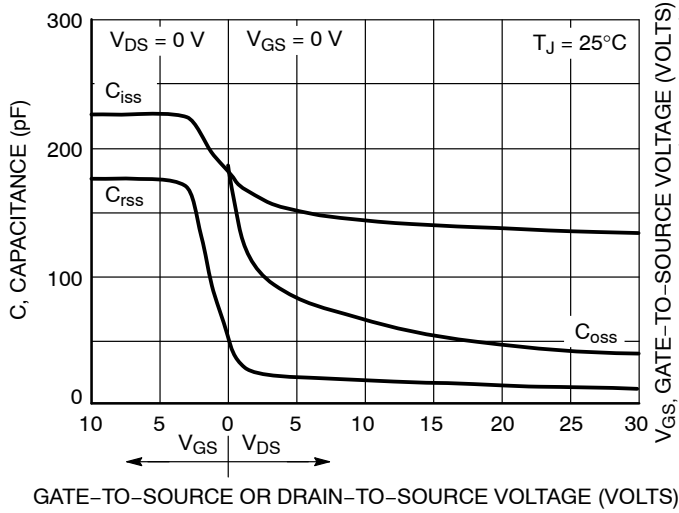


Figure 6. Drain-to-Source Leakage Current vs. Voltage

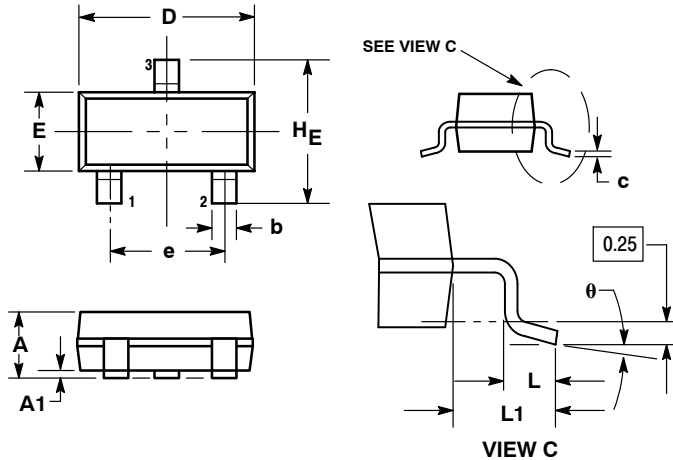
TYPICAL PERFORMANCE CURVES



NTR4503N

PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AP



NOTES:

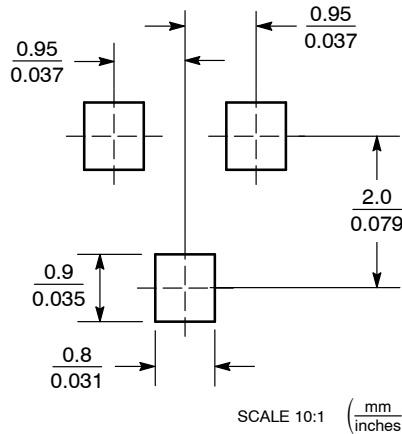
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

STYLE 21:

1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NTR4503N/D