

# 4Gb D-die DDR4 SDRAM

78FBGA with Lead-Free & Halogen-Free  
(RoHS compliant)

1.2V

## datasheet

SAMSUNG ELECTRONICS RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION AND SPECIFICATIONS WITHOUT NOTICE.

Products and specifications discussed herein are for reference purposes only. All information discussed herein is provided on an "AS IS" basis, without warranties of any kind.

This document and all information discussed herein remain the sole and exclusive property of Samsung Electronics. No license of any patent, copyright, mask work, trademark or any other intellectual property right is granted by one party to the other party under this document, by implication, estoppel or otherwise.

Samsung products are not intended for use in life support, critical care, medical, safety equipment, or similar applications where product failure could result in loss of life or personal or physical harm, or any military or defense application, or any governmental procurement to which special terms or provisions may apply.

For updates or additional information about Samsung products, contact your nearest Samsung office.

All brand names, trademarks and registered trademarks belong to their respective owners.

(C) 2014 Samsung Electronics Co., Ltd. All rights reserved.

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>	<u>Editor</u>
1.0	- First SPEC release	Feb. 2014	-	S.H.Kim
1.1	- Add x8 Product	Feb. 2014	-	S.H.Kim

**Table Of Contents**

**4Gb D-die DDR4 SDRAM**

1. Ordering Information ..... 4

2. Key Features ..... 4

3. Package pinout/Mechanical Dimension & Addressing ..... 5

    3.1 x4 Package Pinout (Top view) : 78ball FBGA Package ..... 5

    3.2 x8 Package Pinout (Top view) : 78ball FBGA Package ..... 6

    3.3 FBGA Package Dimension (x4/x8) ..... 7

4. Input/Output Functional Description ..... 8

5. DDR4 SDRAM Addressing ..... 10

6. Absolute Maximum Ratings ..... 11

7. AC & DC Operating Conditions ..... 11

8. AC & DC Input Measurement Levels ..... 12

    8.1 AC & DC Logic input levels for single-ended signals ..... 12

    8.2 V<sub>REF</sub> Tolerances ..... 12

    8.3 AC & DC Logic Input Levels for Differential Signals ..... 13

        8.3.1. Differential signals definition ..... 13

        8.3.2. Differential swing requirement for clock (CK<sub>t</sub> - CK<sub>c</sub>) ..... 13

        8.3.3. Single-ended requirements for differential signals ..... 14

        8.3.4. Address, Command and Control Overshoot and Undershoot specifications ..... 15

        8.3.5. Clock Overshoot and Undershoot Specifications ..... 15

        8.3.6. Data, Strobe and Mask Overshoot and Undershoot Specifications ..... 16

    8.4 Slew rate definitions for Differential Input Signals (CK) ..... 17

    8.5 Differential Input Cross Point Voltage ..... 18

    8.6 CMOS rail to rail Input Levels ..... 19

        8.6.1. CMOS rail to rail Input Levels for RESET<sub>n</sub> ..... 19

    8.7 AC and DC Logic Input Levels for DQS Signals ..... 20

        8.7.1. Differential signal definition ..... 20

        8.7.2. Differential swing requirements for DQS (DQS<sub>t</sub> - DQS<sub>c</sub>) ..... 20

        8.7.3. Peak voltage calculation method ..... 20

        8.7.4. Differential Input Cross Point Voltage ..... 21

        8.7.5. Differential Input Slew Rate Definition ..... 21

9. AC and DC output Measurement levels ..... 23

    9.1 Output Driver DC Electrical Characteristics ..... 23

        9.1.1. Alert<sub>n</sub> output Drive Characteristic ..... 25

        9.1.2. Output Driver Characteristic of Connectivity Test ( CT ) Mode ..... 25

    9.2 Single-ended AC & DC Output Levels ..... 26

    9.3 Differential AC & DC Output Levels ..... 26

    9.4 Single-ended Output Slew Rate ..... 27

    9.5 Differential Output Slew Rate ..... 28

    9.6 Single-ended AC & DC Output Levels of Connectivity Test Mode ..... 29

    9.7 Test Load for Connectivity Test Mode Timing ..... 29

10. Speed Bin ..... 30

    10.1 Speed Bin Table Note ..... 33

11. IDD and IDDQ Specification Parameters and Test conditions ..... 34

    11.1 IDD, IPP and IDDQ Measurement Conditions ..... 34

    11.2 4Gb DDR4 SDRAM D-die IDD Specification Table ..... 49

12. Input/Output Capacitance ..... 52

13. Electrical Characteristics & AC Timing ..... 54

    13.1 Reference Load for AC Timing and Output Slew Rate ..... 54

    13.2 tREFI ..... 54

    13.3 Timing Parameters by Speed Grade ..... 55

    13.4 The DQ input receiver compliance mask for voltage and timing (see figure) ..... 61

    13.5 DDR4 Function Matrix ..... 66



## 1. Ordering Information

[ Table 1 ] Samsung 4Gb DDR4 D-die ordering information table

Organization	DDR4-2133 (15-15-15)	DDR4-2400 (17-17-17) <sup>2</sup>	Package
1Gx4	K4A4G045WD-BCPB	K4A4G045WD-BCRC	78 FBGA
512Mx8	K4A4G085WD-BCPB	K4A4G085WD-BCRC	78 FBGA

**NOTE :**

1. Speed bin is in order of CL-tRCD-tRP.
2. Backward compatible to DDR4-2133(15-15-15)

## 2. Key Features

[ Table 2 ] 4Gb DDR4 D-die Speed bins

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	
tCK(min)	1.25	1.071	0.938	0.833	ns
CAS Latency	11	13	15	17	nCK
tRCD(min)	13.75	13.92	14.06	14.16	ns
tRP(min)	13.75	13.92	14.06	14.16	ns
tRAS(min)	35	34	33	32	ns
tRC(min)	48.75	47.92	47.06	46.16	ns

- JEDEC standard 1.2V (1.14V~1.26V)
- $V_{DDQ} = 1.2V$  (1.14V~1.26V)
- 800 MHz  $f_{CK}$  for 1600Mb/sec/pin, 933 MHz  $f_{CK}$  for 1866Mb/sec/pin, 1067MHz  $f_{CK}$  for 2133Mb/sec/pin, 1200MHz  $f_{CK}$  for 2400Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency(posted CAS): 10,11,12,13,14,15,16,17,18
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600) , 10,12 (DDR4-1866) , 11,14 (DDR4-2133) and 12,16 (DDR4-2400)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm  $\pm$  1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than  $T_{CASE}$  85°C, 3.9us at 85°C <  $T_{CASE}$   $\leq$  95 °C
- Asynchronous Reset
- Package : 78 balls FBGA - x4/x8
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-free
- CRC(Cyclic Redundancy Check) for Read/Write data security
- Command address parity check
- DBI(Data Bus Inversion)
- Gear down mode
- POD (Pseudo Open Drain) interface for data input/output
- Internal VREF for data inputs
- External VPP for DRAM Activating Power

The 4Gb DDR4 SDRAM D-die is organized as a 64Mbit x 4 I/Os x 16banks or 32Mbit x8 I/Os x 16banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 2400Mb/sec/pin (DDR4-2400) for general applications.

The chip is designed to comply with the following key DDR4 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset .

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and  $\overline{CK}$  falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and  $\overline{DQS}$ ) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a  $\overline{RAS}/\overline{CAS}$  multiplexing style. The DDR4 device operates with a single 1.2V (1.14V~1.26V) power supply and 1.2V (1.14V~1.26V) . The 4Gb DDR4 D-die device is available in 78ball FBGAs(x4/x8).

**NOTE :** 1. This data sheet is an abstract of full DDR4 specification and does not cover the common features which are described in "DDR4 SDRAM Device Operation & Timing Diagram".

2. The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

### 3. Package pinout/Mechanical Dimension & Addressing

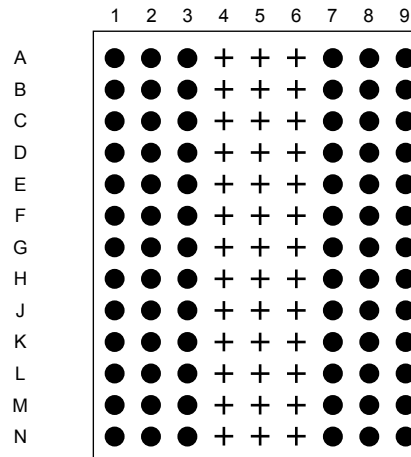
#### 3.1 x4 Package Pinout (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	NC				NC	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	NC	DQ2				DQ3	NC	VSSQ	D
E	VSS	VDDQ	NC				NC	VDDQ	VSS	E
F	VDD	NC	ODT				CK_t	CK_c	VDD	F
G	VSS	NC	CKE				CS_n	NC	NC	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N

#### Ball Locations (x4)

- Populated ball
- + Ball not populated

Top view  
(See the balls through the package)



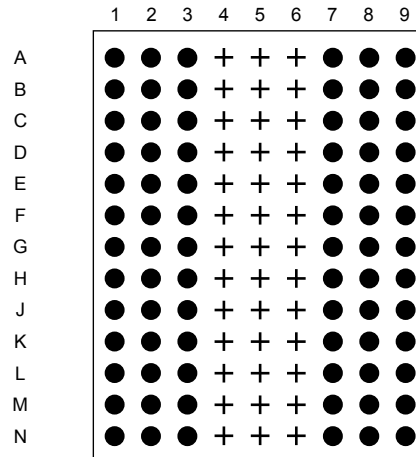
3.2 x8 Package Pinout (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n, DBI_n, TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	NC	ODT				CK_t	CK_c	VDD	F
G	VSS	NC	CKE				CS_n	NC	NC	G
H	VDD	WE_n A14	ACT_n				CAS_n	RAS_n	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N

Ball Locations (x8)

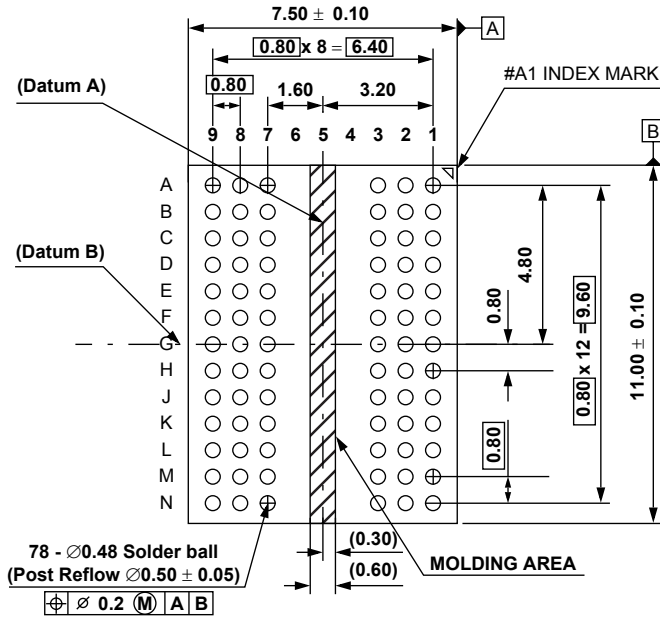
- Populated ball
- + Ball not populated

Top view  
(See the balls through the package)

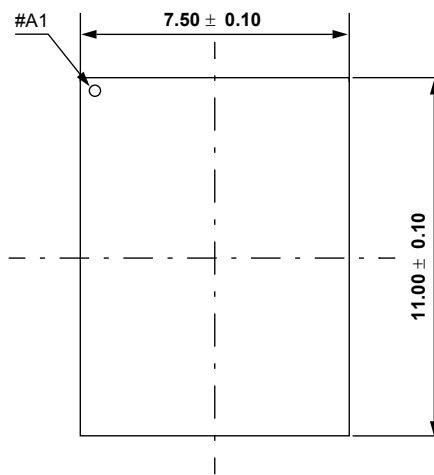


3.3 FBGA Package Dimension (x4/x8)

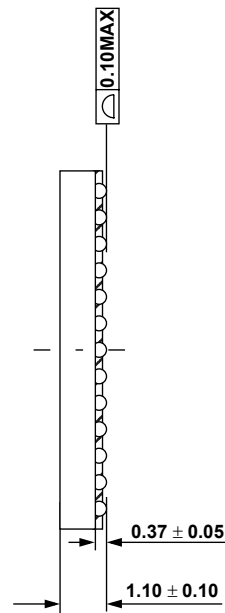
Units : Millimeters



BOTTOM VIEW



TOP VIEW



## 4. Input/Output Functional Description

[ Table 3 ] Input/Output function description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQS_u_t, DQS_u_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n, CAS_n/A15 and WE_n/A14 will be considered as Row Address A15, A14
RAS_n, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A15, A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/ BC_n, RAS_n, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V <sub>DD</sub> .
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c,	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t paired with differential signal DQS_c to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.



Symbol	Type	Function
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/ TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/ TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n,CAS_n/A15,WE_n/ A14,BG0-BG1,BA0-BA1,A15-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal . If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V ( 2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
<b>NOTE</b> : Input only pins (BG0-BG1,BA0-BA1, A0-A15, ACT_n, RAS_n, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.		

## 5. DDR4 SDRAM Addressing

## 2 Gb Addressing Table

Configuration		512 Mb x4	256 Mb x8	128 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A14	A0~A13	A0~A13
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

## 4 Gb Addressing Table

Configuration		1 Gb x4	512 Mb x8	256 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A15	A0~A14	A0~A14
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

## 8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A16	A0~A15	A0~A15
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

## 16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A17	A0~A16	A0~A16
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

**NOTE 1 :** Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.

Page size is per bank, calculated as follows:  $\text{page size} = 2^{\text{COLBITS}} \times \text{ORG} \times 8$   
 where, COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

## 6. Absolute Maximum Ratings

[ Table 4 ] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T <sub>STG</sub>	Storage Temperature	-55 to +100	°C	1,2

**NOTE :**

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
- VPP must be equal or greater than VDD/VDDQ at all times.
- Overshoot area above 1.5 V is specified in section 8.3.4 , 8.3.5 and 8.3.6.

## 7. AC & DC Operating Conditions

[ Table 5 ] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

**NOTE :**

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- DC bandwidth is limited to 20MHz.

## 8. AC & DC Input Measurement Levels

### 8.1 AC & DC Logic input levels for single-ended signals

[ Table 6 ] Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		Unit	NOTE
		Min.	Max.		
$V_{IH.CA}(DC75)$	DC input logic high	$V_{REFCA} + 0.075$	$V_{DD}$	V	
$V_{IL.CA}(DC75)$	DC input logic low	$V_{SS}$	$V_{REFCA} - 0.075$	V	
$V_{IH.CA}(AC100)$	AC input logic high	$V_{REF} + 0.1$	Note 2	V	1
$V_{IL.CA}(AC100)$	AC input logic low	Note 2	$V_{REF} - 0.1$	V	1
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	2,3

**NOTE :**

1. See "Overshoot and Undershoot Specifications".
2. The AC peak noise on  $V_{REFCA}$  may not allow  $V_{REFCA}$  to deviate from  $V_{REFCA}(DC)$  by more than  $\pm 1\% V_{DD}$  (for reference : approx.  $\pm 12mV$ )
3. For reference : approx.  $V_{DD}/2 \pm 12mV$

### 8.2 $V_{REF}$ Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages  $V_{REFCA}$  is illustrated in Figure 1. It shows a valid reference voltage  $V_{REF}(t)$  as a function of time. ( $V_{REF}$  stands for  $V_{REFCA}$  and  $V_{REFDQ}$  likewise).

$V_{REF}(DC)$  is the linear average of  $V_{REF}(t)$  over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 6 on page 12. Furthermore  $V_{REF}(t)$  may temporarily deviate from  $V_{REF}(DC)$  by no more than  $\pm 1\% V_{DD}$ .

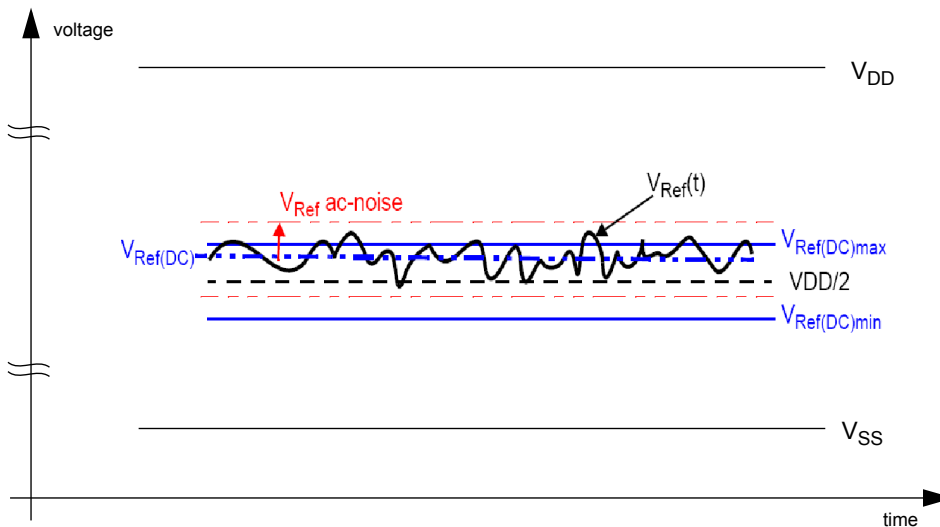


Figure 1. Illustration of  $V_{REF}(DC)$  tolerance and  $V_{REF}$  ac-noise limits

The voltage levels for setup and hold time measurements  $V_{IH}(AC)$ ,  $V_{IH}(DC)$ ,  $V_{IL}(AC)$  and  $V_{IL}(DC)$  are dependent on  $V_{REF}$ .

" $V_{REF}$ " shall be understood as  $V_{REF}(DC)$ , as defined in Figure 1.

This clarifies, that dc-variations of  $V_{REF}$  affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for  $V_{REF}(DC)$  deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with  $V_{REF}$  ac-noise. Timing and voltage effects due to ac-noise on  $V_{REF}$  up to the specified limit ( $\pm 1\%$  of  $V_{DD}$ ) are included in DRAM timings and their associated deratings.

### 8.3 AC & DC Logic Input Levels for Differential Signals

#### 8.3.1 Differential signals definition

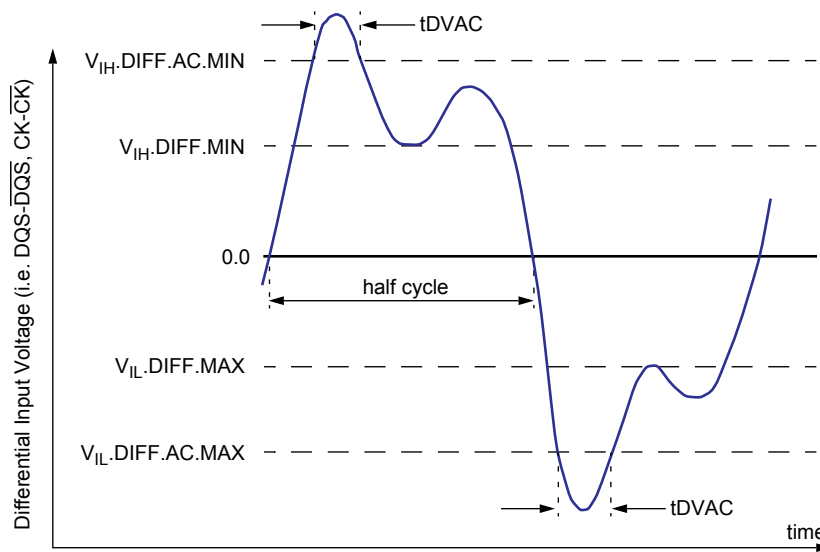


Figure 2. Definition of differential ac-swing and "time above ac level" tDVAC

**NOTE :**

1. Differential signal rising edge from V<sub>IL,DIFF.MAX</sub> to V<sub>IH,DIFF.MIN</sub> must be monotonic slope.
2. Differential signal falling edge from V<sub>IH,DIFF.MIN</sub> to V<sub>IL,DIFF.MAX</sub> must be monotonic slope.

#### 8.3.2 Differential swing requirement for clock (CK<sub>t</sub> - CK<sub>c</sub>)

[ Table 7 ] Differential AC & DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400		unit	NOTE
		min	max	min	max		
V <sub>IHdiff</sub>	differential input high	+0.150	NOTE 3	TBD	NOTE 3	V	1
V <sub>ILdiff</sub>	differential input low	NOTE 3	-0.150	NOTE 3	TBD	V	1
V <sub>IHdiff(AC)</sub>	differential input high ac	2 x (V <sub>IH(AC)</sub> - V <sub>REF</sub> )	NOTE 3	2 x (V <sub>IH(AC)</sub> - V <sub>REF</sub> )	NOTE 3	V	2
V <sub>ILdiff(AC)</sub>	differential input low ac	NOTE 3	2 x (V <sub>IL(AC)</sub> - V <sub>REF</sub> )	NOTE 3	2 x (V <sub>IL(AC)</sub> - V <sub>REF</sub> )	V	2

**NOTE:**

1. Used to define a differential signal slew-rate.
2. for CK<sub>t</sub> - CK<sub>c</sub> use V<sub>IHCA</sub>/V<sub>ILCA(AC)</sub> of ADD/CMD and V<sub>REFCA</sub>;
3. These values are not defined; however, the differential signals CK<sub>t</sub> - CK<sub>c</sub>, need to be within the respective limits (V<sub>IHCA</sub>(DC) max, V<sub>ILCA</sub>(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

[ Table 8 ] Allowed time before ringback (tDVAC) for CK<sub>t</sub> - CK<sub>c</sub>

Slew Rate [V/ns]	tDVAC [ps] @  V <sub>IH/Ldiff(AC)</sub>   = 200mV		tDVAC [ps] @  V <sub>IH/Ldiff(AC)</sub>   = TBDmV	
	min	max	min	max
> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
< 1.0	80	-	TBD	-

### 8.3.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK<sub>t</sub>, CK<sub>c</sub>) has also to comply with certain requirements for single-ended signals.

CK<sub>t</sub> and CK<sub>c</sub> have to approximately reach V<sub>SEH</sub>min / V<sub>SEL</sub>max [approximately equal to the ac-levels { V<sub>IH,CA</sub>(AC) / V<sub>IL,CA</sub>(AC)} for ADD/CMD signals] in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g. if Different value than V<sub>IH,CA</sub>(AC100)/V<sub>IL,CA</sub>(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK<sub>t</sub> and CK<sub>c</sub>.

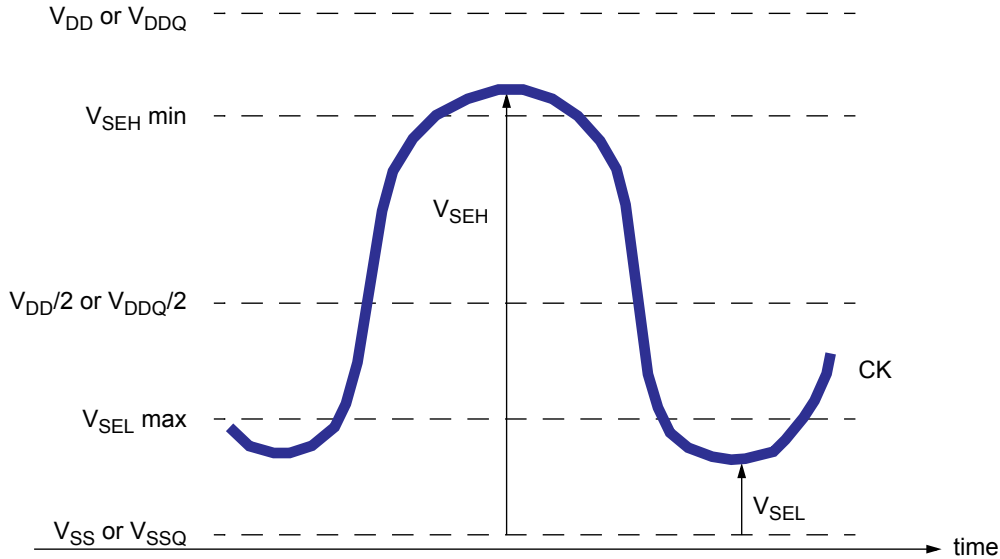


Figure 3. Single-ended requirement for differential signals

Note that while ADD/CMD signal requirements are with respect to V<sub>REFCA</sub>, the single-ended components of differential signals have a requirement with respect to V<sub>DD</sub>/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V<sub>SEL</sub>max, V<sub>SEH</sub>min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[ Table 9 ] Single-ended levels for CK<sub>t</sub>, CK<sub>c</sub>

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	NOTE
		Min	Max	Min	Max		
V <sub>SEH</sub>	Single-ended high-level for CK <sub>t</sub> , CK <sub>c</sub>	(V <sub>DD</sub> /2)+0.100	NOTE3	TBD	NOTE3	V	1, 2
V <sub>SEL</sub>	Single-ended low-level for CK <sub>t</sub> , CK <sub>c</sub>	NOTE3	(V <sub>DD</sub> /2)-0.100	NOTE3	TBD	V	1, 2

- NOTE :
1. For CK<sub>t</sub> - CK<sub>c</sub> use V<sub>IH,CA</sub>/V<sub>IL,CA</sub>(AC) of ADD/CMD;
  2. V<sub>IH</sub>(AC)/V<sub>IL</sub>(AC) for ADD/CMD is based on V<sub>REFCA</sub>;
  3. These values are not defined, however the single-ended signals CK<sub>t</sub> - CK<sub>c</sub> need to be within the respective limits (V<sub>IH,CA</sub>(DC) max, V<sub>IL,CA</sub>(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

8.3.4 Address, Command and Control Overshoot and Undershoot specifications

[ Table 10 ] AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Specification				Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06	0.06	0.06	0.06	V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	0.24	0.24	0.24	0.24	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	V-ns
Maximum overshoot area per 1tCK Above Absolute Max	0.0083	0.0071	0.0062	0.0055	V-ns
Maximum overshoot area per 1tCK Between Absolute Max and VDD Max	0.2550	0.2185	0.1914	0.1699	V-ns
Maximum undershoot area per 1tCK Below VSS	0.2644	0.2265	0.1984	0.1762	V-ns
(A0-A13,BG0-BG1,BA0-BA1,ACT_n,RAS_n,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)					

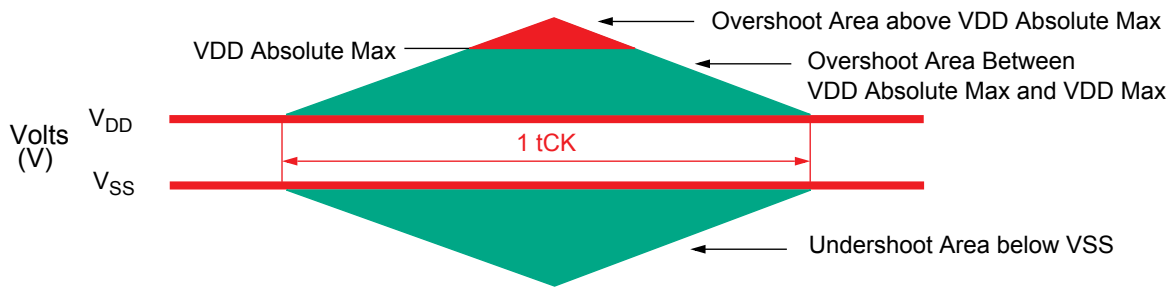


Figure 4. Address, Command and Control Overshoot and Undershoot Definition

8.3.5 Clock Overshoot and Undershoot Specifications

[ Table 11 ] AC overshoot/undershoot specification for Clock

Parameter	Specification				Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06	0.06	0.06	0.06	V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	0.24	0.24	0.24	0.24	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	V
Maximum overshoot area per 1UI Above Absolute Max	0.0038	0.0032	0.0028	0.0025	V-ns
Maximum overshoot area per 1UI Between Absolute Max and VDD Max	0.1125	0.0964	0.0844	0.0750	V-ns
Maximum undershoot area per 1UI Below VSS	0.1144	0.0980	0.0858	0.0762	V-ns
(CK_t, CK_c)					

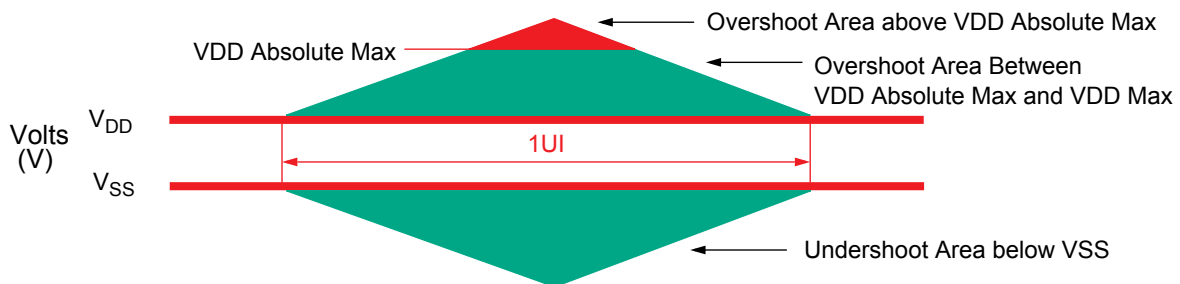


Figure 5. Clock Overshoot and Undershoot Definition

8.3.6 Data, Strobe and Mask Overshoot and Undershoot Specifications

[ Table 12 ] AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Specification				Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	
Maximum peak amplitude above Max absolute level of Vin, Vout	0.16	0.16	0.16	0.16	V
Overshoot area Between Max Absolute level of Vin, Vout and VDDQ Max	0.24	0.24	0.24	0.24	V
Undershoot area Between Min absolute level of Vin, Vout and VSSQ	0.30	0.30	0.30	0.30	V
Maximum peak amplitude below Min absolute level of Vin, Vout	0.10	0.10	0.10	0.10	V
Maximum overshoot area per 1UI Above Max absolute level of Vin, Vout	0.0150	0.0129	0.0113	0.0100	V-ns
Maximum overshoot area per 1UI Between Max absolute level of Vin,Vout and VDDQ Max	0.1050	0.0900	0.0788	0.0700	V-ns
Maximum undershoot area per 1UI Between Min absolute level of Vin,Vout and VSSQ	0.1050	0.0900	0.0788	0.0700	V-ns
Maximum undershoot area per 1UI Below Min absolute level of Vin,Vout	0.0150	0.0129	0.0113	0.0100	V-ns

(DQ, DQS\_t, DQS\_c, DM\_n, DBI\_n, TDQS\_t, TDQS\_c)

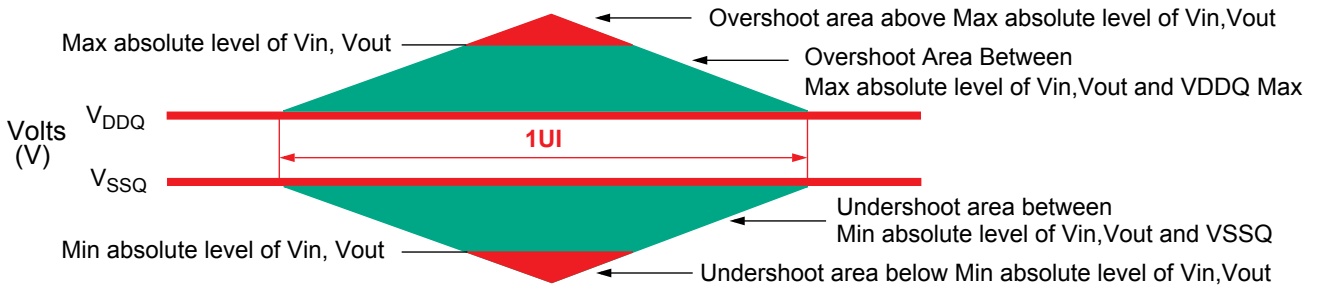


Figure 6. Data, Strobe and Mask Overshoot and Undershoot Definition



### 8.4 Slew rate definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK<sub>t</sub>, CK<sub>c</sub>) are defined and measured as shown in Table 13 and Figure 7.

[ Table 13 ] Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge(CK <sub>t</sub> - CK <sub>c</sub> )	V <sub>ILdiffmax</sub>	V <sub>IHdiffmin</sub>	$[ V_{IHdiffmin} - V_{ILdiffmax} ] / \Delta TR_{diff}$
Differential input slew rate for falling edge(CK <sub>t</sub> - CK <sub>c</sub> )	V <sub>IHdiffmin</sub>	V <sub>ILdiffmax</sub>	$[ V_{IHdiffmin} - V_{ILdiffmax} ] / \Delta TF_{diff}$

**NOTE :**  
The differential signal (i.e. CK -  $\overline{CK}$  and DQS -  $\overline{DQS}$ ) must be linear between these thresholds.

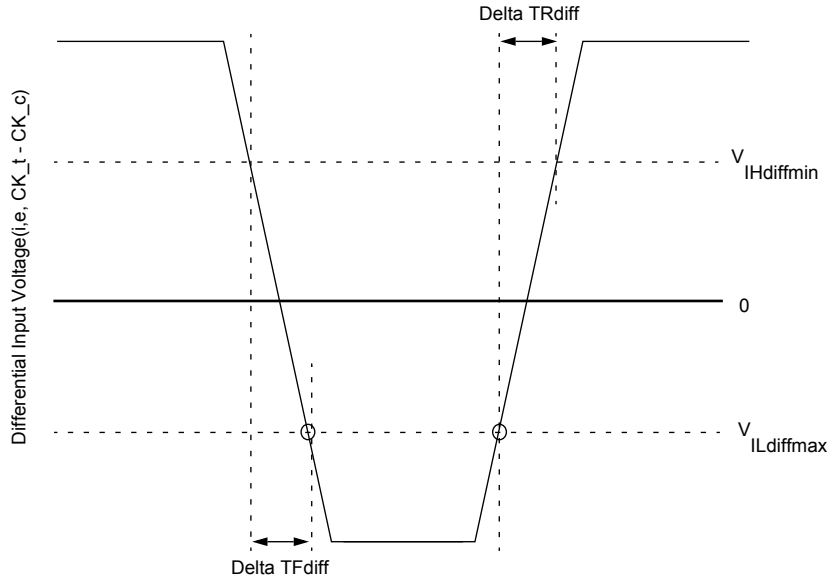


Figure 7. Differential Input Slew Rate definition for CK,  $\overline{CK}$

### 8.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK<sub>t</sub>, CK<sub>c</sub>) must meet the requirements in Table 15. The differential input cross point voltage V<sub>ix</sub> is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

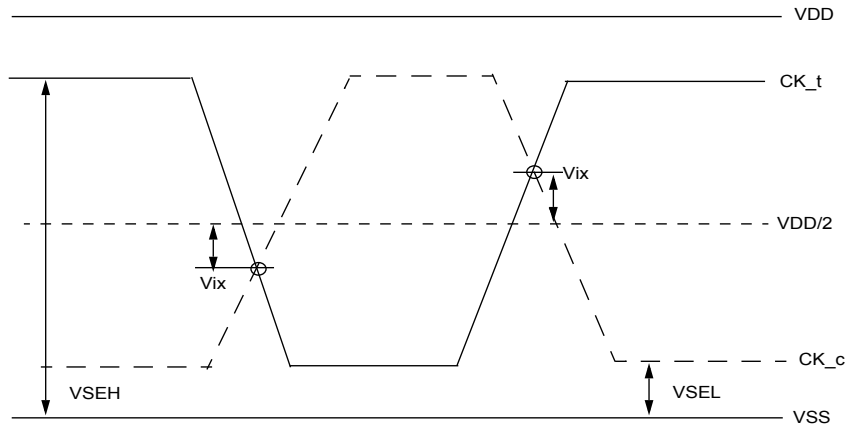


Figure 8. Vix Definition (CK)

[ Table 14 ] Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133			
		min		max	
-	Area of VSEH, VSEL	$VSEL \leq VDD/2 - 145mV$	$VDD/2 - 145mV \leq VSEL \leq VDD/2 - 100mV$	$VDD/2 + 100mV \leq VSEL \leq VDD/2 + 145mV$	$VDD/2 + 145mV \leq VSEL$
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK <sub>t</sub> , CK <sub>c</sub>	-120mV	$-(VDD/2 - VSEL) + 25mV$	$(VSEH - VDD/2) - 25mV$	120mV

Symbol	Parameter	DDR4-2400			
		min		max	
-	Area of VSEH, VSEL	TBD	TBD	TBD	TBD
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK <sub>t</sub> , CK <sub>c</sub>	TBD	TBD	TBD	TBD

## 8.6 CMOS rail to rail Input Levels

### 8.6.1 CMOS rail to rail Input Levels for RESET\_n

[ Table 15 ] CMOS rail to rail Input Levels for RESET\_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

- NOTE :**
1. After RESET\_n is registered LOW, RESET\_n level shall be maintained below VIL(DC)\_RESET during tPW\_RESET, otherwise, SDRAM may not be reset.
  2. Once RESET\_n is registered HIGH, RESET\_n level must be maintained above VIH(DC)\_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET\_n signal LOW.
  3. RESET is destructive to data contents.
  4. No slope reversal (ringback) requirement during its level transition from Low to High.
  5. This definition is applied only "Reset Procedure at Power Stable".
  6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
  7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

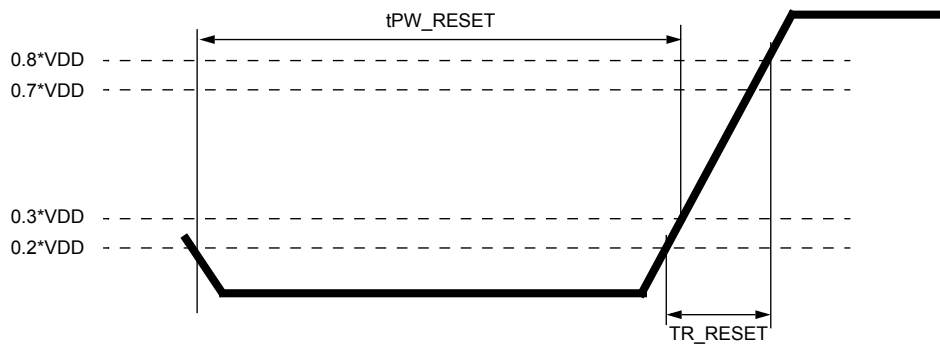


Figure 9. RESET\_n Input Slew Rate Definition

## 8.7 AC and DC Logic Input Levels for DQS Signals

### 8.7.1 Differential signal definition

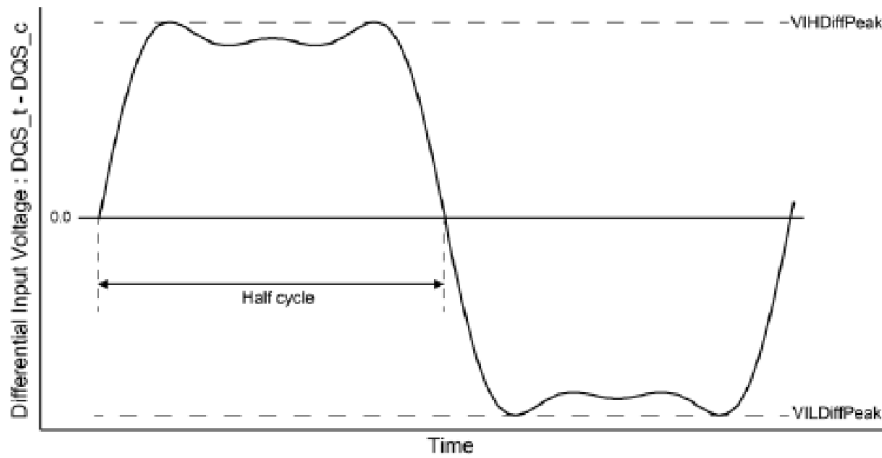


Figure 10. Definition of differential DQS Signal AC-swing Level

### 8.7.2 Differential swing requirements for DQS (DQS\_t - DQS\_c)

[ Table 16 ] Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-1600, 1866, 2133		DDR4-2400		Unit	Note
		Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	186	Note2	TBD	TBD	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-186	TBD	TBD	mV	1

- NOTE :**
- Used to define a differential signal slew-rate.
  - These values are not defined; however, the differential signals DQS\_t - DQS\_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

### 8.7.3 Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

$$\text{VIH.DIFF.Peak Voltage} = \text{Max}(f(t))$$

$$\text{VIL.DIFF.Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = \text{VDQS}_t - \text{VDQS}_c$$

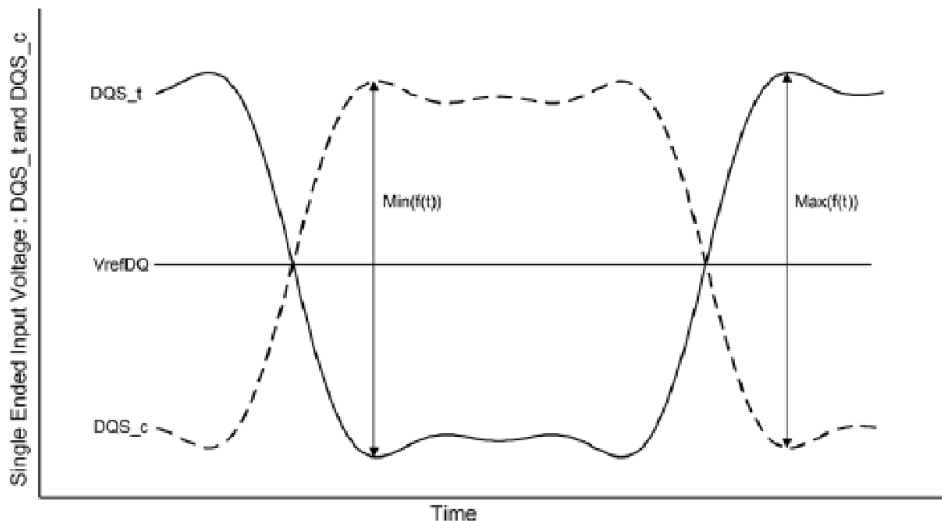
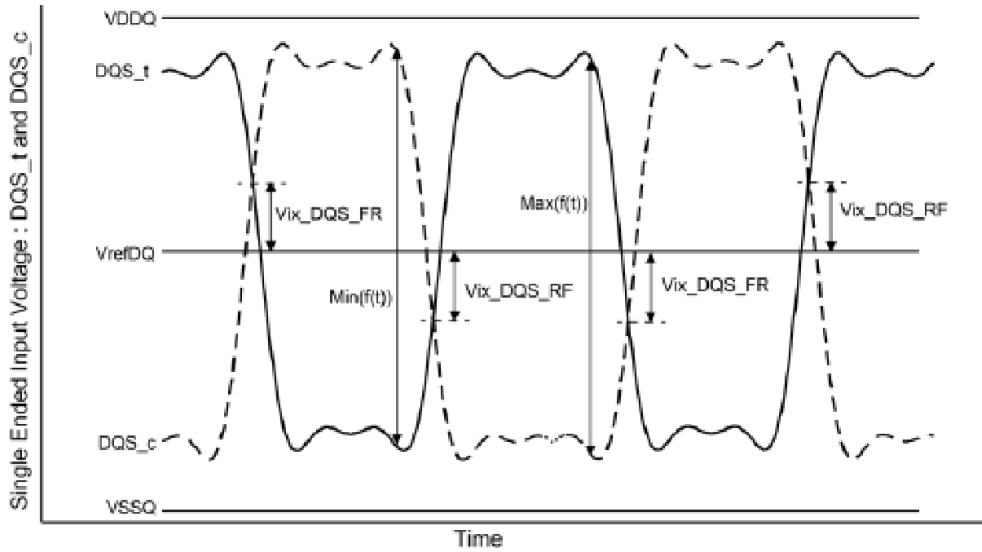


Figure 11. Definition of differential DQS Peak Voltage

### 8.7.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS<sub>t</sub>, DQS<sub>c</sub>) must meet the requirements in Table 17. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is VrefDQ.Vix Definition (DQS)



[ Table 17 ] Cross point voltage for differential input signals (DQS)

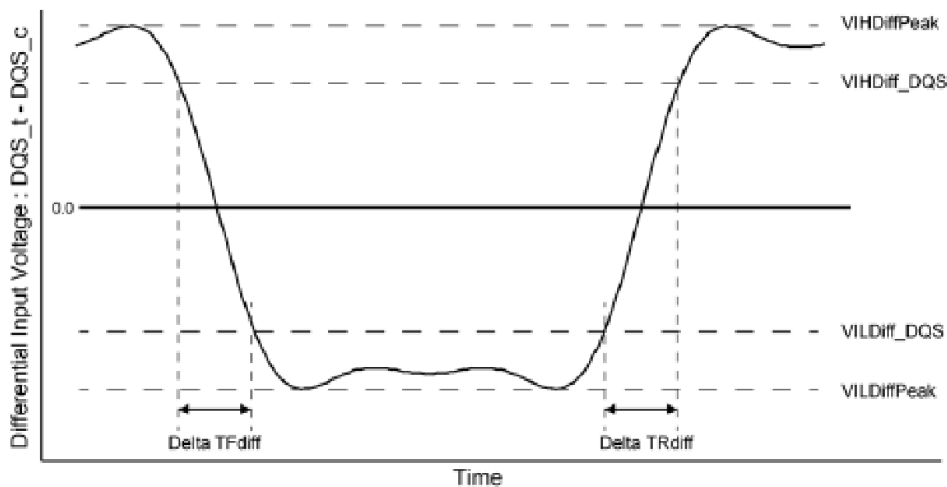
Symbol	Parameter	DDR4-1600, 1866, 2133		DDR4-2400		Unit	Note
		Min	Max	Min	Max		
Vix_DQS_ratio	DQS Differential input crosspoint voltage ratio	-	25	-	25	%	1, 2, 3

**NOTE :**

1. The base level of Vix\_DQS\_FR/RF is VrefDQ that is DDR4 SDRAM internal setting value by Vref Training.
2. Vix\_DQS\_FR is defined by this equation :  $Vix\_DQS\_FR = |\text{Min}(f(t)) \times Vix\_DQS\_Ratio|$
3. Vix\_DQS\_RF is defined by this equation :  $Vix\_DQS\_RF = \text{Max}(f(t)) \times Vix\_DQS\_Ratio$

### 8.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS<sub>t</sub>, DQS<sub>c</sub>) are defined and measured as shown in are DD and Table CC.



**NOTE :**

1. Differential signal rising edge from VILDiff\_DQS to VIHdiff\_DQS must be monotonic slope.
2. Differential signal falling edge from VIHdiff\_DQS to VILDiff\_DQS must be monotonic slope.

Figure 12. Differential Input Slew Rate Definition for DQS<sub>t</sub>, DQS<sub>c</sub>

[ Table 18 ] Differential Input Slew Rate Definition for DQS\_t, DQS\_c

Description	From		To		Defined by
	From	To	From	To	
Differential input slew rate for rising edge(DQS_t - DQS_c)	VILDiff_DQS	VIHDiff_DQS	VIHDiff_DQS	VILDiff_DQS	$ VILDiff\_DQS - VIHDiff\_DQS /\Delta t_{RDiff}$
Differential input slew rate for falling edge(DQS_t - DQS_c)	VIHDiff_DQS	VILDiff_DQS	VILDiff_DQS	VIHDiff_DQS	$ VILDiff\_DQS - VIHDiff\_DQS /\Delta t_{FDiff}$

[ Table 19 ] Differential Input Level for DQS\_t, DQS\_c

Symbol	Parameter	DDR4-1600, 1866, 2133		DDR4-2400		Unit	NOTE
		Min	Max	Min	Max		
VIHDiff_DQS	Differential Input High	136	-	TBD	TBD	mV	
VILDiff_DQS	Differential Input Low	-	-136	TBD	TBD	mV	

[ Table 20 ] Differential Input Slew Rate for DQS\_t, DQS\_c

Symbol	Parameter	DDR4-1600, 1866, 2133		DDR4-2400		Unit	NOTE
		Min	Max	Min	Max		
SRI <sub>diff</sub>	Differential Input Slew Rate	TBD	18	TBD	TBD	V/ns	

## 9. AC and DC output Measurement levels

### 9.1 Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors ( $R_{ON_{Pu}}$  and  $R_{ON_{Pd}}$ ) are defined as follows:

$$R_{ON_{Pu}} = \frac{V_{DDQ} - V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ON_{Pd}} \text{ is off}$$

$$R_{ON_{Pd}} = \frac{V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ON_{Pu}} \text{ is off}$$

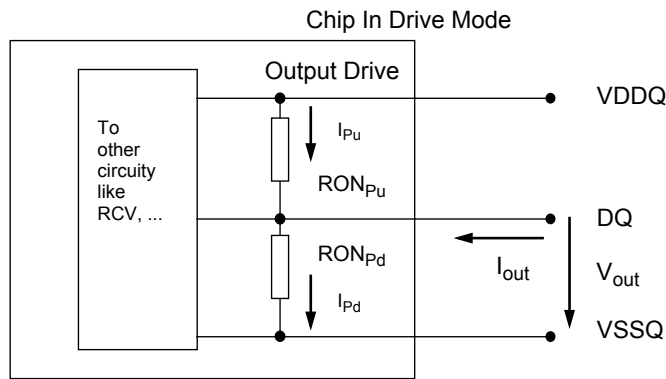


Figure 13. Output driver

[ Table 21 ] Output Driver DC Electrical Characteristics, assuming RZQ=240ohm; entire operating temperature range; after proper ZQ calibration

RON <sub>NOM</sub>	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10	-	10	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPuDD		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPdDD		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

**NOTE :**

- The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
- Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 \* VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 \* VDDQ and 1.1 \* VDDQ.
- Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8\*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

- RON variance range ratio to RON Nominal value in a given component, including DQS\_t and DQS\_c.

$$MMPuDD = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPdDD = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

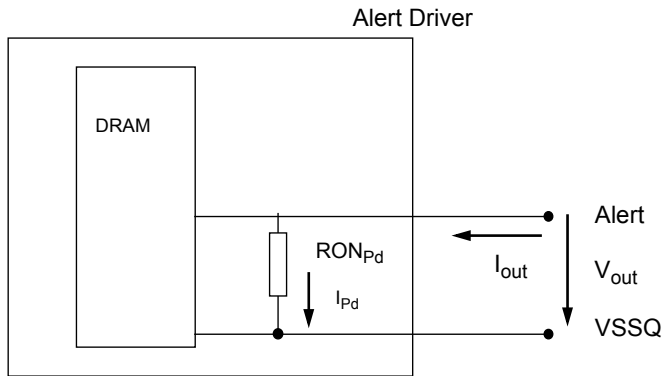
- This parameter of x16 device is specified for Uper byte and Lower byte.



9.1.1 Alert\_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{V_{out}}{|I_{out}|} \text{ under the condition that } RON_{Pu} \text{ is off}$$



RON <sub>NOM</sub>	Resistor	V <sub>out</sub>	Min	Nom	Max	Unit	NOTE
34Ω	RON <sub>34Pd</sub>	V <sub>OLdc</sub> = 0.1 * VDDQ	0.6	1	1.2	34Ω	1
		V <sub>OMdc</sub> = 0.8 * VDDQ	0.8	1	1.2	34Ω	1
		V <sub>OHdc</sub> = 1.1 * VDDQ	0.8	1	1.4	34Ω	1

NOTE :  
1. VDDQ voltage is at VDDQ DC. VDDQ DC definition is TBD.

9.1.2 Output Driver Characteristic of Connectivity Test ( CT ) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test ( CT ) Mode. The individual pull-up and pull-down resistors (RON<sub>Pu\_CT</sub> and RON<sub>Pd\_CT</sub>) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ} - V_{OUT}}{|I_{out}|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|I_{out}|}$$

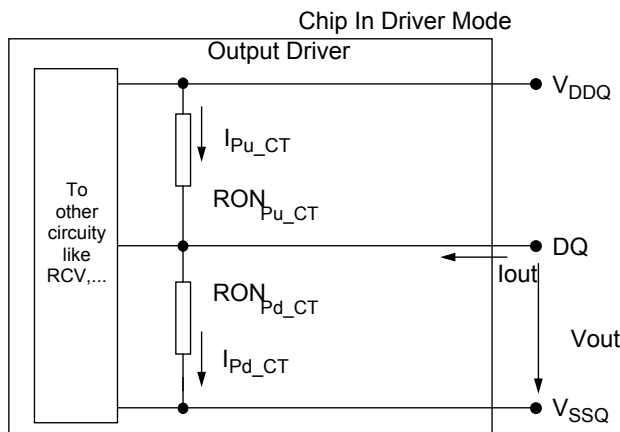


Figure 14. Output Driver

RON <sub>NOM_CT</sub>	Resistor	Vout	Max	Units	NOTE
34Ω	RON <sub>Pd_CT</sub>	VOB <sub>dc</sub> = 0.2 × V <sub>DDQ</sub>	1.9	34Ω	1
		VOL <sub>dc</sub> = 0.5 × V <sub>DDQ</sub>	1.1	34Ω	1
		VOM <sub>dc</sub> = 0.8 × V <sub>DDQ</sub>	2.2	34Ω	1
		VOH <sub>dc</sub> = 1.1 × V <sub>DDQ</sub>	2.5	34Ω	1
	RON <sub>Pu_CT</sub>	VOB <sub>dc</sub> = 0.2 × V <sub>DDQ</sub>	2.5	34Ω	1
		VOL <sub>dc</sub> = 0.5 × V <sub>DDQ</sub>	2.2	34Ω	1
		VOM <sub>dc</sub> = 0.8 × V <sub>DDQ</sub>	2.0	34Ω	1
		VOH <sub>dc</sub> = 1.1 × V <sub>DDQ</sub>	1.9	34Ω	1

**NOTE :**

1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

## 9.2 Single-ended AC & DC Output Levels

[ Table 22 ] Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400	Units	NOTE
V <sub>OH</sub> (DC)	DC output high measurement level (for IV curve linearity)	1.1 × V <sub>DDQ</sub>	V	
V <sub>OM</sub> (DC)	DC output mid measurement level (for IV curve linearity)	0.8 × V <sub>DDQ</sub>	V	
V <sub>OL</sub> (DC)	DC output low measurement level (for IV curve linearity)	0.5 × V <sub>DDQ</sub>	V	
V <sub>OH</sub> (AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) × V <sub>DDQ</sub>	V	1
V <sub>OL</sub> (AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) × V <sub>DDQ</sub>	V	1

**NOTE :**

1. The swing of ± 0.15 × V<sub>DDQ</sub> is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V<sub>TT</sub> = V<sub>DDQ</sub>.

## 9.3 Differential AC & DC Output Levels

[ Table 23 ] Differential AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400	Units	NOTE
V <sub>OHdiff</sub> (AC)	AC differential output high measurement level (for output SR)	+0.3 × V <sub>DDQ</sub>	V	1
V <sub>OLdiff</sub> (AC)	AC differential output low measurement level (for output SR)	-0.3 × V <sub>DDQ</sub>	V	1

**NOTE :**

1. The swing of ± 0.3 × V<sub>DDQ</sub> is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V<sub>TT</sub> = V<sub>DDQ</sub> at each of the differential outputs.

### 9.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $V_{OL(AC)}$  and  $V_{OH(AC)}$  for single ended signals as shown in Table 24 and Figure 15.

[ Table 24 ] Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{se}$
Single ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{se}$

**NOTE :**

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

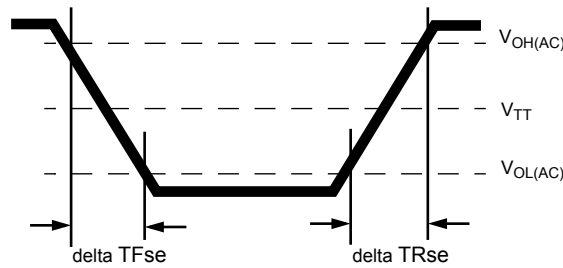


Figure 15. Single-ended Output Slew Rate Definition

[ Table 25 ] Single-ended output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

**NOTE :**

1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

### 9.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 26 and Figure 16.

[ Table 26 ] Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V <sub>OLdiff(AC)</sub>	V <sub>OHdiff(AC)</sub>	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TR_{diff}$
Differential output slew rate for falling edge	V <sub>OHdiff(AC)</sub>	V <sub>OLdiff(AC)</sub>	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TF_{diff}$

**NOTE :**

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

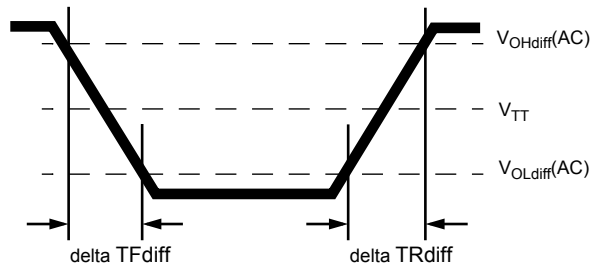


Figure 16. Differential Output Slew Rate Definition

[ Table 27 ] Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

## 9.6 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[ Table 28 ] Single-ended AC & DC output levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133 /2400	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$V_{TT} + (0.1 \times V_{DDQ})$	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	$V_{TT} - (0.1 \times V_{DDQ})$	V	1

**NOTE**

1. The effective test load is 50Ω terminated by  $V_{TT} = 0.5 \times V_{DDQ}$ .

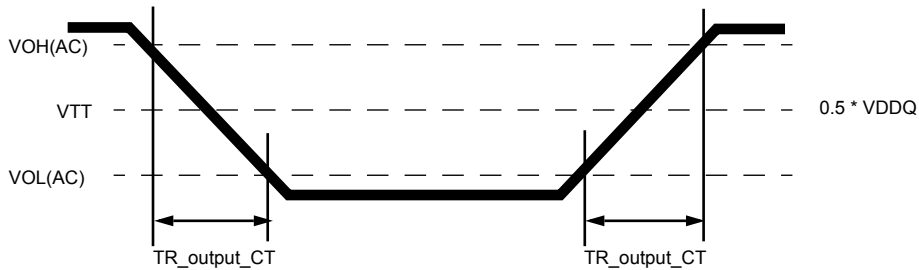


Figure 17. Output Slew Rate Definition of Connectivity Test Mode

[ Table 29 ] Single-ended output slew rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

## 9.7 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 18.

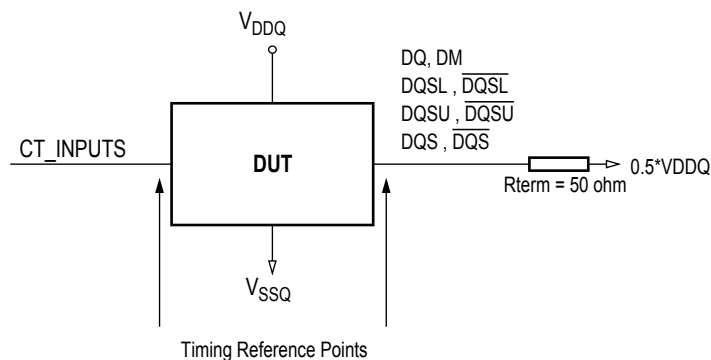


Figure 18. Connectivity Test Mode Timing Reference Load

## 10. Speed Bin

[ Table 30 ] DDR4-1600 Speed Bins and Operations

Speed Bin			DDR4-1600		Unit	NOTE	
CL-nRCD-nRP			11-11-11				
Parameter	Symbol		min	max			
Internal read command to first data			tAA	13.75	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) + 2nCK	ns	10
ACT to internal read or write delay time			tRCD	13.75	-	ns	10
PRE command period			tRP	13.75	-	ns	10
ACT to PRE command period			tRAS	35	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	48.75	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings			10,11,12		nCK	11	
Supported CL Settings with read DBI			12,13,14		nCK	11	
Supported CWL Settings			9,11		nCK		

[ Table 31 ] DDR4-1866 Speed Bins and Operations

Speed Bin			DDR4-1866		Unit	NOTE	
CL-nRCD-nRP			13-13-13				
Parameter	Symbol		min	max			
Internal read command to first data			tAA	13.92	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) + 2nCK	ns	10
ACT to internal read or write delay time			tRCD	13.92	-	ns	10
PRE command period			tRP	13.92	-	ns	10
ACT to PRE command period			tRAS	34	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	47.92	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15,16		nCK	11	
Supported CL Settings with read DBI			12,13,14,15,16,18,19		nCK	11	
Supported CWL Settings			9,10,11,12		nCK		

[ Table 32 ] DDR4-2133 Speed Bins and Operations

Speed Bin			DDR4-2133		Unit	NOTE	
CL-nRCD-nRP			15-15-15				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		14.06 (13.75) <sup>5</sup>	18.00	ns	10	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10	
ACT to internal read or write delay time	tRCD		14.06 (13.75) <sup>5</sup>	-	ns	10	
PRE command period	tRP		14.06 (13.75) <sup>5</sup>	-	ns	10	
ACT to PRE command period	tRAS		33	9 x tREFI	ns	10	
ACT to ACT or REF command period	tRC		47.06 (46.75) <sup>5</sup>	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,9
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15,16		nCK	11	
Supported CL Settings with read DBI			12,13,14,15,16,18,19		nCK		
Supported CWL Settings			9,10,11,12,14		nCK		

[ Table 33 ] DDR4-2400 Speed Bins and Operations

Speed Bin			DDR4-2400		Unit	NOTE	
CL-nRCD-nRP			17-17-17				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		14.16 (13.75) <sup>5</sup>	18.00	ns	10	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10	
ACT to internal read or write delay time	tRCD		14.16 (13.75) <sup>5</sup>	-	ns	10	
PRE command period	tRP		14.16 (13.75) <sup>5</sup>	-	ns	10	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	10	
ACT to ACT or REF command period	tRC		46.16 (45.75) <sup>5</sup>	-	ns	10	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.938		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.938	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15,16,17,18		nCK	11	
Supported CL Settings with read DBI			12,13,14,15,16,18,19,20,21		nCK		
Supported CWL Settings			9,10,11,12,14,16		nCK		



## 10.1 Speed Bin Table Note

### Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V

- VPP = 2.5V +0.25/-0.125 V

- The values defined with above-mentioned table are DLL ON case.

- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Programmed 13.75ns on the DIMM SPD to be backward compatible to the lower frequency. The system operates clock cycle is calculated by dividing tAA, tRCD, tRP(in ns) by tCK(in ns) and rounding up to the next integer. tRC = 13.75ns + tRAS
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
9. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
10. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
11. CL number in parentheses, it means that these numbers are optional.

## 11. IDD and IDDQ Specification Parameters and Test conditions

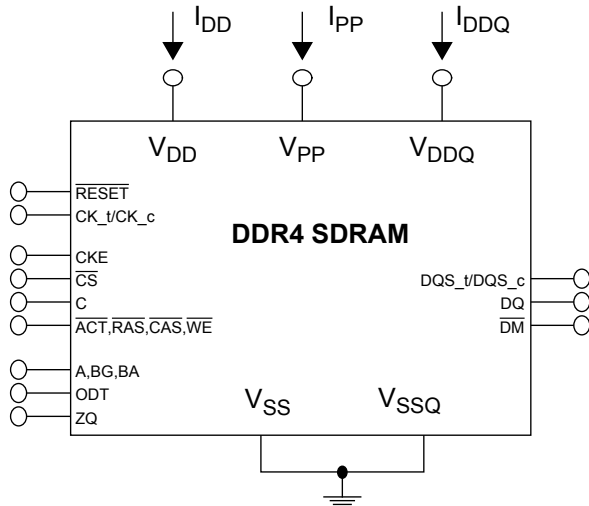
### 11.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 19 shows the setup and test load for IDD, IPP and IDDQ measurements.

- I IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- I IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- I IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.  
Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 20. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

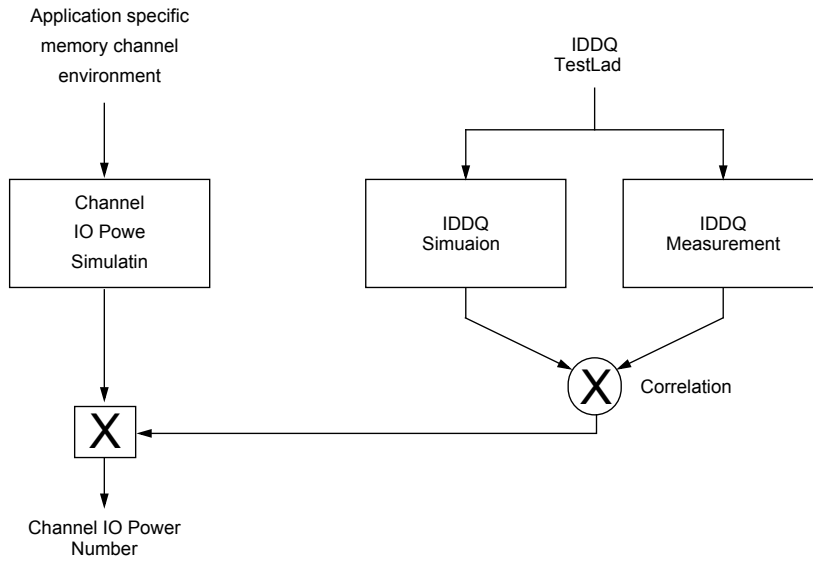
For IDD, IPP and IDDQ measurements, the following definitions apply:

- I "0" and "LOW" is defined as  $V_{IN} \leq V_{ILAC(max)}$ .
- I "1" and "HIGH" is defined as  $V_{IN} \geq V_{IHAC(min)}$ .
- I "MID-LEVEL" is defined as inputs are  $V_{REF} = V_{DD} / 2$ .
- I Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 34.
- I Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 35.
- I Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 36 through Table 44.
- I IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting  
 $R_{ON} = R_{ZQ}/7$  (34 Ohm in MR1);  
 $R_{TT\_NOM} = R_{ZQ}/6$  (40 Ohm in MR1);  
 $R_{TT\_WR} = R_{ZQ}/2$  (120 Ohm in MR2);  
 $R_{TT\_PARK} = \text{Disable}$ ;  
 $Q_{off} = 0_B$  (Output Buffer enabled) in MR1;  
 $T_{DQS\_t}$  disabled in MR1;  
CRC disabled in MR2;  
CA parity feature disabled in MR5;  
Gear down mode disabled in MR3  
Read/Write DBI disabled in MR5;  
DM disabled in MR5
- I Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- I Define D = {CS<sub>n</sub>, ACT<sub>n</sub>, RAS<sub>n</sub>, CAS<sub>n</sub>, WE<sub>n</sub>} := {HIGH, LOW, LOW, LOW, LOW}
- I Define D# = {CS<sub>n</sub>, ACT<sub>n</sub>, RAS<sub>n</sub>, CAS<sub>n</sub>, WE<sub>n</sub>} := {HIGH, HIGH, HIGH, HIGH, HIGH}



**NOTE:**  
1. DIMM level Output test load condition may be different from above

**Figure 19. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements**



**Figure 20. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.**

[ Table 34 ] Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
		11-11-11	13-13-13	15-15-15	17-17-17	
tCK		1.25	1.071	0.938	0.833	ns
CL		11	13	15	17	nCK
CWL		11	12	14	16	nCK
nRCD		11	13	15	17	nCK
nRC		39	45	51	56	nCK
nRAS		28	32	36	39	nCK
nRP		11	13	15	17	nCK
nFAW	x4	16	16	16	16	nCK
	x8	20	22	23	26	nCK
	x16	28	28	32	36	nCK
nRRDS	x4	4	4	4	4	nCK
	x8	4	4	4	4	nCK
	x16	5	5	6	7	nCK
nRRDL	x4	5	5	6	6	nCK
	x8	5	5	6	6	nCK
	x16	6	6	7	8	nCK
tCCD_S		4	4	4	4	nCK
tCCD_L		5	5	6	6	nCK
tWTR_S		2	3	3	3	nCK
tWTR_L		6	7	8	9	nCK
nRFC 2Gb		128	150	171	193	nCK
nRFC 4Gb		208	243	278	313	nCK
nRFC 8Gb		280	327	374	421	nCK
nRFC 16Gb		TBD	TBD	TBD	TBD	nCK
TBD						nCK

[ Table 35 ] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	<b>Operating One Bank Active-Precharge Current (AL=0)</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, nRC, nRAS, CL:</b> see Table 34 on page 36; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> High between ACT and PRE; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling according to Table 36 on page 40; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 36 on page 40); <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> see Table 36 on page 40
IDD0A	<b>Operating One Bank Active-Precharge Current (AL=CL-1)</b> <b>AL = CL-1, Other conditions:</b> see IDD0
IPP0	<b>Operating One Bank Active-Precharge IPP Current</b> <b>Same condition with IDD0</b>
IDD1	<b>Operating One Bank Active-Read-Precharge Current (AL=0)</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, nRC, nRAS, nRCD, CL:</b> see Table 34 on page 36; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> High between ACT, RD and PRE; <b>Command, Address, Bank Group Address, Bank Address Inputs, Data IO:</b> partially toggling according to Table 37 on page 41; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 37 on page 41); <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> see Table 37 on page 41
IDD1A	<b>Operating One Bank Active-Read-Precharge Current (AL=CL-1)</b> <b>AL = CL-1, Other conditions:</b> see IDD1
IPP1	<b>Operating One Bank Active-Read-Precharge IPP Current</b> <b>Same condition with IDD1</b>
IDD2N	<b>Precharge Standby Current (AL=0)</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> see Table 34 on page 36; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling according to Table 38 on page 42; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> see Table 38 on page 42
IDD2NA	<b>Precharge Standby Current (AL=CL-1)</b> <b>AL = CL-1, Other conditions:</b> see IDD2N
IPP2N	<b>Precharge Standby IPP Current</b> <b>Same condition with IDD2N</b>
IDD2NT	<b>Precharge Standby ODT Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> see Table 34 on page 36; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling according to Table 39 on page 43; <b>Data IO:</b> VSSQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> toggling according to Table 39 on page 43; <b>Pattern Details:</b> see Table 39 on page 43
IDDQ2NT (Optional)	<b>Precharge Standby ODT IDDQ Current</b> Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	<b>Precharge Standby Current with CAL enabled</b> Same definition like for IDD2N, CAL enabled <sup>3</sup>
IDD2NG	<b>Precharge Standby Current with Gear Down mode enabled</b> Same definition like for IDD2N, Gear Down mode enabled <sup>3</sup>
IDD2ND	<b>Precharge Standby Current with DLL disabled</b> Same definition like for IDD2N, DLL disabled <sup>3</sup>
IDD2N_par	<b>Precharge Standby Current with CA parity enabled</b> Same definition like for IDD2N, CA parity enabled <sup>3</sup>
IDD2P	<b>Precharge Power-Down Current</b> <b>CKE:</b> Low; <b>External clock:</b> On; <b>tCK, CL:</b> see Table 34 on page 36; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0
IPP2P	<b>Precharge Power-Down IPP Current</b> <b>Same condition with IDD2P</b>
IDD2Q	<b>Precharge Quiet Standby Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> see Table 34 on page 36; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks closed; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0
IDD3N	<b>Active Standby Current</b> <b>CKE:</b> High; <b>External clock:</b> On; <b>tCK, CL:</b> see Table 34 on page 36; <b>BL:</b> 8 <sup>1</sup> ; <b>AL:</b> 0; <b>CS_n:</b> stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling according to Table 38 on page 42; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks open; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> see Table 38 on page 42

Symbol	Description
IDD3NA	<b>Active Standby Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD3N
IPP3N	<b>Active Standby IPP Current</b> Same condition with IDD3N
IDD3P	<b>Active Power-Down Current</b> CKE: Low; External clock: On; tCK, CL: see Table 34 on page 36; BL: 8 <sup>1</sup> ; AL: 0; CS_n: stable at 1; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> stable at 0; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks open; <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0
IPP3P	<b>Active Power-Down IPP Current</b> Same condition with IDD3P
IDD4R	<b>Operating Burst Read Current</b> CKE: High; External clock: On; tCK, CL: see Table 34 on page 36; BL: 8 <sup>2</sup> ; AL: 0; CS_n: High between RD; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling according to Table 40 on page 44; <b>Data IO:</b> seamless read data burst with different data between one burst and the next one according to Table 40 on page 44; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 40 on page 44); <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> see Table 40 on page 44
IDD4RA	<b>Operating Burst Read Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD4R
IDD4RB	<b>Operating Burst Read Current with Read DBI</b> Read DBI enabled <sup>3</sup> , Other conditions: see IDD4R
IPP4R	<b>Operating Burst Read IPP Current</b> Same condition with IDD4R
IDDQ4R (Optional)	<b>Operating Burst Read IDDQ Current</b> Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	<b>Operating Burst Read IDDQ Current with Read DBI</b> Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	<b>Operating Burst Write Current</b> CKE: High; External clock: On; tCK, CL: see Table 34 on page 36; BL: 8 <sup>1</sup> ; AL: 0; CS_n: High between WR; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling according to Table 41 on page 45; <b>Data IO:</b> seamless write data burst with different data between one burst and the next one according to Table 41 on page 45; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 41 on page 45); <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at HIGH; <b>Pattern Details:</b> see Table 41 on page 45
IDD4WA	<b>Operating Burst Write Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD4W
IDD4WB	<b>Operating Burst Write Current with Write DBI</b> Write DBI enabled <sup>3</sup> , Other conditions: see IDD4W
IDD4WC	<b>Operating Burst Write Current with Write CRC</b> Write CRC enabled <sup>3</sup> , Other conditions: see IDD4W
IDD4W_par	<b>Operating Burst Write Current with CA Parity</b> CA Parity enabled <sup>3</sup> , Other conditions: see IDD4W
IPP4W	<b>Operating Burst Write IPP Current</b> Same condition with IDD4W
IDD5B	<b>Burst Refresh Current (1X REF)</b> CKE: High; External clock: On; tCK, CL, nRFC: see Table 34 on page 36; BL: 8 <sup>1</sup> ; AL: 0; CS_n: High between REF; <b>Command, Address, Bank Group Address, Bank Address Inputs:</b> partially toggling according to Table 43 on page 47; <b>Data IO:</b> VDDQ; <b>DM_n:</b> stable at 1; <b>Bank Activity:</b> REF command every nRFC (see Table 43 on page 47); <b>Output Buffer and RTT:</b> Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal:</b> stable at 0; <b>Pattern Details:</b> see Table 43 on page 47
IPP5B	<b>Burst Refresh Write IPP Current (1X REF)</b> Same condition with IDD5B
IDD5F2	<b>Burst Refresh Current (2X REF)</b> tRFC=tRFC_x2, Other conditions: see IDD5B
IPP5F2	<b>Burst Refresh Write IPP Current (2X REF)</b> Same condition with IDD5F2
IDD5F4	<b>Burst Refresh Current (4X REF)</b> tRFC=tRFC_x4, Other conditions: see IDD5B
IPP5F4	<b>Burst Refresh Write IPP Current (4X REF)</b> Same condition with IDD5F4

Symbol	Description
IDD6N	<b>Self Refresh Current: Normal Temperature Range</b> TCASE: 0 - 85°C; <b>Low Power Array Self Refresh (LP ASR)</b> : Normal <sup>4</sup> ; <b>CKE</b> : Low; <b>External clock</b> : Off; CK_t and CK_c#: LOW; <b>CL</b> : see Table 34 on page 36; <b>BL</b> : 8 <sup>1</sup> ; <b>AL</b> : 0; <b>CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO</b> : High; <b>DM_n</b> : stable at 1; <b>Bank Activity</b> : Self-Refresh operation; <b>Output Buffer and RTT</b> : Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal</b> : MID-LEVEL
IPP6N	<b>Self Refresh IPP Current: Normal Temperature Range</b> Same condition with IDD6N
IDD6E	<b>Self-Refresh Current: Extended Temperature Range</b> <sup>)</sup> TCASE: 0 - 95°C; <b>Low Power Array Self Refresh (LP ASR)</b> : Extended <sup>4</sup> ; <b>CKE</b> : Low; <b>External clock</b> : Off; CK_t and CK_c#: LOW; <b>CL</b> : see Table 34 on page 36; <b>BL</b> : 8 <sup>1</sup> ; <b>AL</b> : 0; <b>CS_n, Command, Address, Bank Group Address, Bank Address, Data IO</b> : High; <b>DM_n</b> :stable at 1; <b>Bank Activity</b> : Extended Temperature Self-Refresh operation; <b>Output Buffer and RTT</b> : Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal</b> : MID-LEVEL
IPP6E	<b>Self Refresh IPP Current: Extended Temperature Range</b> Same condition with IDD6E
IDD6R	<b>Self-Refresh Current: Reduced Temperature Range</b> TCASE: 0 - TBD (~35-45)°C; <b>Low Power Array Self Refresh (LP ASR)</b> : Reduced <sup>4</sup> ; <b>CKE</b> : Low; <b>External clock</b> : Off; CK_t and CK_c#: LOW; <b>CL</b> : see Table 34 on page 36; <b>BL</b> : 8 <sup>1</sup> ; <b>AL</b> : 0; <b>CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO</b> : High; <b>DM_n</b> :stable at 1; <b>Bank Activity</b> : Extended Temperature Self-Refresh operation; <b>Output Buffer and RTT</b> : Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal</b> : MID-LEVEL
IPP6R	<b>Self Refresh IPP Current: Reduced Temperature Range</b> Same condition with IDD6R
IDD6A	<b>Auto Self-Refresh Current</b> TCASE: 0 - 95°C; <b>Low Power Array Self Refresh (LP ASR)</b> : Auto <sup>4</sup> ; <b>CKE</b> : Low; <b>External clock</b> : Off; CK_t and CK_c#: LOW; <b>CL</b> : see Table 34 on page 36; <b>BL</b> : 8 <sup>1</sup> ; <b>AL</b> : 0; <b>CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO</b> : High; <b>DM_n</b> :stable at 1; <b>Bank Activity</b> : Auto Self-Refresh operation; <b>Output Buffer and RTT</b> : Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal</b> : MID-LEVEL
IPP6A	<b>Auto Self-Refresh IPP Current</b> Same condition with IDD6A
IDD7	<b>Operating Bank Interleave Read Current</b> <b>CKE</b> : High; <b>External clock</b> : On; <b>tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL</b> : see Table 34 on page 36; <b>BL</b> : 8 <sup>1</sup> ; <b>AL</b> : CL-1; <b>CS_n</b> : High between ACT and RDA; <b>Command, Address, Bank Group Address, Bank Address Inputs</b> : partially toggling according to Table 44 on page 48; <b>Data IO</b> : read data bursts with different data between one burst and the next one according to Table 44 on page 48; <b>DM_n</b> : stable at 1; <b>Bank Activity</b> : two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 44 on page 48; <b>Output Buffer and RTT</b> : Enabled in Mode Registers <sup>2</sup> ; <b>ODT Signal</b> : stable at 0; <b>Pattern Details</b> : see Table 44 on page 48
IPP7	<b>Operating Bank Interleave Read IPP Current</b> Same condition with IDD7
IDD8	<b>Maximum Power Down Current</b> TBD
IPP8	<b>Maximum Power Down IPP Current</b> Same condition with IDD8

**NOTE :**

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
  - set MR1 [A12 = 0] : Qoff = Output buffer enabled
  - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
  - RTT\_Nom enable
  - set MR1 [A10:8 = 011] : RTT\_NOM = RZQ/6
  - RTT\_WR enable
  - set MR2 [A10:9 = 01] : RTT\_WR = RZQ/2
  - RTT\_PARK disable
  - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s  
   010] : 1866MT/s, 2133MT/s  
   011] : 2400MT/s  
 Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate  
 DLL disabled : set MR1 [A0 = 0]  
 CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s  
   010] : 2400MT/s  
 Read DBI enabled : set MR5 [A12 = 1]  
 Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal  
   01] : Reduced Temperature range  
   10] : Extended Temperature range  
   11] : Auto Self Refresh
5. IDD2NG should be measured after sync pulse(NOP) input.

[ Table 36 ] IDD0, IDD0A and IPP0 Measurement-Loop Pattern<sup>1</sup>

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>				
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-			
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3,4	D_#, D_#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	0	-	
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																				
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																				
		1	1*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 1</b> instead																				
		2	2*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 2</b> instead																				
		3	3*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 3</b> instead																				
		4	4*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 1</b> instead																				
		5	5*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 2</b> instead																				
		6	6*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 3</b> instead																				
		7	7*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 0</b> instead																				
		8	8*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 0</b> instead																				
		9	9*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 1</b> instead																				
10	10*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 2</b> instead																						
11	11*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 3</b> instead																						
12	12*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 1</b> instead																						
13	13*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 2</b> instead																						
14	14*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 3</b> instead																						
15	15*nRC	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 0</b> instead																						

- NOTE :**  
 1. DQS\_t, DQS\_c are VDDQ.  
 2. BG1 is don't care for x16 device  
 3. C[2:0] are used only for 3DS device  
 4. DQ signals are VDDQ.

For x4 and x8 only





[ Table 37 ] IDD1, IDD1A and IPP1 Measurement-Loop Pattern<sup>1</sup>

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-			
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			3, 4	D#, D#	1	1	1	1	1	1	0	0	3 <sup>b</sup>	3	3	0	0	0	7	F	0	-	
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																			
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																			
			1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	1	0	0	0	0	0	0	-	
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	0	0	0	3 <sup>b</sup>	3	3	0	0	0	7	F	0	-	
		...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																				
		1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
		...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																				
		1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																				
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		8	7*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		9	9*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
		11	11*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																			
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																			
13	13*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																					
14	14*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																					
15	15*nRC	repeat Sub-Loop 1, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																					
16	16*nRC	repeat Sub-Loop 0, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																					

For x4 and x8 only

NOTE :

1. DQS\_t, DQS\_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

[ Table 38 ] IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N\_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern<sup>1</sup>

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	0	0
			3	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	0	0
		1	4-7	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 1</b> instead																			
		2	8-11	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 2</b> instead																			
		3	12-15	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 3</b> instead																			
		4	16-19	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 1</b> instead																			
		5	20-23	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 2</b> instead																			
		6	24-27	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 3</b> instead																			
		7	28-31	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 0</b> instead																			
		8	32-35	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 0</b> instead																			
		9	36-39	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 1</b> instead																			
		10	40-43	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 2</b> instead																			
		11	44-47	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 3</b> instead																			
		12	48-51	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 1</b> instead																			
13	52-55	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 2</b> instead																					
14	56-59	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 3</b> instead																					
15	60-63	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 0</b> instead																					

NOTE :

1. DQS\_t, DQS\_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

[ Table 39 ] IDD2NT and IDDQ2NT Measurement-Loop Pattern<sup>1</sup>

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>		
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	-
			3	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 1, BA[1:0] = 1 instead																		
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																		
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																		
12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																				
13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																				

- NOTE :**  
 1. DQS\_t, DQS\_c are VDDQ.  
 2. BG1 is don't care for x16 device  
 3. C[2:0] are used only for 3DS device  
 4. DQ signals are VDDQ.

For x4 and x8 only



[ Table 40 ] IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern<sup>1</sup>

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2,3	D#, D#	1	1	1	1	1	1	0	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	-	
		1	4	RD	0	1	1	0	1	0	0	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	-	
		2	8-11	repeat Sub-Loop 0, use $BG[1:0]^2 = 0$ , $BA[1:0] = 2$ instead																			
		3	12-15	repeat Sub-Loop 1, use $BG[1:0]^2 = 1$ , $BA[1:0] = 3$ instead																			
		4	16-19	repeat Sub-Loop 0, use $BG[1:0]^2 = 0$ , $BA[1:0] = 1$ instead																			
		5	20-23	repeat Sub-Loop 1, use $BG[1:0]^2 = 1$ , $BA[1:0] = 2$ instead																			
		6	24-27	repeat Sub-Loop 0, use $BG[1:0]^2 = 0$ , $BA[1:0] = 3$ instead																			
		7	28-31	repeat Sub-Loop 1, use $BG[1:0]^2 = 1$ , $BA[1:0] = 0$ instead																			
		8	32-35	repeat Sub-Loop 0, use $BG[1:0]^2 = 2$ , $BA[1:0] = 0$ instead																			
		9	36-39	repeat Sub-Loop 1, use $BG[1:0]^2 = 3$ , $BA[1:0] = 1$ instead																			
		10	40-43	repeat Sub-Loop 0, use $BG[1:0]^2 = 2$ , $BA[1:0] = 2$ instead																			
11	44-47	repeat Sub-Loop 1, use $BG[1:0]^2 = 3$ , $BA[1:0] = 3$ instead																					
12	48-51	repeat Sub-Loop 0, use $BG[1:0]^2 = 2$ , $BA[1:0] = 1$ instead																					
13	52-55	repeat Sub-Loop 1, use $BG[1:0]^2 = 3$ , $BA[1:0] = 2$ instead																					
14	56-59	repeat Sub-Loop 0, use $BG[1:0]^2 = 2$ , $BA[1:0] = 3$ instead																					
15	60-63	repeat Sub-Loop 1, use $BG[1:0]^2 = 3$ , $BA[1:0] = 0$ instead																					
																				For x4 and x8 only			

- NOTE :**  
 1. DQS\_t, DQS\_c are used according to RD Commands, otherwise VDDQ.  
 2. BG1 is don't care for x16 device  
 3. C[2:0] are used only for 3DS device  
 4. Burst Sequence driven on each DQ signal by Read Command.



[ Table 41 ] IDD4W, IDD4WA, IDD4WB and IDD4W\_par Measurement-Loop Pattern<sup>1</sup>

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>		
toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-
		1	4	WR	0	1	1	0	1	0	0	0	1	1	0	0	0	7	F	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-
		2	8-11	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 2</b> instead																		
		3	12-15	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 3</b> instead																		
		4	16-19	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 1</b> instead																		
		5	20-23	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 2</b> instead																		
		6	24-27	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 3</b> instead																		
		7	28-31	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 0</b> instead																		
		8	32-35	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 0</b> instead																		
		9	36-39	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 1</b> instead																		
		10	40-43	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 2</b> instead																		
11	44-47	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 3</b> instead																				
12	48-51	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 1</b> instead																				
13	52-55	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 2</b> instead																				
14	56-59	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 3</b> instead																				
15	60-63	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 0</b> instead																				
																				For x4 and x8 only		

- NOTE :**
1. DQS\_t, DQS\_c are used according to WR Commands, otherwise VDDQ.
  2. BG1 is don't care for x16 device
  3. C[2:0] are used only for 3DS device
  4. Burst Sequence driven on each DQ signal by Write Command.

[ Table 42 ] IDD4WC Measurement-Loop Pattern<sup>1</sup>

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>		
toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC	
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	-
			5	WR	0	1	1	0	1	0	0	0	1	1	0	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	0	7	F	0	-
		2	10-14	repeat Sub-Loop 0, use $BG[1:0]^2 = 0$ , $BA[1:0] = 2$ instead																		
		3	15-19	repeat Sub-Loop 1, use $BG[1:0]^2 = 1$ , $BA[1:0] = 3$ instead																		
		4	20-24	repeat Sub-Loop 0, use $BG[1:0]^2 = 0$ , $BA[1:0] = 1$ instead																		
		5	25-29	repeat Sub-Loop 1, use $BG[1:0]^2 = 1$ , $BA[1:0] = 2$ instead																		
		6	30-34	repeat Sub-Loop 0, use $BG[1:0]^2 = 0$ , $BA[1:0] = 3$ instead																		
		7	35-39	repeat Sub-Loop 1, use $BG[1:0]^2 = 1$ , $BA[1:0] = 0$ instead																		
		8	40-44	repeat Sub-Loop 0, use $BG[1:0]^2 = 2$ , $BA[1:0] = 0$ instead																		
		9	45-49	repeat Sub-Loop 1, use $BG[1:0]^2 = 3$ , $BA[1:0] = 1$ instead																		
		10	50-54	repeat Sub-Loop 0, use $BG[1:0]^2 = 2$ , $BA[1:0] = 2$ instead																		
11	55-59	repeat Sub-Loop 1, use $BG[1:0]^2 = 3$ , $BA[1:0] = 3$ instead																				
12	60-64	repeat Sub-Loop 0, use $BG[1:0]^2 = 2$ , $BA[1:0] = 1$ instead																				
13	65-69	repeat Sub-Loop 1, use $BG[1:0]^2 = 3$ , $BA[1:0] = 2$ instead																				
14	70-74	repeat Sub-Loop 0, use $BG[1:0]^2 = 2$ , $BA[1:0] = 3$ instead																				
15	75-79	repeat Sub-Loop 1, use $BG[1:0]^2 = 3$ , $BA[1:0] = 0$ instead																				

NOTE :

1. DQS\_t, DQS\_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Write Command.

For x4 and x8 only

[ Table 43 ] IDD5B Measurement-Loop Pattern<sup>1</sup>

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>		
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		2	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		3	3	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-
		4	4	D#, D#	1	1	1	1	1	1	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-
		4-7	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 1 instead																			
		8-11	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 2 instead																			
		12-15	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 3 instead																			
		16-19	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 1 instead																			
		20-23	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 2 instead																			
		24-27	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 0, BA[1:0] = 3 instead																			
		28-31	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 1, BA[1:0] = 0 instead																			
		32-35	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 0 instead																			
		36-39	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 1 instead																			
		40-43	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 2 instead																			
		44-47	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 3 instead																			
		48-51	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 1 instead																			
		52-55	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 2 instead																			
		56-59	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 2, BA[1:0] = 3 instead																			
		60-63	repeat pattern 1...4, use BG[1:0] <sup>2</sup> = 3, BA[1:0] = 0 instead																			
2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																				

For x4 and x8 only

- NOTE :**  
 1. DQS\_t, DQS\_c are VDDQ.  
 2. BG1 is don't care for x16 device.  
 3. C[2:0] are used only for 3DS device.  
 4. DQ signals are VDDQ.



[ Table 44 ] IDD7 Measurement-Loop Pattern<sup>1</sup>

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0] <sup>3</sup>	BG[1:0] <sup>2</sup>	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data <sup>4</sup>			
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1	RDA	0	1	1	0	1	0		0	0	0	0	0	1	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	1	0	0	0	3 <sup>2</sup>	3	0	0	0	7	F	0	0	-
		...	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																				
		1	nRRD	ACT	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0		0	0	1	1	0	0	1	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
		...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																				
		2	2*nRRD	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 2</b> instead																			
		3	3*nRRD	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 3</b> instead																			
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																			
		5	nFAW	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 1</b> instead																			
		6	nFAW + nRRD	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 2</b> instead																			
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 0, BA[1:0] = 3</b> instead																			
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 1, BA[1:0] = 0</b> instead																			
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																			
		10	2*nFAW	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 0</b> instead																			
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 1</b> instead																			
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 2</b> instead																			
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 3</b> instead																			
14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																					
15	3*nFAW	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 1</b> instead																					
16	3*nFAW + nRRD	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 2</b> instead																					
17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use <b>BG[1:0]<sup>2</sup> = 2, BA[1:0] = 3</b> instead																					
18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use <b>BG[1:0]<sup>2</sup> = 3, BA[1:0] = 0</b> instead																					
19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																					
20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																					

- NOTE :**  
 1. DQS\_t, DQS\_c are VDDQ.  
 2. BG1 is don't care for x16 device.  
 3. C[2:0] are used only for 3DS device.  
 4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

For x4 and x8 only



### 11.2 4Gb DDR4 SDRAM D-die IDD Specification Table

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

[ Table 45 ]  $I_{DD}$  and  $I_{DDQ}$  Specification

Symbol	1Gx4 (K4A4G045WD)		512Mx8 (K4A4G085WD)		Unit	NOTE
	DDR4-2133	DDR4-2400	DDR4-2133	DDR4-2400		
	15-15-15	17-17-17	15-15-15	17-17-17		
	1.2V	1.2V	1.2V	1.2V		
	IDD Max.	IDD Max.	IDD Max.	IDD Max.		
$I_{DD0}$	33	34	TBD	TBD	mA	
$I_{DD0A}$	36	38	TBD	TBD	mA	
$I_{DD1}$	41	42	TBD	TBD	mA	
$I_{DD1A}$	44	46	TBD	TBD	mA	
$I_{DD2N}$	16	18	TBD	TBD	mA	
$I_{DD2NA}$	23	25	TBD	TBD	mA	
$I_{DD2NT}$	18	20	TBD	TBD	mA	
$I_{DD2NL}$	14	15	TBD	TBD	mA	
$I_{DD2NG}$	19	20	TBD	TBD	mA	
$I_{DD2ND}$	14	15	TBD	TBD	mA	
$I_{DD2N\_par}$	19	20	TBD	TBD	mA	
$I_{DD2P}$	11	11	TBD	TBD	mA	
$I_{DD2Q}$	15	17	TBD	TBD	mA	
$I_{DD3N}$	30	32	TBD	TBD	mA	
$I_{DD3NA}$	35	37	TBD	TBD	mA	
$I_{DD3P}$	15	16	TBD	TBD	mA	
$I_{DD4R}$	83	90	TBD	TBD	mA	
$I_{DD4RA}$	85	94	TBD	TBD	mA	
$I_{DD4RB}$	84	92	TBD	TBD	mA	
$I_{DD4W}$	72	76	TBD	TBD	mA	
$I_{DD4WA}$	76	80	TBD	TBD	mA	
$I_{DD4WB}$	72	76	TBD	TBD	mA	
$I_{DD4WC}$	65	68	TBD	TBD	mA	
$I_{DD4W\_par}$	81	87	TBD	TBD	mA	
$I_{DD5B}$	153	154	TBD	TBD	mA	
$I_{DD5F2}$	128	128	TBD	TBD	mA	
$I_{DD5F4}$	97	97	TBD	TBD	mA	
$I_{DD6N}$	12	12	TBD	TBD	mA	
$I_{DD6E}$	16	16	TBD	TBD	mA	
$I_{DD6R}$	9	9	TBD	TBD	mA	
$I_{DD6A}$	12	12	TBD	TBD	mA	
$I_{DD7}$	138	140	TBD	TBD	mA	
$I_{DD8}$	7	7	TBD	TBD	mA	

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

[ Table 46 ]  $I_{PP}$  Specification

Symbol	1Gx4 (K4A4G0485WD)		512Mx8 (K4A4G085WD)		Unit	NOTE
	DDR4-2133	DDR4-2400	DDR4-2133	DDR4-2400		
	15-15-15	17-17-17	15-15-15	17-17-17		
	1.2V	1.2V	1.2V	1.2V		
	IPP Max.	IPP Max.	IPP Max.	IPP Max.		
$I_{PP0}$	1.5	1.5	TBD	TBD	mA	
$I_{PP1}$	1.5	1.4	TBD	TBD	mA	
$I_{PP2N}$	1.2	1.2	TBD	TBD	mA	
$I_{PP2P}$	1.2	1.2	TBD	TBD	mA	
$I_{PP3N}$	1.2	1.2	TBD	TBD	mA	
$I_{PP3P}$	1.2	1.2	TBD	TBD	mA	
$I_{PP4R}$	1.2	1.2	TBD	TBD	mA	
$I_{PP4W}$	1.2	1.2	TBD	TBD	mA	
$I_{PP5B}$	17.5	17.6	TBD	TBD	mA	
$I_{PP5F2}$	14.4	14.4	TBD	TBD	mA	
$I_{PP5F4}$	10.7	10.7	TBD	TBD	mA	
$I_{PP6N}$	1.4	1.4	TBD	TBD	mA	
$I_{PP6E}$	2.0	2.0	TBD	TBD	mA	
$I_{PP6R}$	1.1	1.1	TBD	TBD	mA	
$I_{PP6A}$	1.4	1.4	TBD	TBD	mA	
$I_{PP7}$	7.1	7.1	TBD	TBD	mA	
$I_{PP8}$	0.7	0.7	TBD	TBD	mA	

[ Table 47 ]  $I_{DD6}$  Specification

Symbol	Temperature Range	Value		Value		Unit	NOTE
		1Gx4 (K4A4G045WD)		512Mx8 (K4A4G085WD)			
		DDR4-2133	DDR4-2400	DDR4-2133	DDR4-2400		
		15-15-15	17-17-17	15-15-15	17-17-17		
		1.2V		1.2V			
$I_{DD6N}$	0 - 85 °C	12	12	TBD	TBD	mA	3,4
$I_{DD6E}$	0 - 95 °C	16	16	TBD	TBD	mA	4,5,6
$I_{DD6R}$	0 - 45°C	9	9	TBD	TBD	mA	4,6,8
$I_{DD6A}$	0 - 85 °C	12	12	TBD	TBD	mA	4,6,7

**NOTE :**

1. Some  $I_{DD}$  currents are higher for x16 organization due to larger page-size architecture.
2. Max. values for  $I_{DD}$  currents considering worst case conditions of process, temperature and voltage.
3. Applicable for MR2 settings A6=0 and A7=0.
4. Supplier data sheets include a max value for  $I_{DD6}$ .
5. Applicable for MR2 settings A6=0 and A7=1.  $I_{DD6ET}$  is only specified for devices which support the Extended Temperature Range feature.
6. Refer to the supplier data sheet for the value specification method (e.g. max, typical) for  $I_{DD6ET}$  and  $I_{DD6TC}$
7. Applicable for MR2 settings A6=1 and A7=0.  $I_{DD6TC}$  is only specified for devices which support the Auto Self Refresh feature.
8. Applicable for MR2 settings TBD.  $I_{DD6R}$  is verified by design and characterization, and may not be subject to production test.

## 12. Input/Output Capacitance

[ Table 48 ] Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	NOTE
		min	max	min	max		
C <sub>IO</sub>	Input/output capacitance	0.7	1.4	0.7	1.3	pF	1,2,3
C <sub>DIO</sub>	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C <sub>DDQS</sub>	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	1,2,3,5
C <sub>CK</sub>	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	pF	1,3
C <sub>DCK</sub>	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	1,3,4
C <sub>I</sub>	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	pF	1,3,6
C <sub>DI_CTRL</sub>	Input capacitance delta(All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
C <sub>DI_ADD_CMD</sub>	Input capacitance delta(All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C <sub>ALERT</sub>	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	1,3
C <sub>ZQ</sub>	Input/output capacitance of ZQ	0.5	2.3	0.5	2.3	pF	1,3,12
C <sub>TEN</sub>	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

**NOTE:**

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM\_n, DQS\_T, DQS\_C, TDQS\_T, TDQS\_C. Although the DM, TDQS\_T and TDQS\_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK\_T-CK\_C
5. Absolute value of CIO(DQS\_T)-CIO(DQS\_C)
6. CI applies to ODT, CS\_n, CKE, A0-A15, BA0-BA1, BG0-BG1, RAS\_n, CAS\_n/A15, WE\_n/A14, ACT\_n and PAR.
7. CDI\_CTRL applies to ODT, CS\_n and CKE
8.  $CDI\_CTRL = CI(CTRL) - 0.5 * (CI(CLK\_T) + CI(CLK\_C))$
9. CDI\_ADD\_CMD applies to, A0-A15, BA0-BA1, BG0-BG1, RAS\_n, CAS\_n/A15, WE\_n/A14, ACT\_n and PAR.
10.  $CDI\_ADD\_CMD = CI(ADD\_CMD) - 0.5 * (CI(CLK\_T) + CI(CLK\_C))$
11.  $CDIO = CIO(DQ, DM) - 0.5 * (CIO(DQS\_T) + CIO(DQS\_C))$
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

[ Table 49 ] DRAM package electrical specifications

Symbol	Parameter	DDR4-1600/1866		DDR4-2133,2400		Unit	NOTE
		min	max	min	max		
Z <sub>IO</sub>	Input/output Zpkg	45	85	50	85	Ω	1,2,4,5,10,11
T <sub>dIO</sub>	Input/output Pkg Delay	14	42	14	37	ps	1,3,4,5,11
L <sub>io</sub>	Input/Output Lpkg	-	3.3	-	3.3	nH	11,12
C <sub>io</sub>	Input/Output Cpkg	-	0.78	-	0.78	pF	11,13
Z <sub>IO DQS</sub>	DQS_t, DQS_c Zpkg	45	85	45	85	Ω	1,2,5,10,11
T <sub>dIO DQS</sub>	DQS_t, DQS_c Pkg Delay	14	42	14	42	ps	1,3,5,10,11
L <sub>io DQS</sub>	DQS Lpkg	-	3.3	-	3.3	nH	11,12
C <sub>io DQS</sub>	DQS Cpkg	-	0.78	-	0.78	pF	11,13
DZ <sub>DIO DQS</sub>	Delta Zpkg DQS_t, DQS_c	-	10	-	10	Ω	1,2,5,7,10
D <sub>TdDIO DQS</sub>	Delta Delay DQS_t, DQS_c	-	5	-	5	pF	1,3,5,7,10
Z <sub>I CTRL</sub>	Input- CTRL pins Zpkg	50	90	50	90	Ω	1,2,5,9,10,11
T <sub>dI CTRL</sub>	Input- CTRL pins Pkg Delay	14	42	14	42	ps	1,3,5,9,10,11
L <sub>i CTRL</sub>	Input CTRL Lpkg	-	3.4	-	3.4	nH	11,12
C <sub>i CTRL</sub>	Input CTRL Cpkg	-	0.7	-	0.7	pF	11,13
Z <sub>I ADD CMD</sub>	Input- CMD ADD pins Zpkg	50	90	50	90	Ω	1,2,5,8,10,11
T <sub>dI ADD CMD</sub>	Input- CMD ADD pins Pkg Delay	14	45	14	45	ps	1,3,5,8,10,11
L <sub>i ADD CMD</sub>	Input CMD ADD Lpkg	-	3.6	-	3.6	nH	11,12
C <sub>i ADD CMD</sub>	Input CMD ADD Cpkg	-	0.74	-	0.74	pF	11,13
Z <sub>CK</sub>	CLK_t & CLK_c Zpkg	50	90	50	90	Ω	1,2,5,10,11
T <sub>dCK</sub>	CLK_t & CLK_c Pkg Delay	14	42	14	42	ps	1,3,5,10,11
L <sub>i CLK</sub>	Input CLK Lpkg	-	3.4	-	3.4	nH	11,12
C <sub>i CLK</sub>	Input CLK Cpkg	-	0.7	-	0.7	pF	11,13
DZ <sub>DCK</sub>	Delta Zpkg CLK_t & CLK_c	-	10	-	10	Ω	1,2,5,6,10
D <sub>TdCK</sub>	Delta Delay CLK_t & CLK_c	-	5	-	5	ps	1,3,5,6,10
Z <sub>OZQ</sub>	ZQ Zpkg	40	100	40	100	Ω	1,2,5,10,11
T <sub>dO ZQ</sub>	ZQ Delay	20	90	20	90	ps	1,3,5,10,11
Z <sub>O ALERT</sub>	ALERT Zpkg	40	100	40	100	Ω	1,2,5,10,11
T <sub>dO ALERT</sub>	ALERT Delay	20	55	20	55	ps	1,3,5,10,11

**NOTE :**  
1. This parameter is not subject to production test. It is verified by design and characterization. The package parasitic (L & C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side(not pin). Measurement procedure tbd

2. Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

$$Z_{pkg}(\text{total per pin}) = \sqrt{L_{pkg}/C_{pkg}}$$

3. Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

$$T_{dpgk}(\text{total per pin}) = \sqrt{L_{pkg} * C_{pkg}}$$

4. Z & Td IO applies to DQ, DM, DQS\_C, DQS\_T, TDQS\_T and TDQS\_C

5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

6. Absolute value of ZCK\_t-ZCK\_c for impedance(Z) or absolute value of TdCK\_t-TdCK\_c for delay(Td)

7. Absolute value of ZIO(DQS\_t)-ZIO(DQS\_c) for impedance(Z) or absolute value of TdIO(DQS\_t)-TdIO(DQS\_c) for delay(Td)

8. ZI & Td ADD CMD applies to A0-A13, ACT\_n BA0-BA1, BG0-BG1, RAS\_n, CAS\_n/A15, WE\_n/A14.

9. ZI & Td CTRL applies to ODT, CS\_n and CKE

10. This table applies to monolithic X4 and X8 devices.

11. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.

12. It is assumed that Lpkg can be approximated as Lpkg = Zo\*Td.

13. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo.

## 13. Electrical Characteristics & AC Timing

### 13.1 Reference Load for AC Timing and Output Slew Rate

Figure 21 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

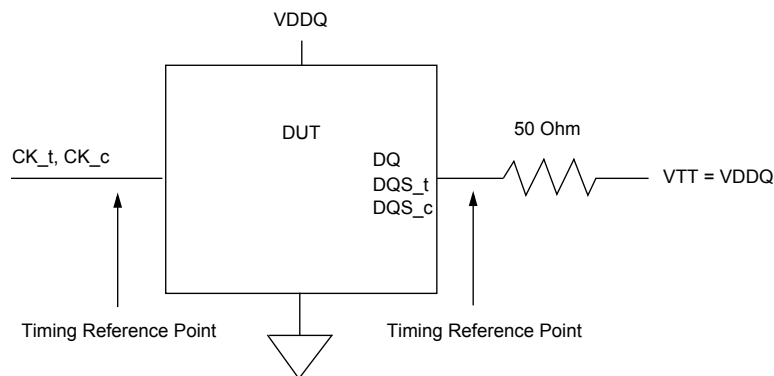


Figure 21. Reference Load for AC Timing and Output Slew Rate

### 13.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

[ Table 50 ] tREFI by device density

Parameter	Symbol	2Gb	4Gb	8Gb	16Gb	Units	
Average periodic refresh interval	tREFI	0°C ≤ TCASE ≤ 85°C	7.8	7.8	7.8	TBD	μs
		85°C < TCASE ≤ 95°C	3.9	3.9	3.9	TBD	μs

### 13.3 Timing Parameters by Speed Grade

[ Table 51 ] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2400

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>Clock Timing</b>											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	8	-	ns	22
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.938	<1.071	0.833	<0.938	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	125		107		94		83		ps	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	63		54		47		42		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	100		86		75		67		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min)$ $tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)$								ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps	
<b>Command and Address Timing</b>											
CAS_n to CAS_n command delay for same bank group	tCCD_L	5	-	5	-	6	-	6	-	nCK	34

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CAS <sub>n</sub> to CAS <sub>n</sub> command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)	-	Max(20nCK,23ns)	-	Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)	-	Max(16nCK,17ns)	-	Max(16nCK,15ns)	-	Max(16nCK,13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-		1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		1,34
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(4nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	ns	1,28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max(4nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	ns	2,29,34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max(4nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	ns	3,30,34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + pre-charge time	tDAL(min)	Programmed WR + roundup ( tRP / tCK(avg))								nCK	
<b>CS<sub>n</sub> to Command Address Latency</b>											
CS <sub>n</sub> to Command Address Latency	tCAL	3	-	4	-	4	-	5	-	nCK	
<b>DRAM Data Timing</b>											
DQS <sub>t</sub> ,DQS <sub>c</sub> to DQ skew, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	-	TBD	tCK(avg)/2	13,18
DQS <sub>t</sub> ,DQS <sub>c</sub> to DQ Skew deterministic, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	-	TBD	tCK(avg)/2	14,16,18
DQ output hold time from DQS <sub>t</sub> ,DQS <sub>c</sub>	tQH	TBD	-	TBD	-	TBD	-	TBD	-	tCK(avg)/2	13,17,18
DQ output hold time deterministic from DQS <sub>t</sub> , DQS <sub>c</sub>	tQH	TBD	-	TBD	-	TBD	-	TBD	-	UI	14,16,18
DQS <sub>t</sub> ,DQS <sub>c</sub> to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	TBD	-	TBD	-	TBD	-	TBD	UI	13,19
DQ output hold time total from DQS <sub>t</sub> , DQS <sub>c</sub> ; DBI enabled	tQH	TBD	-	TBD	-	TBD	-	TBD	-	UI	13,19



Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQ to DQ offset , per group, per access referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	UI	15,16
<b>Data Strobe Timing</b>											
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE	0.9	TBD	0.9	TBD	0.9	TBD	0.9	TBD	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	tCK	
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-300	150	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	150	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
<b>MPSM Timing</b>											
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD	-	TBD	-	TBD	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-	TBD	-		
<b>Calibration Timing</b>											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
<b>Reset/Self Refresh Timing</b>											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-	max (5nCK, tRFC(min)+10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-		

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PARR	max(5nCK, 10ns) + PL	-	max(5nCK, 10ns) + PL	-	max(5nCK, 10ns) + PL	-	max(5nCK, 10ns) + PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
<b>Power Down Timing</b>											
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-		
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
<b>PDA Timing</b>											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)		max(16nCK, 10ns)		max(16nCK, 10ns)		max(16nCK, 10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD			
<b>ODT Timing</b>											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
<b>Write Leveling Timing</b>											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE									ns	
<b>CA Parity Timing</b>											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL		

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Delay from errant command to ALERT_n assertion	tPAR_ALER_T_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALER_T_PW	48	96	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER_T_RSP	-	43	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		4		5		nCK	
<b>CRC Error Reporting</b>											
CRC error to ALERT_n latency	tCRC_ALER_T	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALER_T_PW	6	10	6	10	6	10	6	10	nCK	
<b>tREFI</b>											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34

**NOTE :**

1. Start of internal write transaction is defined as follows :
  - For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
  - For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
  - For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports  $t_{nPARAM}[nCK]=RU\{t_{PARAM}[ns]/t_{CK}(avg)[ns]\}$ , which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR\_CRC\_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR\_S\_CRC\_DM is used in place of tWTR\_S.
11. When CRC and DM are both enabled tWTR\_L\_CRC\_DM is used in place of tWTR\_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual  $t_{jit}(per)_{total}$  of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS\_t - DQS\_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR\_CRC\_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR\_S\_CRC\_DM is used in place of tWTR\_S.
30. When CRC and DM are both enabled tWTR\_L\_CRC\_DM is used in place of tWTR\_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification ( Low pulse width ).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification ( HIGH pulse width ).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from  $t_{CK}(avg)_{min}$  to  $t_{CK}(avg)_{max}$  at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.  
 $UI=t_{CK}(avg)_{min}/2$

### 13.4 The DQ input receiver compliance mask for voltage and timing (see figure)

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

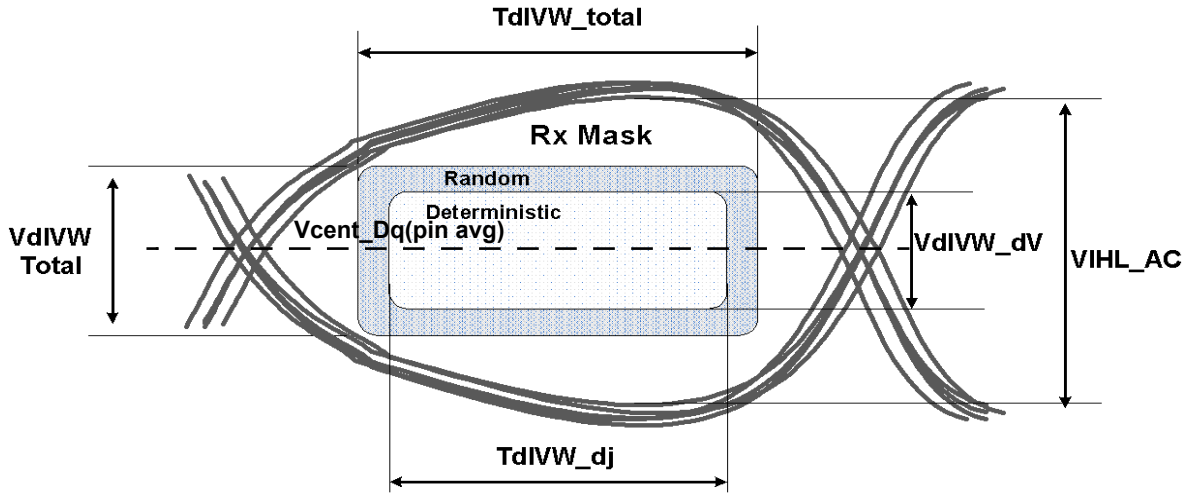


Figure 22. DQ Receiver(Rx) compliance mask

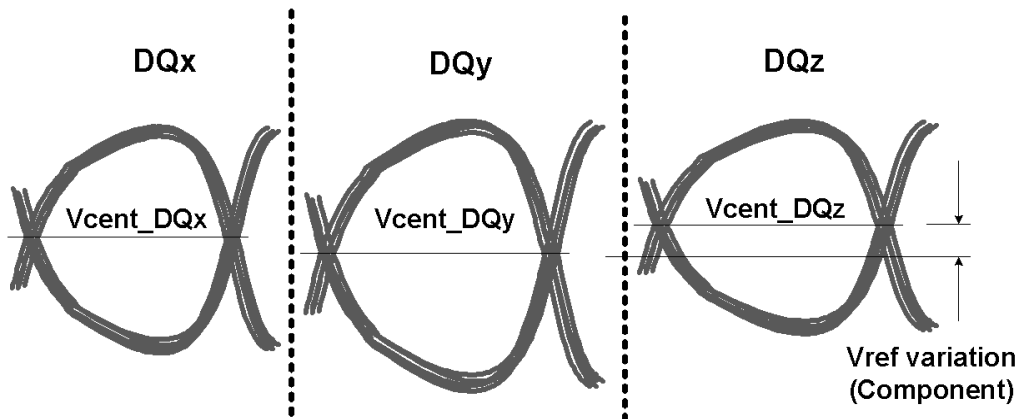
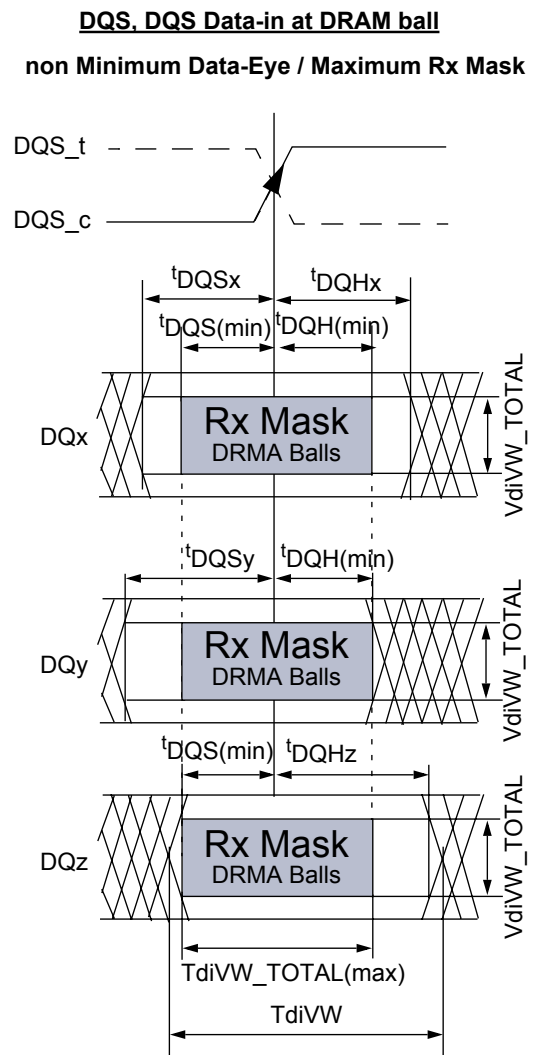
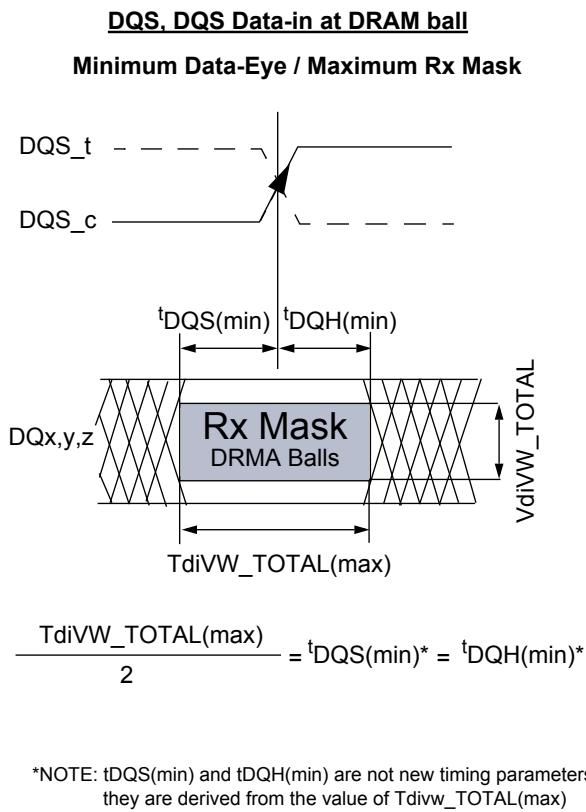


Figure 23. Across pin Vref DQ voltage variation

$V_{cent\_DQ}(\text{pin avg})$  is defined as the midpoint between the largest  $V_{ref\_DQ}$  voltage level and the smallest  $V_{ref\_DQ}$  voltage level across all DQ pins for a given DRAM component. Each DQ pin  $V_{ref}$  level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 22. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level  $V_{ref}$  will be set by the system to account for  $R_{on}$  and ODT settings.



**NOTE:** DQx represents an optimally centered input  
DQy represents earliest valid transiining input  
DQz represents latest valid transitioning input

Figure 24. DQ to DQS Timings at DRAM Balls

All of the timing terms in Figure 24 are measured at the VdiVW\_total voltage levels centered around Vcent\_DQ(pin avg) and are referenced to the DQS\_t/ DQS\_c center aligned to the DQ per pin.

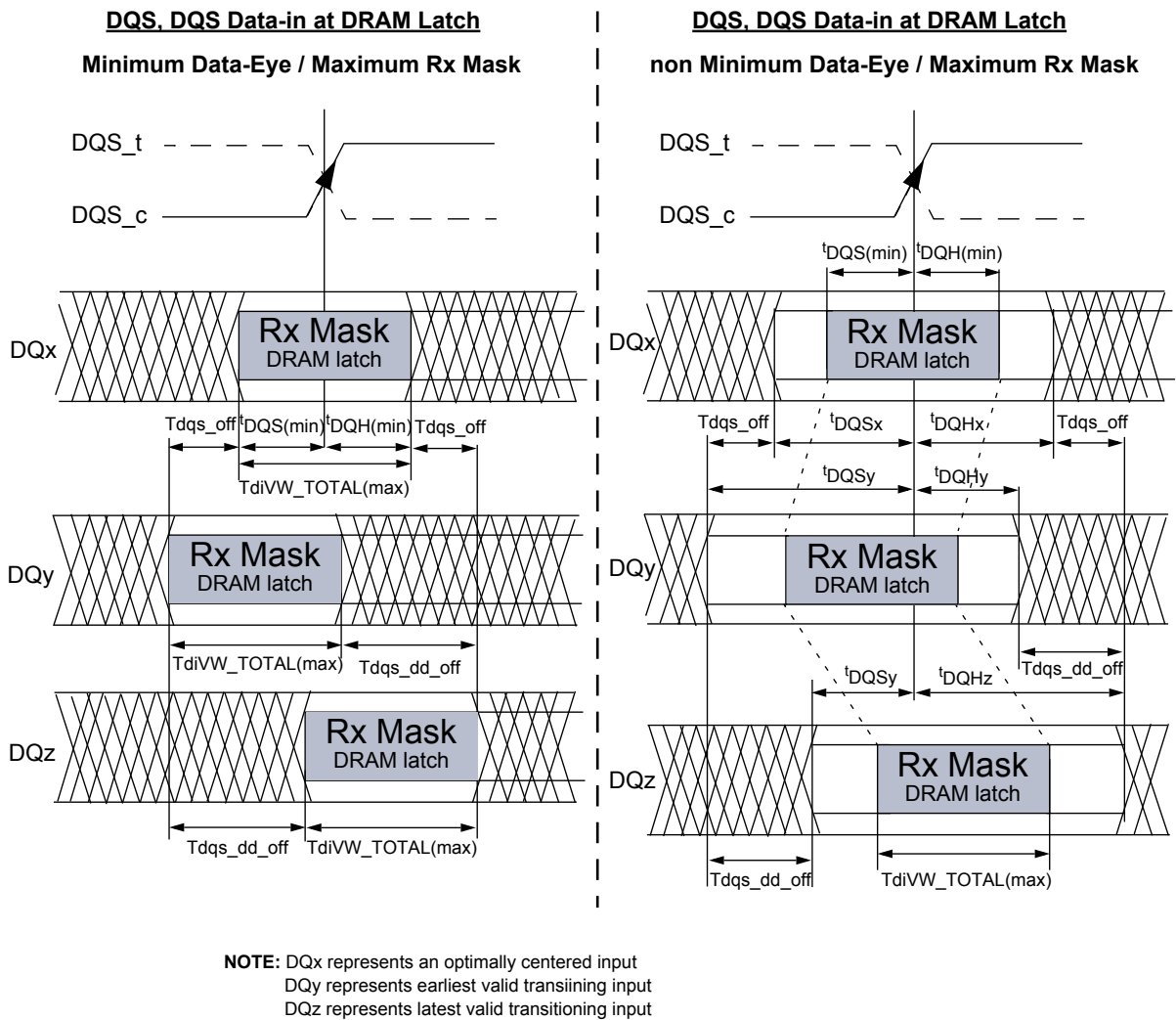
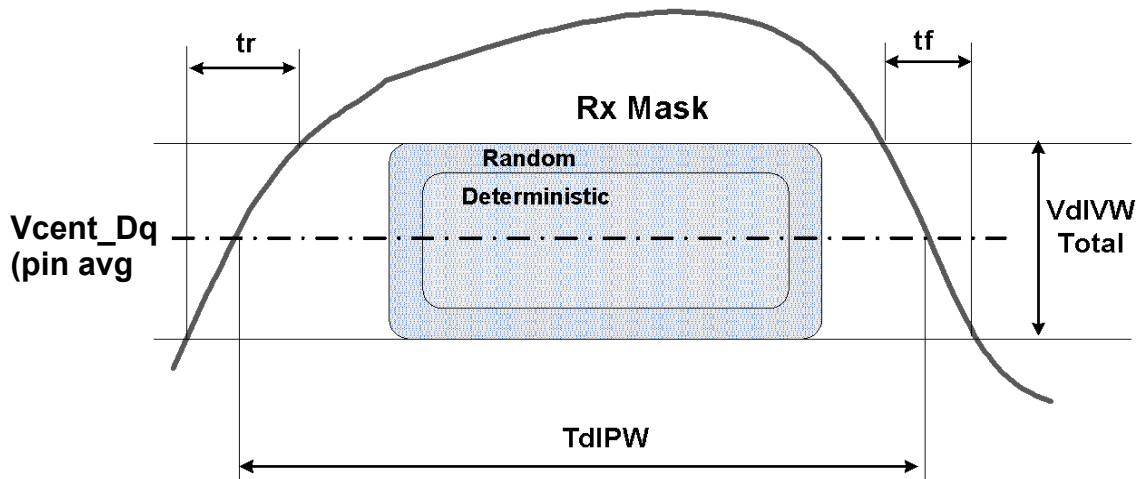


Figure 25. DQ to DQS Timings at DRAM latch

All of the timing terms in Figure 25 are measured at the  $V_{diVW\_total}$  voltage levels centered around  $V_{cent\_DQ}(pin\ avg)$  and are referenced to the  $DQS\_t/ DQS\_c$  center aligned. Typical view assumes DQx, DQy, and DQz edges are aligned at DRAM balls.



**NOTE :**

1.  $SRIN\_dIVW = V_{dIVW\_Total} / (t_r \text{ or } t_f)$ , signal must be monotonic within  $t_r$  and  $t_f$  range.

Figure 26. DQ  $T_{dIPW}$  and  $SRIN\_dIVW$  definition (for each input pulse)



[ Table 52 ] DRAM DQs In Receive Mode; \* UI=tck(avg)min/2

Symbol	Parameter	DDR4 - 1600/1866/2133		DDR4 - 2400		Unit	NOTE
		min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	136 (note12)	-	TBD	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	TBD	mV	1,5,13
TdIVW_total	Rx timing window total	-	0.2 (note12)	-	TBD	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	TBD	UI*	1,5,13
VIHL_AC	DQ AC input swing pk-pk	186	-	TBD	-	mV	7
TdIPW	DQ input pulse width	0.58	-	TBD	-	UI*	8
Tdqs_off	DQ to DQS Setup offset	-	TBD	-	TBD	UI*	9
Tdqh_off	DQ to DQS Hold offset	-	TBD	-	TBD	UI*	9
Tdqs_dd_off	DQ to DQ Setup offset	-	TBD	-	TBD	UI*	10
Tdqh_dd_off	DQ to DQ Hold offset	-	TBD	-	TBD	UI*	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	TBD	9	TBD	TBD	V/ns	11

- NOTE :**
1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent\_DQ(pin avg). The data Rx mask is applied per bit and should include voltage and temperature drift terms. The design specification is BER <1e-16 and how this varies for lower BER is tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).
  2. Rx mask voltage AC swing peak-peak requirement over TdIVW\_total with at least half of TdIVW\_total(max) above Vcent\_DQ(pin avg) and at least half of TdIVW\_total(max) below Vcent\_DQ(pin avg).
  3. Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels centered around Vcent\_DQ(pin avg).
  4. Defined over the DQ internal Vref range 1.
  5. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd
  6. Overshoot and Undershoot Specifications tbd.
  7. DQ input pulse signal swing into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent\_DQ(pin avg)
  8. DQ minimum input pulse width defined at the Vcent\_DQ(pin avg).
  9. DQ to DQS setup or hold offset defined within byte from DRAM ball to DRAM internal latch; <sup>t</sup>DQS and <sup>t</sup>DQH are the minimum DQ setup and hold per DQ pin; each is equal to one-half of TdIVW\_total(max).
  10. DQ to DQ setup or hold delta offset within byte. Defined as the static difference in Tdqs\_off(max) and Tdqs\_off( min) or Tdqh(max) – Tdqh(min) for a given component, from DRAM ball to DRAM internal latch.
  11. Input slew rate over VdIVW Mask centered at Vcent\_DQ(pin avg). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within tbd V/ns of each other.
  12. The total timing and voltage terms(tdIVW\_total & VdIVWtotal) are valid for any BER lower {lower fail rate} than the spec.
  13. VdIVW\_total - VdIVW\_dV and TdIVW\_total - TdIVW\_dj define the difference between random and deterministic fail mask. When VdIVW\_total - VdIVW\_dV = 0 and TdIVW\_total - TdIVW\_dj = 0, random error is assumed to be zero.

### 13.5 DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

[ Table 53 ] Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	x4	x8	x16	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask		V	V	
Data Bus Inversion		V	V	
TDQS		V		
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V	V	
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC	V	V	V	
CA Parity	V	V	V	
Control Gear Down Mode	V	V	V	
Programmable Preamble	V	V	V	
Maximum Power Down Mode	V	V		
Boundary Scan Mode			V	
Additive Latency	V	V		
3DS	V	V		

[ Table 54 ] Function Matrix (By Speed. V:Supported, Blank:Not supported)

Functions	1600/1866/2133 Mbps	2400 Mbps	NOTE
Write Leveling	V	V	
Temperature controlled Refresh	V	V	
Low Power Auto Self Refresh	V	V	
Fine Granularity Refresh	V	V	
Multi Purpose Register	V	V	
Data Mask	V	V	
Data Bus Inversion	V	V	
TDQS	V	V	
ZQ calibration	V	V	
DQ Vref Training	V	V	
Per DRAM Addressability	V	V	
Mode Register Readout	V	V	
CAL	V	V	
WRITE CRC	V	V	
CA Parity	V	V	
Control Gear Down Mode			
Programmable Preamble ( = 2tCK)		V	
Maximum Power Down Mode	V	V	
Boundary Scan Mode	V	V	
3DS	V	V	