18Mb Sync. Burst SRAM Specification

100TQFP with Pb / Pb-Free

(RoHS compliant)

SAMSUNG ELECTRONICS

Document Title

512Kx36 & 1Mx18-Bit Synchronous Burst SRAM

Revision History

Rev.No.	History	Draft Date	Remark
0.0	1. Initial draft	Mar. 23. 2004	Advance
0.1	1. Update the DC current spec(I_{CC}, I_{SB})	May. 21. 2004	Preliminary
0.2	1. Change the ISB,ISB1,ISB2 - ISB ; from 120mA to 170mA - ISB1 ; from 80mA to 150mA - ISB2 ; from 80mA to 130mA	Sep. 21. 2004	Preliminary
0.3	1. Remove the 1.8V Vdd voltage level	Oct. 18. 2004	Preliminary
0.4	1. Remove the -85 speed bin	Jan. 04. 2005	Preliminary
1.0	1. Finalize the datasheet	July 18. 2005	Final
2.0	1. Add the overshoot timing	Feb. 16. 2006	Final
3.0	1. Change ordering information	Apr. 16. 2006	Final

18Mb SB SRAM Ordering Information

Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
1Mx18	3.3/2.5	8.5	7.5	K7B161835B-P(Q)[1]C(I)[2]75	√
512Kx36	3.3/2.5	8.5	7.5	K7B163635B-P(Q)[1]C(I)[2]75	√

Note 1. P(Q) [Package type] : P-Pb Free, Q-Pb
2. C(I) [Operating Temperature] : C-Commercial, I-Industrial

512Kx36 & 1Mx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 2.5 or 3.3V +/- 5% Power Supply.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A (Lead and Lead free package)
- Operating in commeical and industrial temperature range.

GENERAL DESCRIPTION

The K7B163635B and K7B161835B are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS_1}$ high, $\overline{ADSP}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

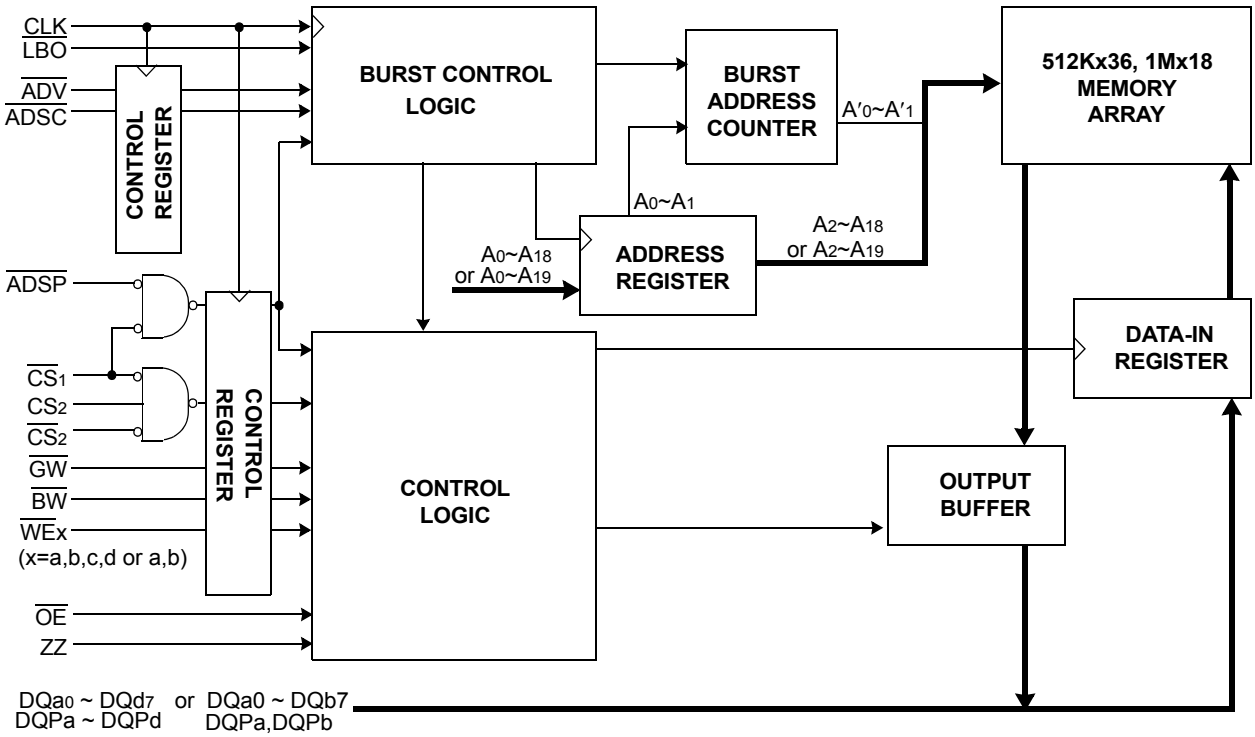
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B163635B and K7B161835B are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

FAST ACCESS TIMES

PARAMETER	Symbol	-75	Unit
Cycle Time	t_{CYC}	8.5	ns
Clock Access Time	t_{CD}	7.5	ns
Output Enable Access Time	t_{OE}	3.5	ns

LOGIC BLOCK DIAGRAM



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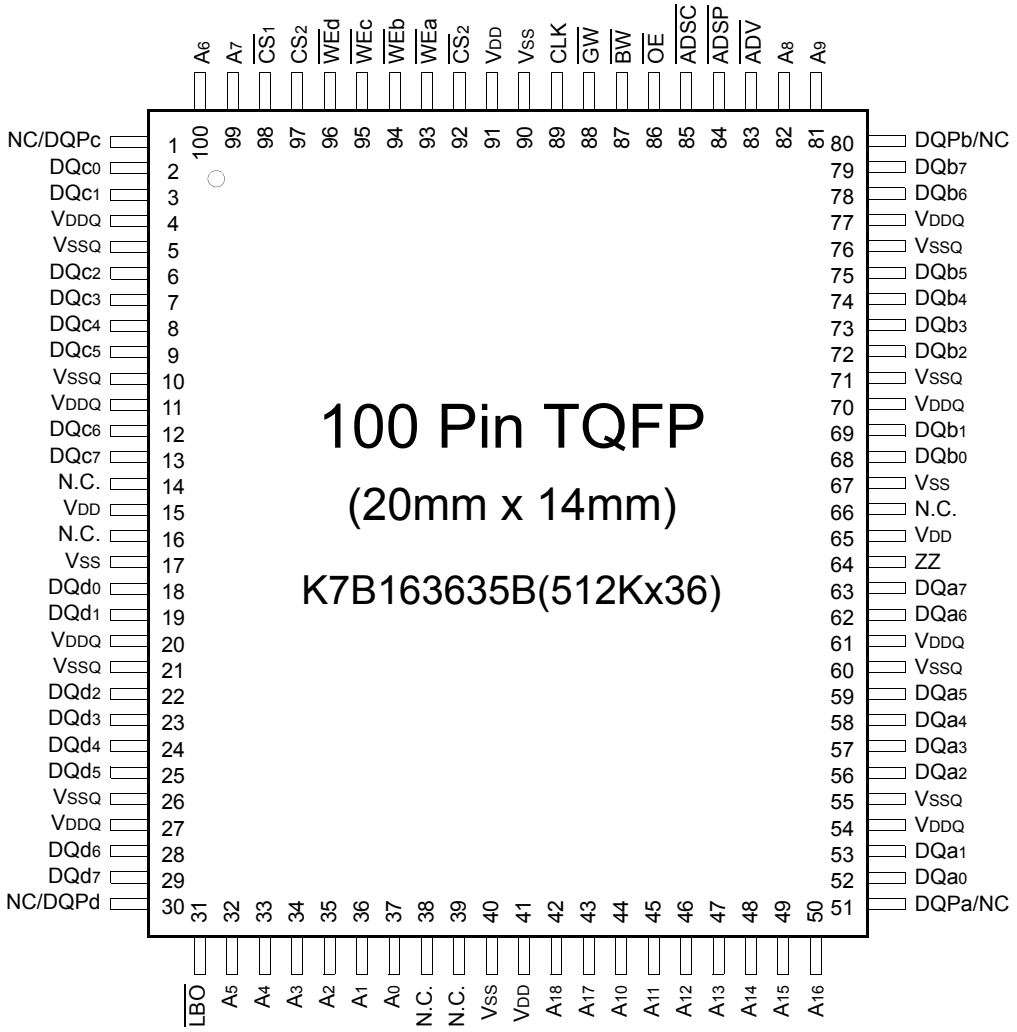
PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{18}	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50,81,82,99,100	V_{DD}	Power Supply(+3.3V)	15,41,65,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85	DQa_0~a_7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb_0~b_7		68,69,72,73,74,75,78,79
$\overline{CS_1}$	Chip Select	98	DQc_0~c_7		2,3,6,7,8,9,12,13
$\overline{CS_2}$	Chip Select	97	DQd_0~d_7		18,19,22,23,24,25,28,29
$\overline{CS_2}$	Chip Select	92	DQPa~P_d or NC		51,80,1,30
$\overline{WE}$x(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	V_{DDQ}	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{LBO}$	Burst Mode Control	31			

Notes : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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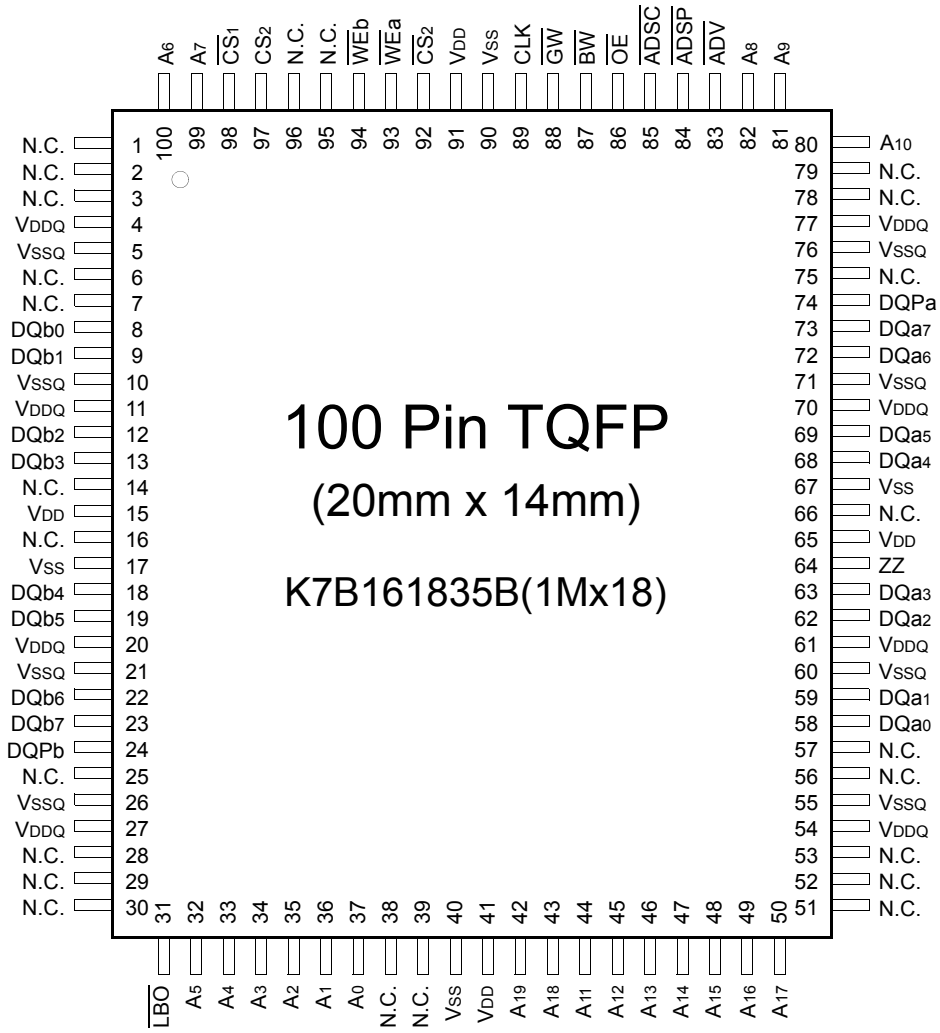
PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,39,51,52,53,56,57, 66,75,78,79,95,96
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS_1}$	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
$\overline{CS_2}$	Chip Select	97	DQPa, Pb		74,24
$\overline{CS_2}$	Chip Select	92			
$\overline{WE}$x(x=a,b)	Byte Write Inputs	93,94	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Notes : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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FUNCTION DESCRIPTION

The K7B163635B and K7B161835B are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c, and $\overline{WE}$d are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B163635B, a 512Kx36 organization, $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb, $\overline{WE}$c controls DQc0 ~ DQc7 and DQPc and $\overline{WE}$d controls DQd0 ~ DQd7 and DQPd.

$\overline{CS}_1$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
↓		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}		V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}		V_{IN}	-0.3 to V_{DD}+0.3	V
Voltage on I/O Pin Relative to V_{SS}		V_{IO}	-0.3 to V_{DDQ}+0.3	V
Power Dissipation		P_D	1.6	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_{OPR}	0 to 70	°C
	Industrial	T_{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

***Note :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \le T_A \le 70°C$)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD1}	2.375	2.5	2.625	V
	V_{DDQ1}	2.375	2.5	2.625	V
	V_{DD2}	3.135	3.3	3.465	V
	V_{DDQ2}	3.135	3.3	3.465	V
Ground	V_{SS}	0	0	0	V

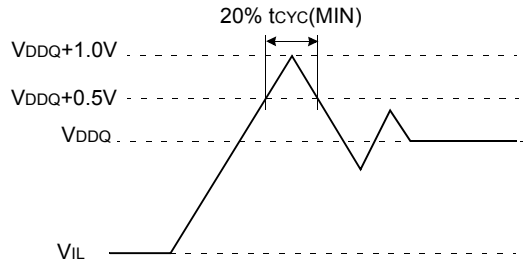
Notes: 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be $V_{DDQ} \le V_{DD}$

CAPACITANCE*(T_A=25°C, f=1MHz)

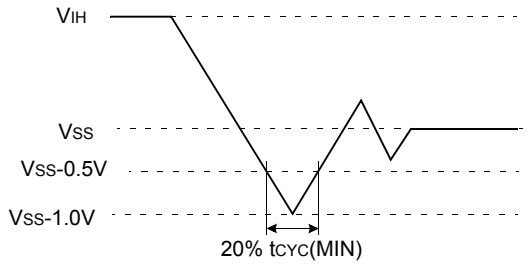
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	6	pF

***Note :** Sampled not 100% tested.

Overshoot Timing



Undershoot Timing



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DC ELECTRICAL CHARACTERISTICS

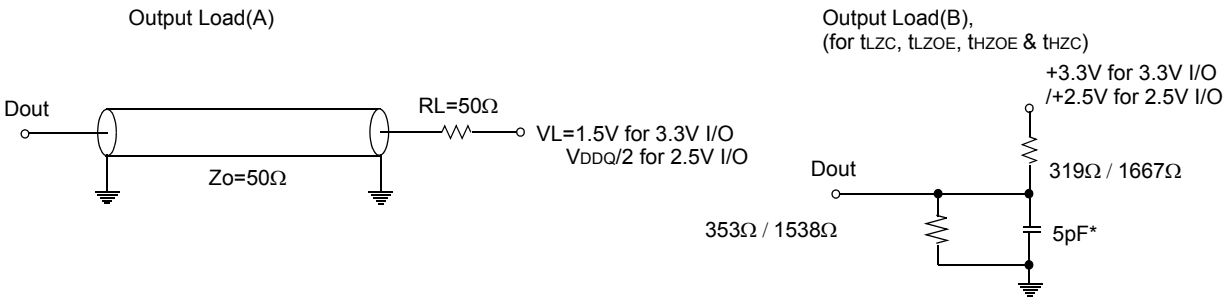
Parameter	Symbol	Test Conditions		Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	μA	
Output Leakage Current	I_{OL}	Output Disabled, V_{out}=V_{SS} to V_{DDQ}		-2	+2	μA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ≤V_{IL} , Cycle Time ≥ t_{CYC} Min	-75	-	250	mA	1,2
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-75	-	170	mA	
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	150	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	130	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL}=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.3**	V	3
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.3**	V	3

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. Data states are all zero.
4. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

* The above parameters are also guaranteed at industrial temperature range.



* Including Scope and Jig Capacitance

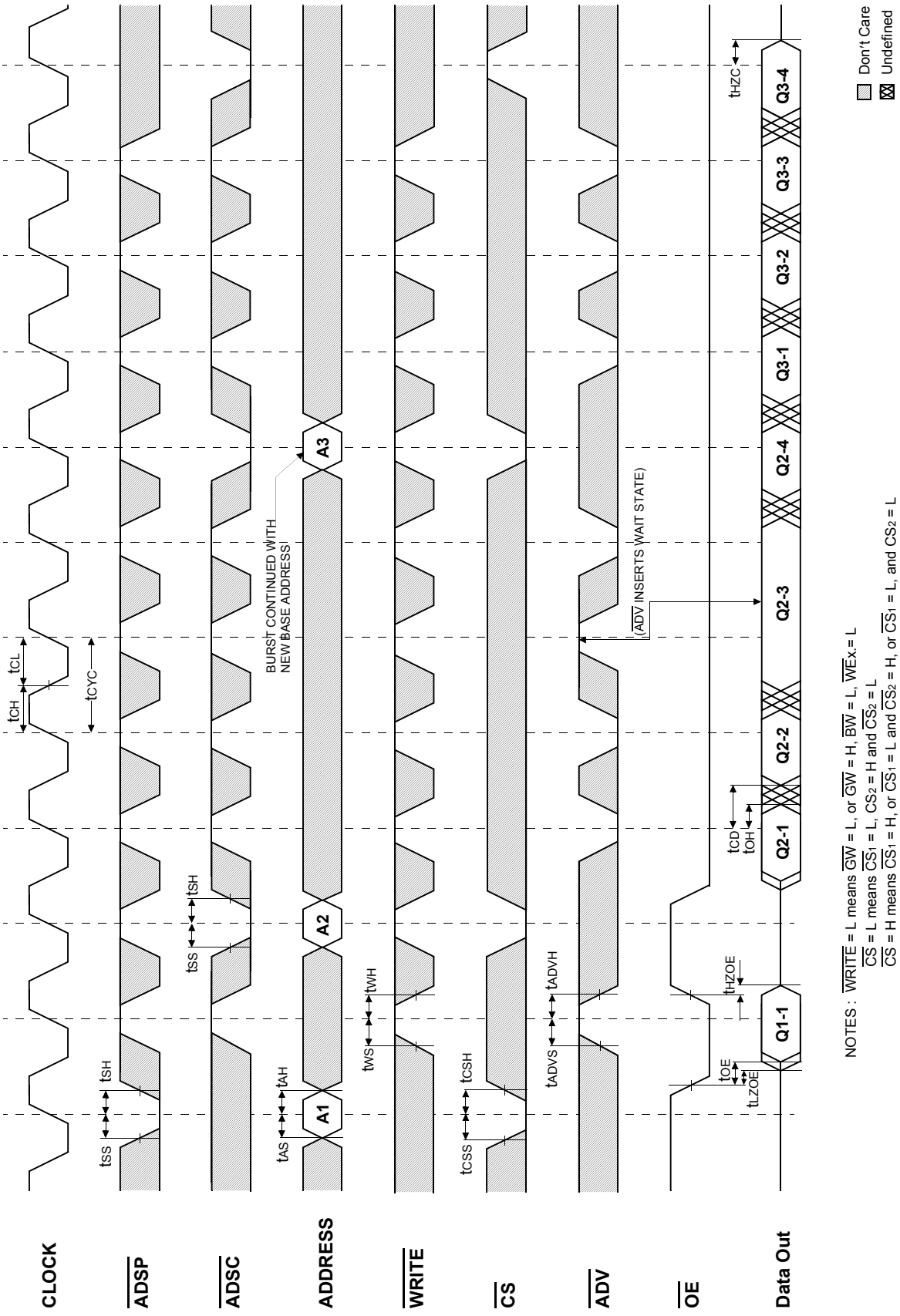
Fig. 1

AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-75		UNIT
		MIN	MAX	
Cycle Time	t_{CYC}	8.5	-	ns
Clock Access Time	t_{CD}	-	7.5	ns
Output Enable to Data Valid	t_{OE}	-	3.5	ns
Clock High to Output Low-Z	t_{LZC}	2.5	-	ns
Output Hold from Clock High	t_{OH}	2.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	3.5	ns
Clock High to Output High-Z	t_{HZC}	-	4.0	ns
Clock High Pulse Width	t_{CH}	2.5	-	ns
Clock Low Pulse Width	t_{CL}	2.5	-	ns
Address Setup to Clock High	t_{AS}	2.0	-	ns
Address Status Setup to Clock High	t_{SS}	2.0	-	ns
Data Setup to Clock High	t_{DS}	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	t_{WS}	2.0	-	ns
Address Advance Setup to Clock High	t_{ADVS}	2.0	-	ns
Chip Select Setup to Clock High	t_{CSS}	2.0	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	t_{WH}	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	cycle

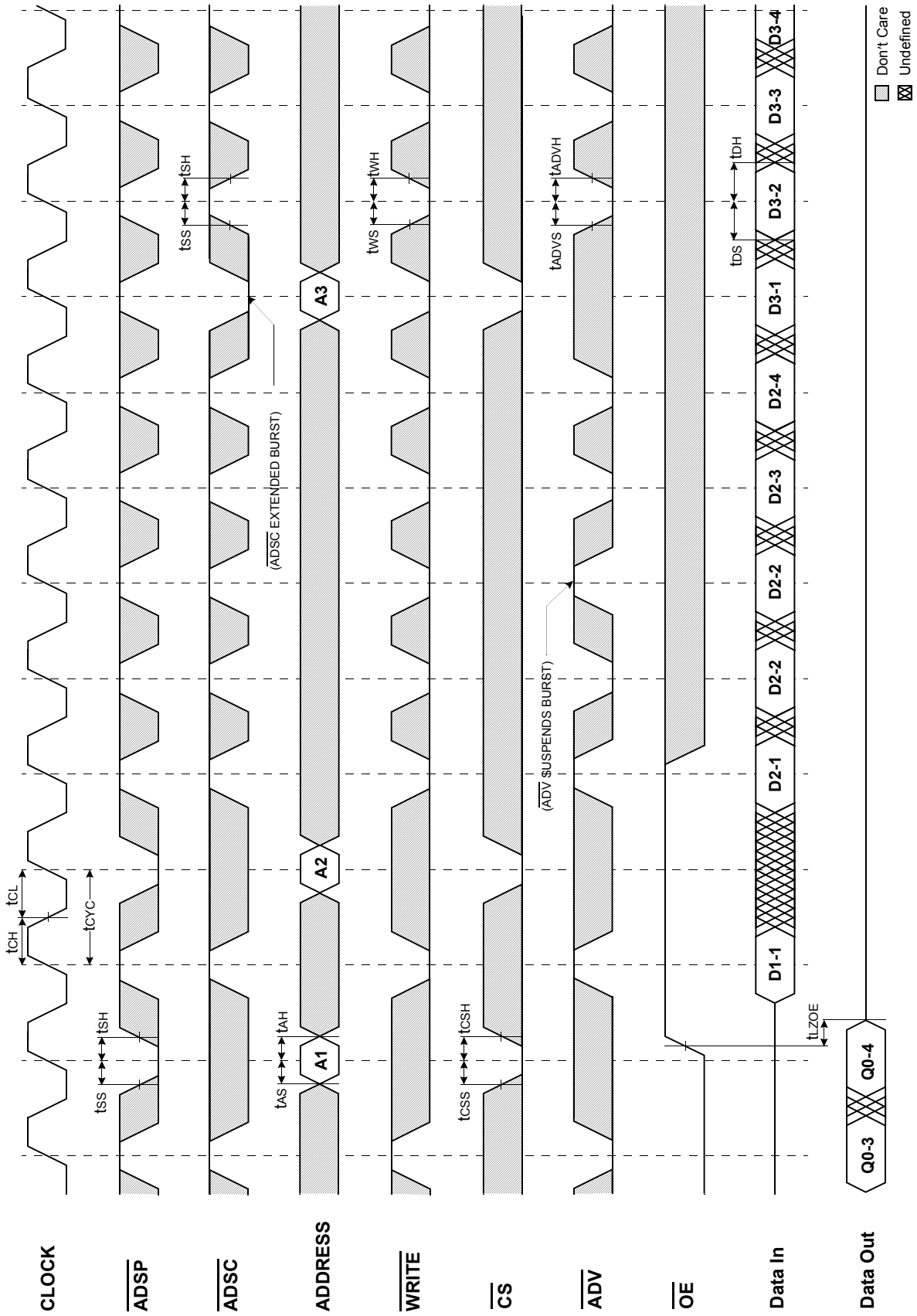
Notes : 1. The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
4. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE

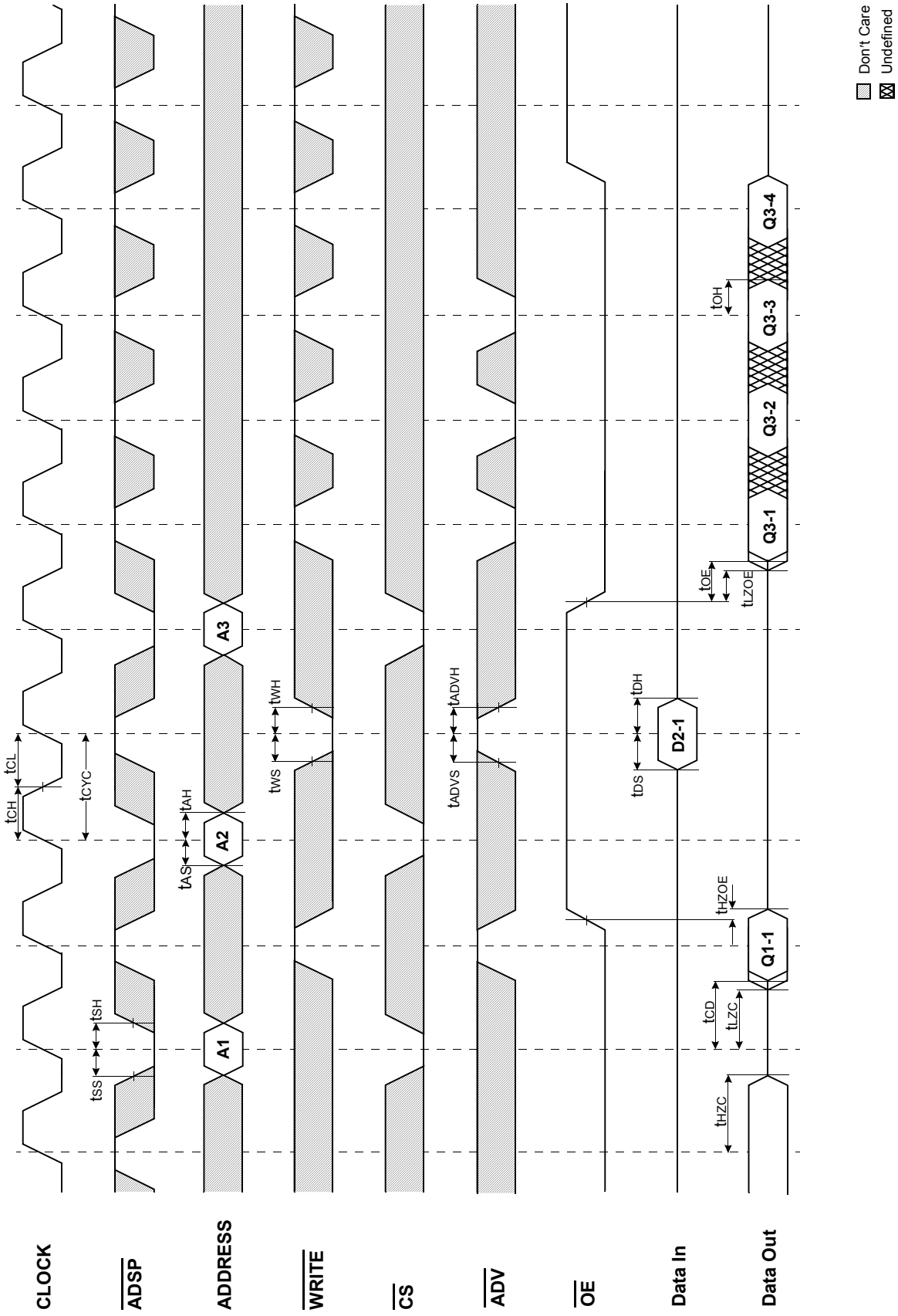


NOTES : WRITE = L means GW = L, or GW = H, BW = L, WEx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

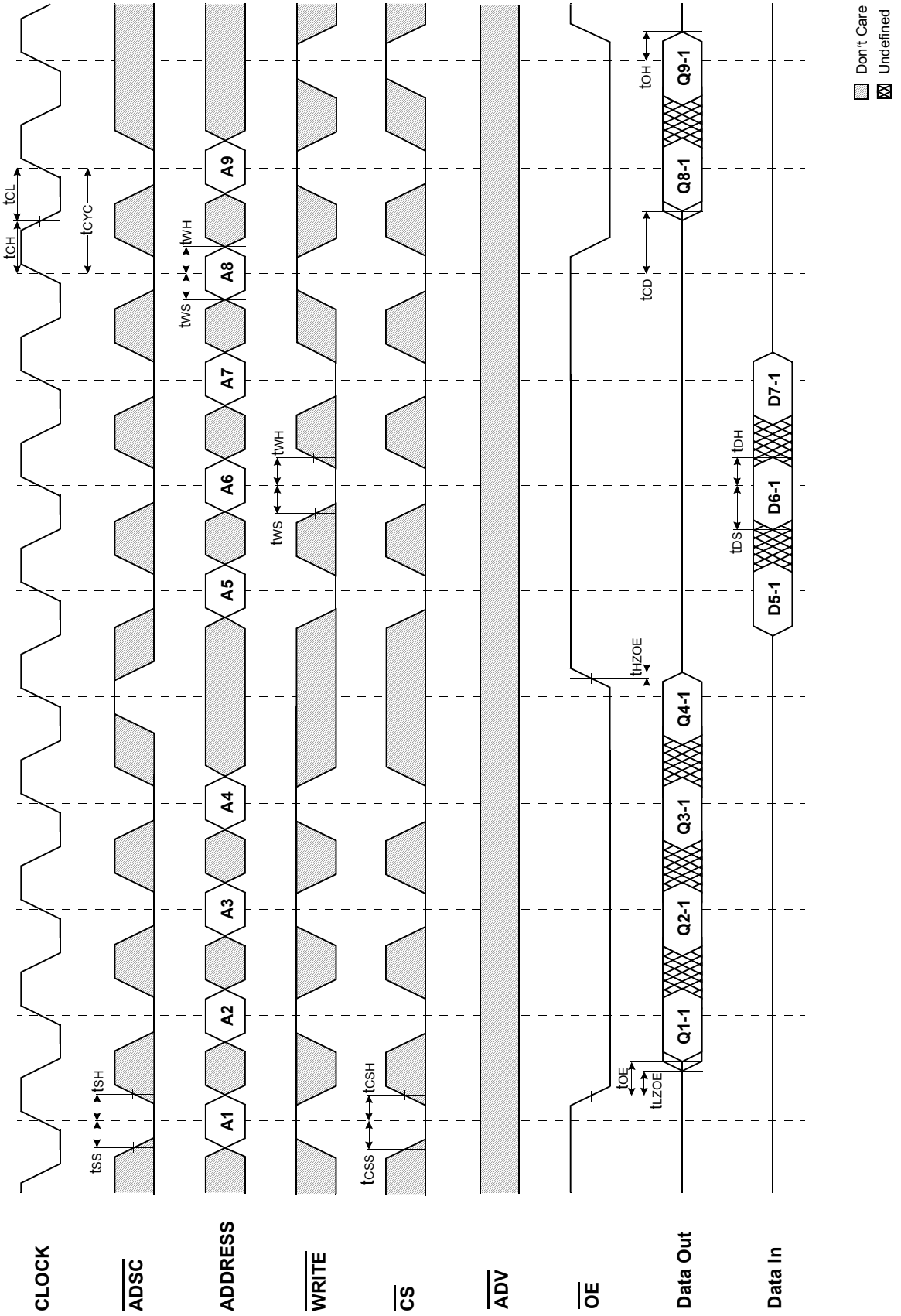
TIMING WAVEFORM OF WRTE CYCLE



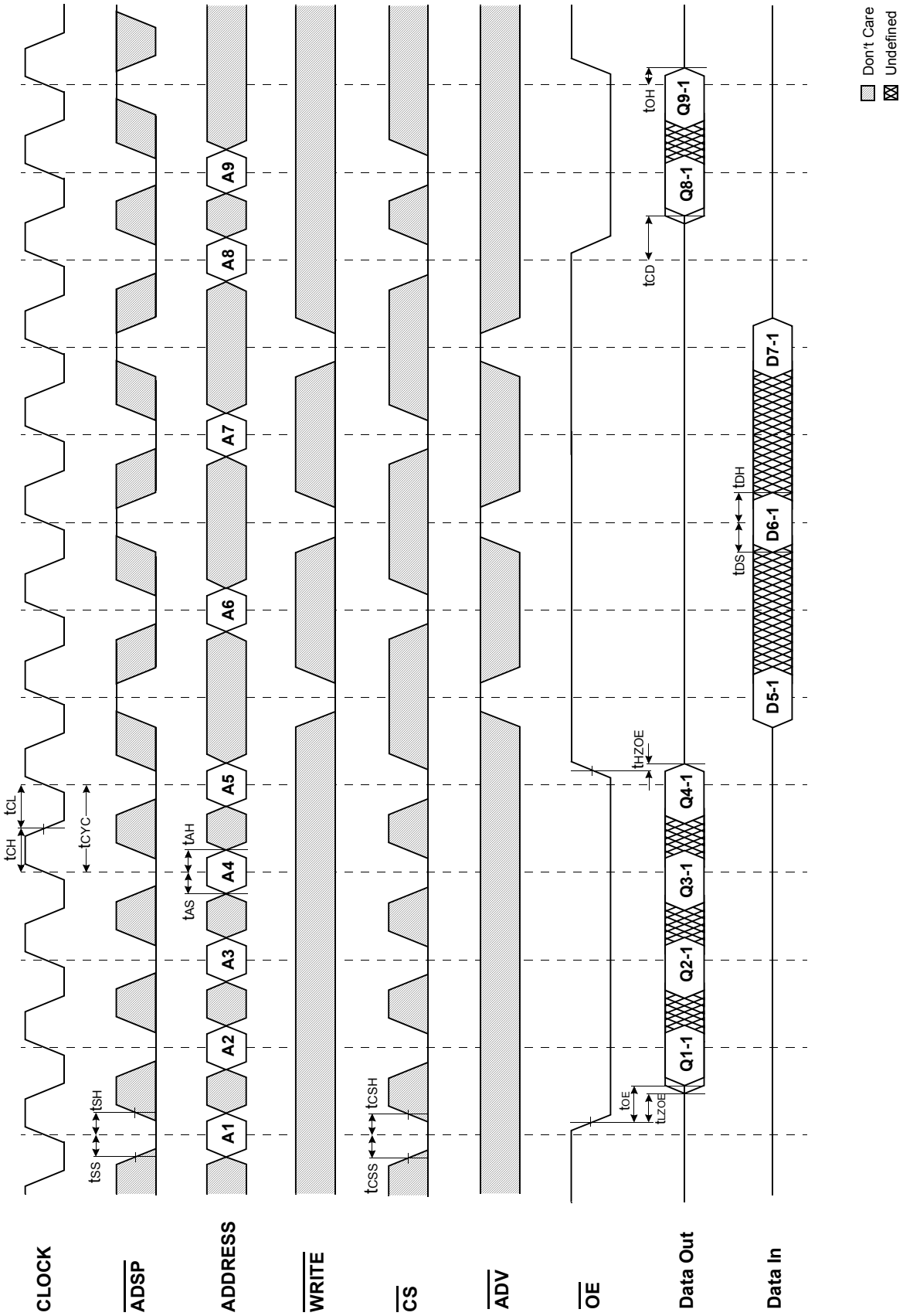
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



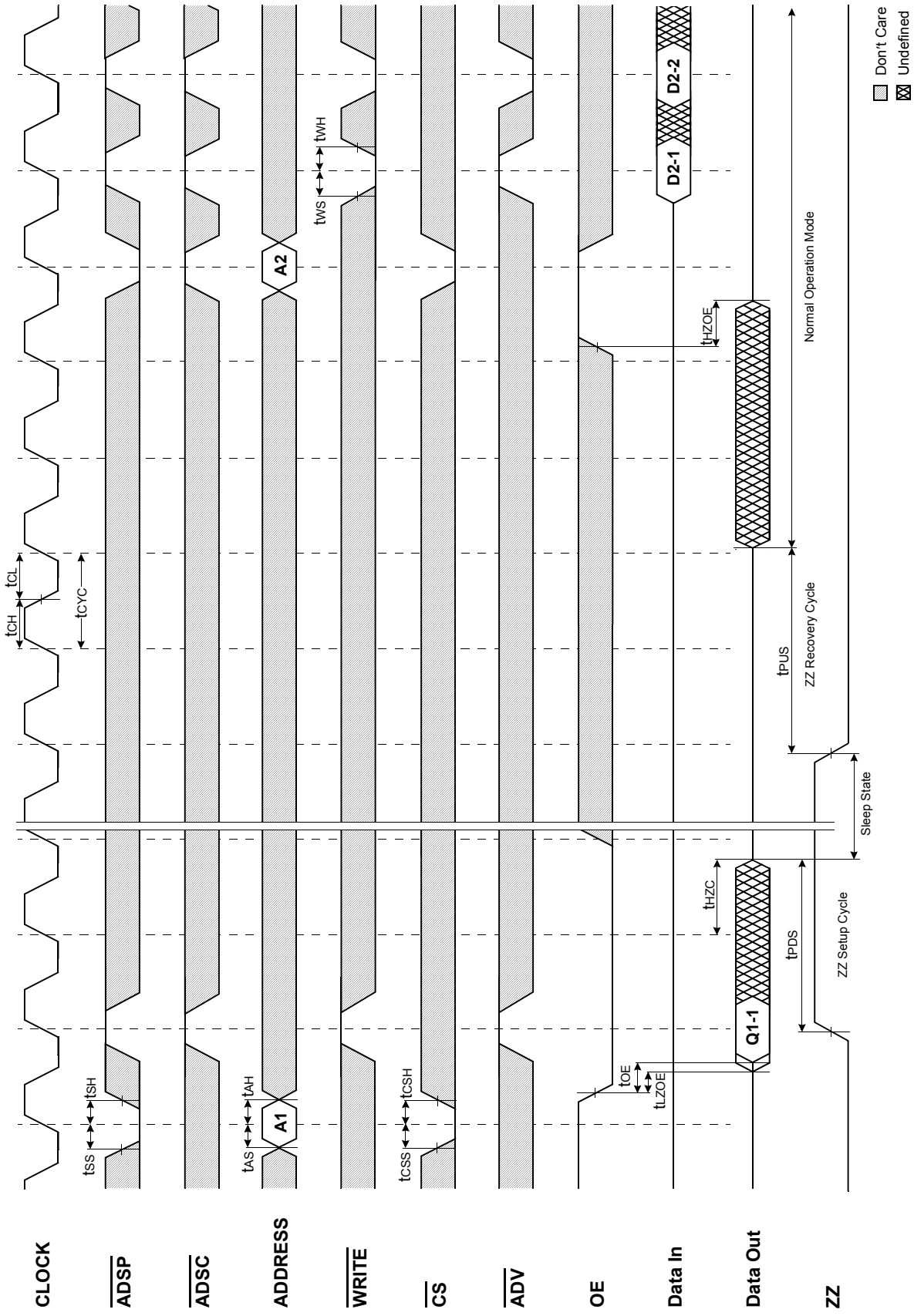
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



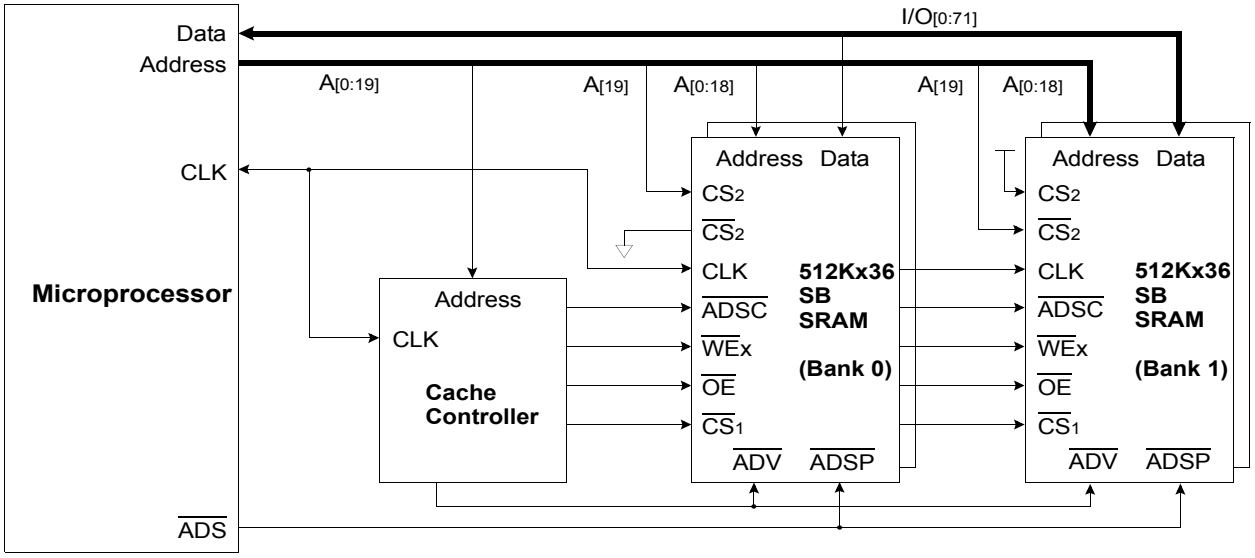
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

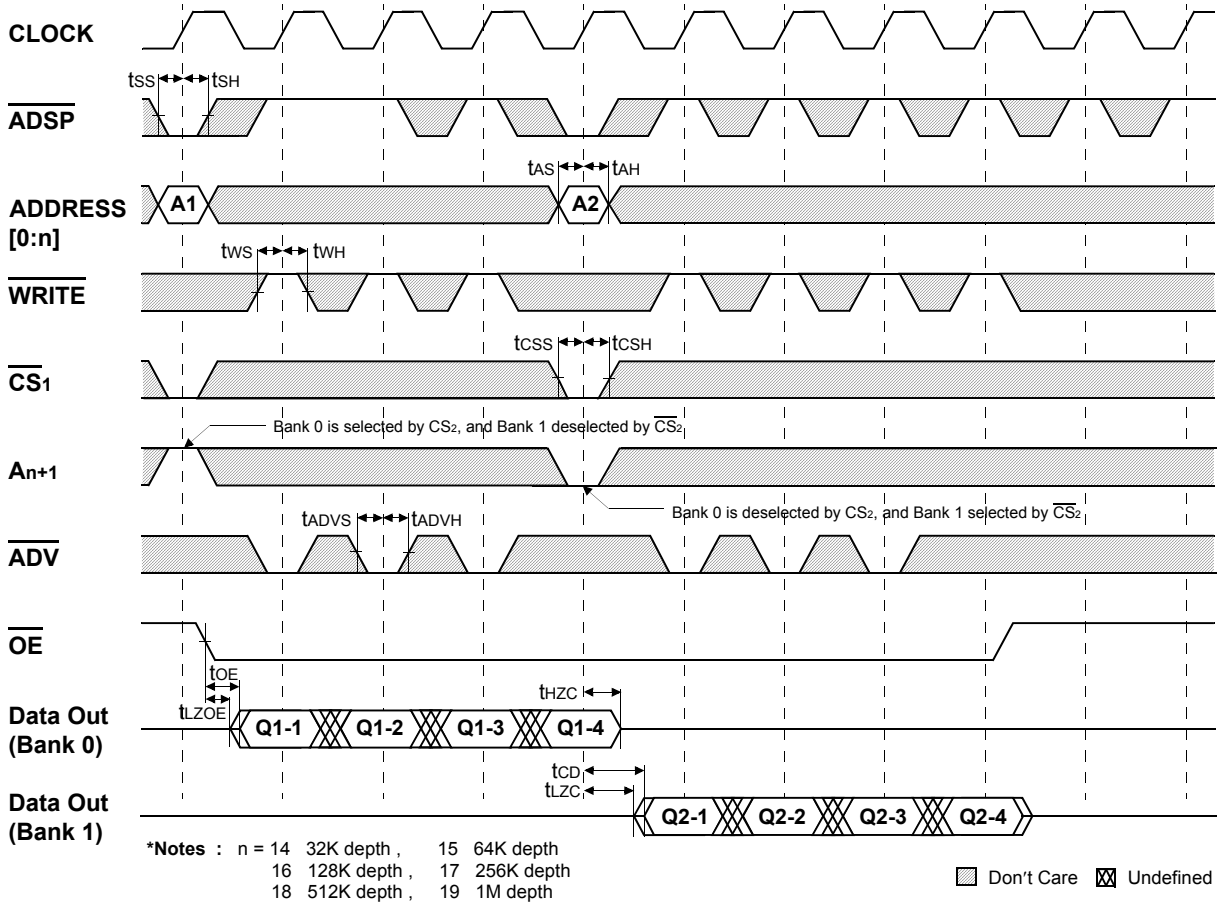
DEPTH EXPANSION

The Samsung 512Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)



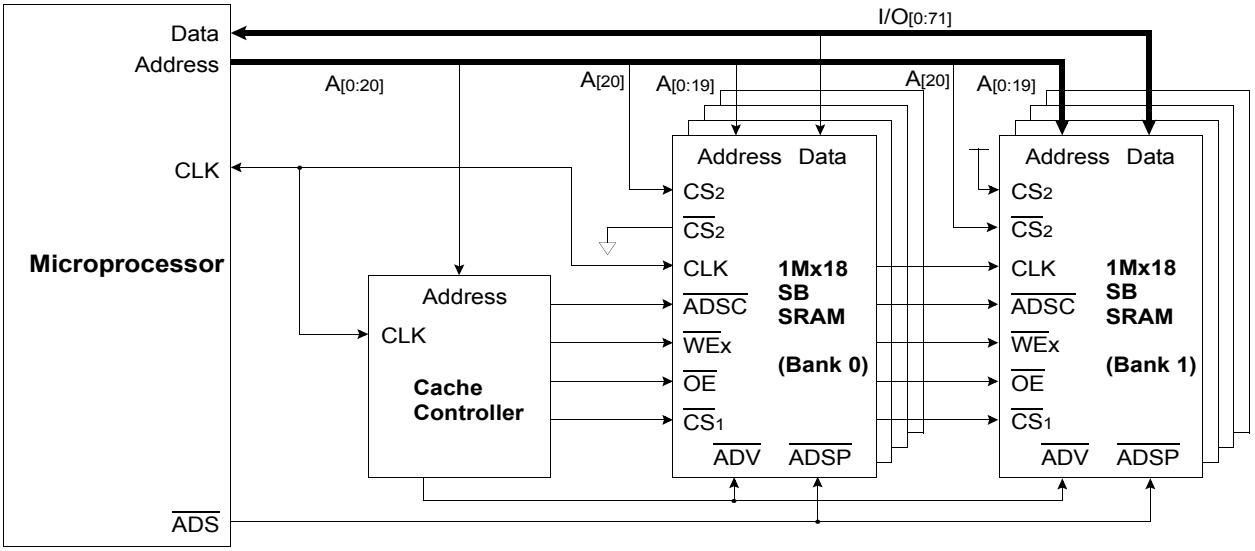
*Notes : n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

Don't Care Undefined

APPLICATION INFORMATION

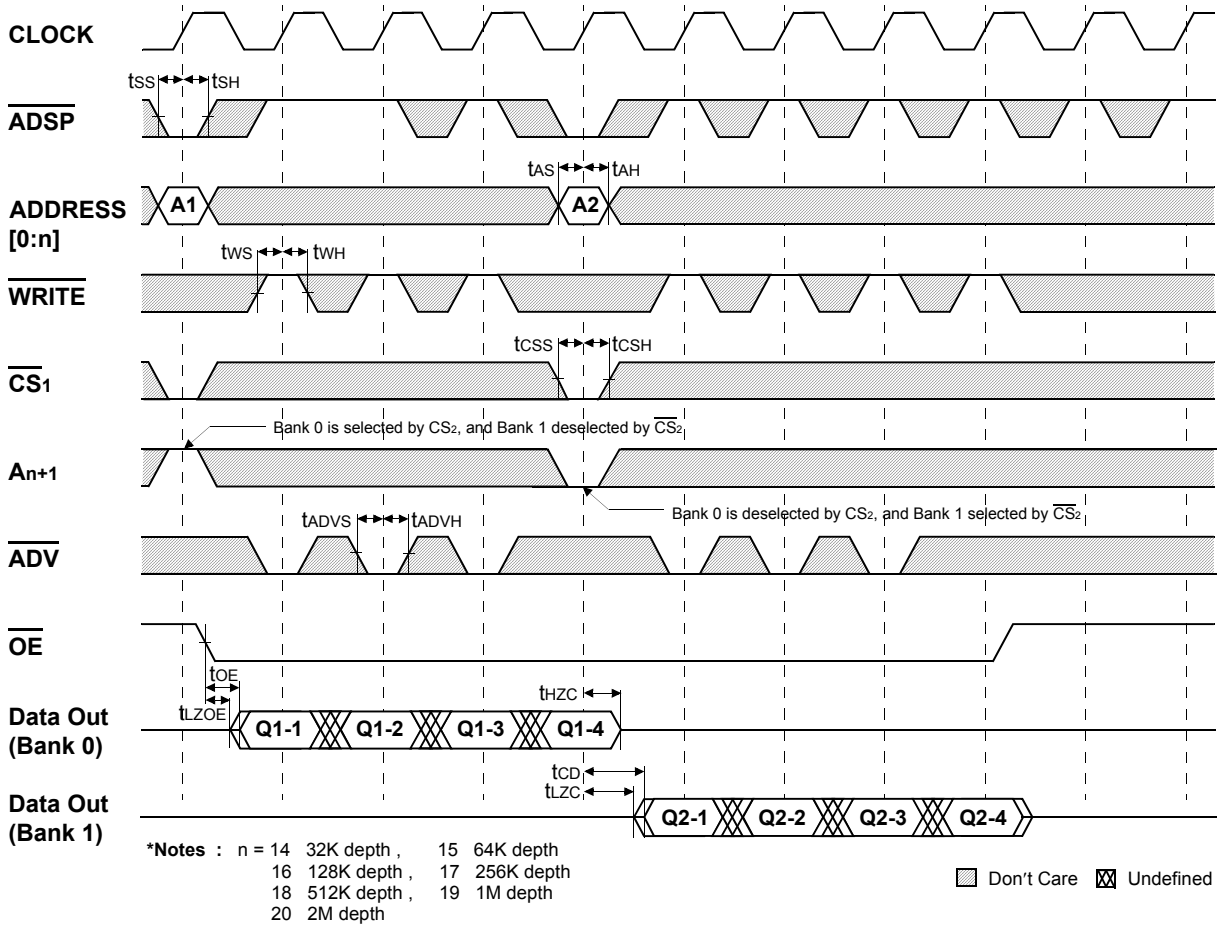
DEPTH EXPANSION

The Samsung 1Mx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)

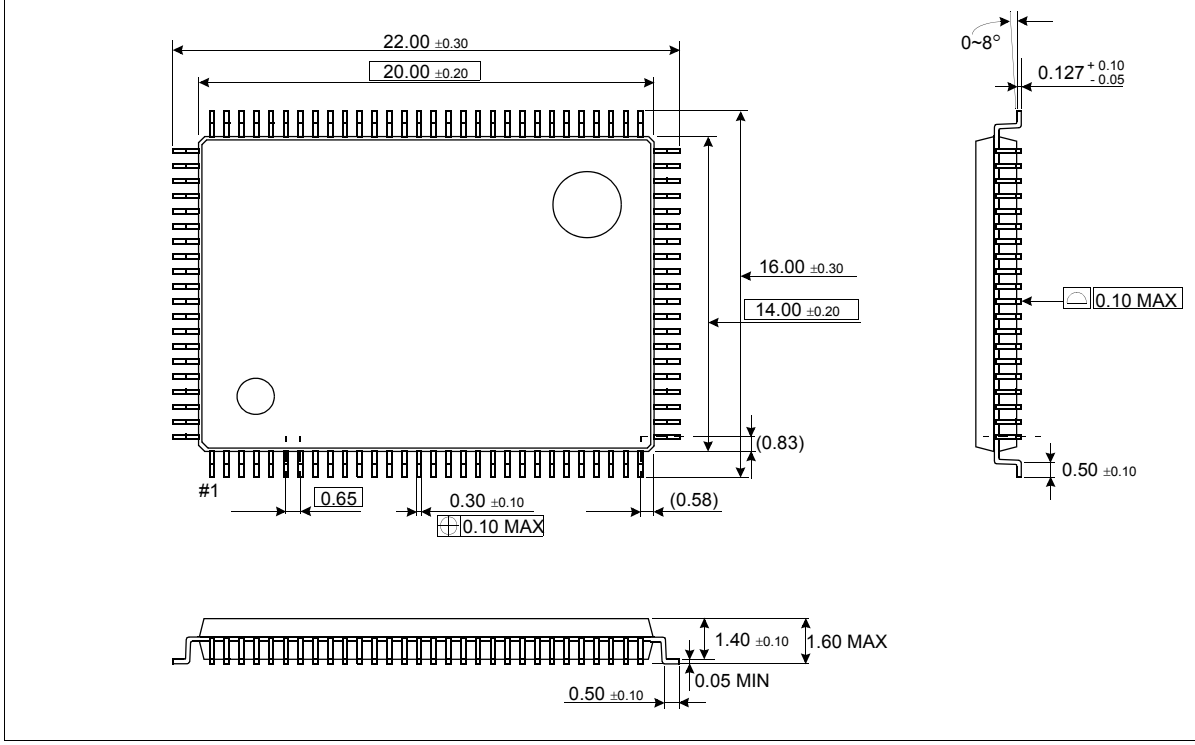


***Notes :** n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth
20 2M depth

PACKAGE DIMENSIONS

100-TQFP-1420A (Lead and Lead free package)

Units ; millimeters/Inches



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