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# LM317L

## 3-Terminal 0.1A Positive Adjustable Regulator

### Features

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Floating Operation for High-Voltage Applications

### Description

The LM317L is a 3-terminal, adjustable, positive-voltage regulator capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator requires only two external resistors to set the output voltage.

#### TO-92



1

1. Adj 2. Output 3. Input

#### 8-SOIC



1

1. Input 2.3.6.7. Output  
4. Adj 5.8. NC

### Ordering Information

| Part Number | Operating Temperature Range | Top Mark | Package | Packing Method |
|-------------|-----------------------------|----------|---------|----------------|
| LM317LM     | 0°C to +125°C               | LM317LM  | 8-SOIC  | Rail           |
| LM317LMX    | 0°C to +125°C               | LM317LM  | 8-SOIC  | Tape and Reel  |
| LM317LZ     | 0°C to +125°C               | LM317LZ  | TO-92   | Bulk           |
| LM317LZX    | 0°C to +125°C               | LM317LZ  | TO-92   | Tape and Reel  |

## Block Diagram

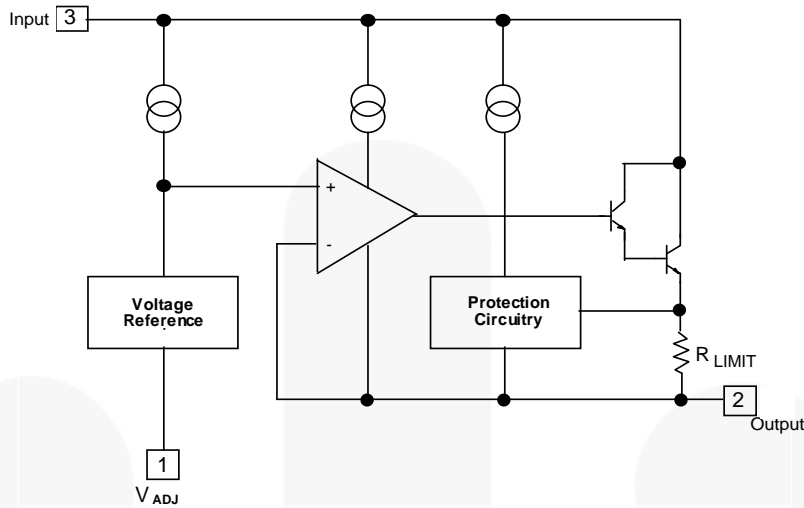


Figure 1. Block Diagram

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

| Symbol      | Parameter                            | Value              | Unit             |
|-------------|--------------------------------------|--------------------|------------------|
| $V_I - V_O$ | Input-Output Voltage Differential    | 40                 | V                |
| $P_D$       | Power Dissipation                    | Internally limited | W                |
| $T_J$       | Operating Junction Temperature Range | 0 ~ +125           | $^\circ\text{C}$ |
| $T_{STG}$   | Storage Temperature Range            | -65 ~ +125         | $^\circ\text{C}$ |

## Electrical Characteristics

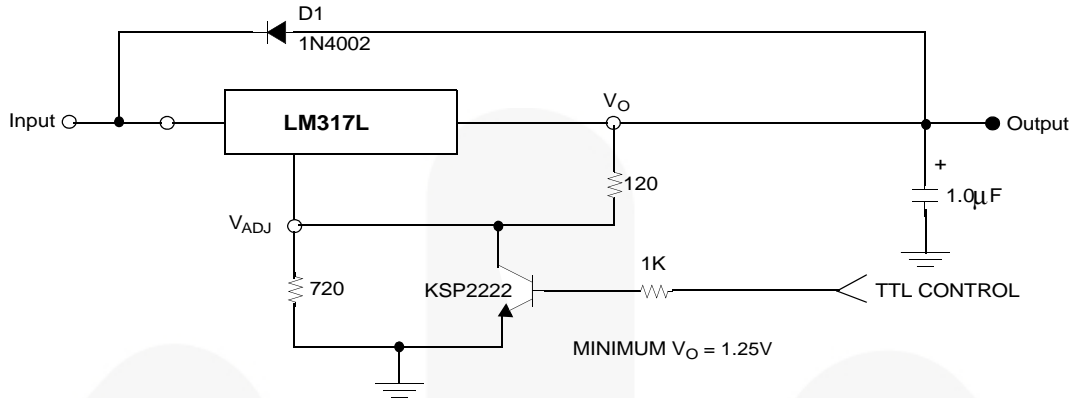
$V_I - V_O = 5\text{ V}$ ,  $I_O = 40\text{ mA}$ ,  $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ ,  $P_{D\text{MAX}} = 625\text{ mW}$ , unless otherwise specified.

| Symbol                  | Parameter                                   | Conditions  | Min. | Typ.  | Max. | Unit          |
|-------------------------|---|---|------|-------|------|---------------|
| $R_{\text{LINE}}$       | Line Regulation <sup>(1)</sup>              | $T_A = +25^\circ\text{C}$ , $3\text{ V} \leq V_I - V_O \leq 40\text{ V}$  |      | 0.01  | 0.04 | % / V         |
|                         |   | $3\text{ V} \leq V_I - V_O \leq 40\text{ V}$  |      | 0.02  | 0.07 | % / V         |
| $R_{\text{LOAD}}$       | Load Regulation <sup>(1)</sup>              | $T_A = +25^\circ\text{C}$ , $10\text{ mA} \leq I_O \leq 100\text{ mA}$ , $V_O \leq 5\text{ V}$                            |      | 5     | 25   | mV            |
|                         |   | $T_A = +25^\circ\text{C}$ , $10\text{ mA} \leq I_O \leq 100\text{ mA}$ , $V_O \geq 5\text{ V}$                            |      | 0.1   | 0.5  | % / $V_O$     |
|                         |   | $10\text{ mA} \leq I_O \leq 100\text{ mA}$ , $V_O \leq 5\text{ V}$  |      | 20    | 70   | mV            |
|                         |   | $10\text{ mA} \leq I_O \leq 100\text{ mA}$ , $V_O \geq 5\text{ V}$  |      | 0.3   | 1.5  | % / $V_O$     |
| $I_{\text{ADJ}}$        | Adjustment Pin Current                      |   |      | 50    | 100  | $\mu\text{A}$ |
| $\Delta I_{\text{ADJ}}$ | Adjustment Pin Current Change               | $3\text{ V} \leq V_I - V_O \leq 40\text{ V}$ ,<br>$10\text{ mA} \leq I_O \leq 100\text{ mA}$ ,<br>$P_D < P_{D\text{MAX}}$ |      | 0.2   | 5    | $\mu\text{A}$ |
| $V_{\text{REF}}$        | Reference Voltage                           | $3\text{ V} < V_I - V_O < 40\text{ V}$ ,<br>$10\text{ mA} \leq I_O \leq 100\text{ mA}$ ,<br>$P_D \leq P_{D\text{MAX}}$    | 1.20 | 1.25  | 1.30 | V             |
| $ST_T$                  | Temperature Stability                       |   |      | 0.7   |      | %             |
| $I_{\text{L(MIN)}}$     | Minimum Load Current to Maintain Regulation | $V_I - V_O = 40\text{ V}$   |      | 3.5   | 10   | mA            |
| $I_{\text{O(MAX)}}$     | Maximum Output Current                      | $V_I - V_O \leq 15\text{ V}$ , $P_D < P_{D\text{MAX}}$  | 100  | 200   |      | mA            |
|                         |   | $T_A = +25^\circ\text{C}$ ,<br>$V_I - V_O \leq 40\text{ V}$ , $P_D < P_{D\text{MAX}}$                                     | 25   | 50    |      | mA            |
| $e_N$                   | RMS Noise, % of $V_{\text{OUT}}$            | $T_A = +25^\circ\text{C}$ , $10\text{ Hz} < f < 10\text{ kHz}$  |      | 0.003 |      | % / $V_O$     |
| RR                      | Ripple Rejection                            | $V_O = 10\text{ V}$ , $f = 120\text{ Hz}$ ,<br>without $C_{\text{ADJ}}$   |      | 65    |      | dB            |
|                         |   | $V_O = 10\text{ V}$ , $f = 120\text{ Hz}$ ,<br>$C_{\text{ADJ}} = 10\text{ }\mu\text{F}$                                   | 66   | 80    |      | dB            |
| ST                      | Long-Term Stability                         | $T_J = +125^\circ\text{C}$ , 1000 Hours   |      | 0.3   |      | %             |

### Notes:

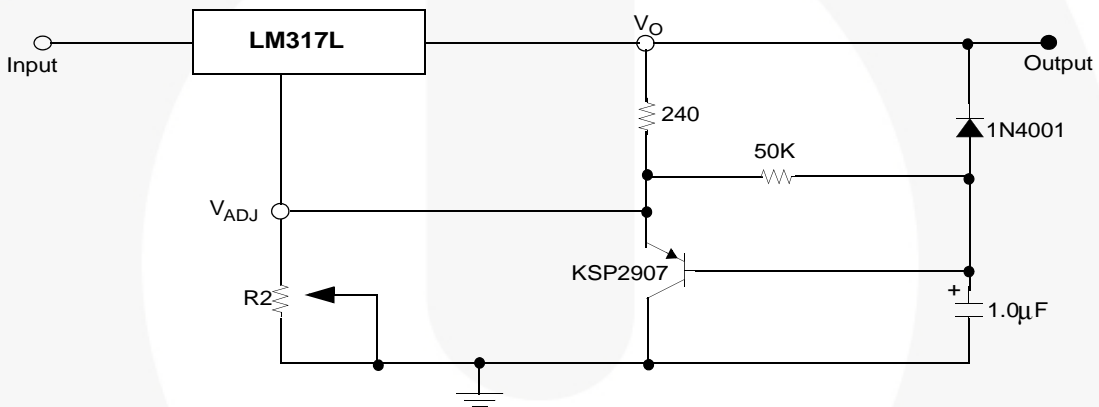
1. Load and Line regulation are specified at constant junction temperature. Change in  $V_O$  due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## Typical Application

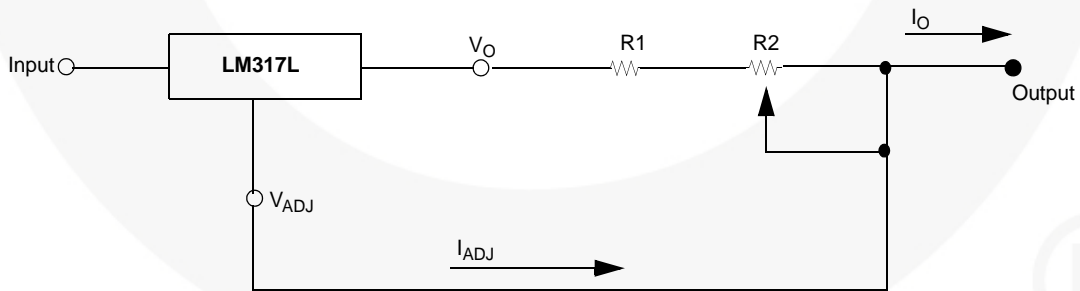


**Figure 2. 5V Electronic Shutdown Regulator**

D1 protects the device during an input short circuit.



**Figure 3. Slow Turn-On Regulator**



**Figure 4. Current Regulator**

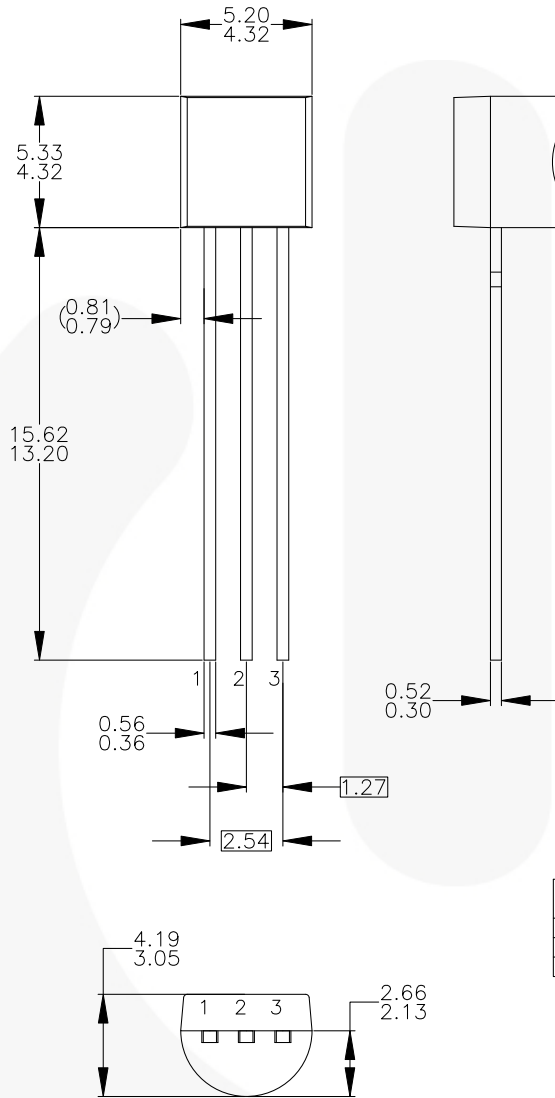
$$I_{O\text{MAX}} = \left( \frac{V_{\text{REF}}}{R1} \right) + I_{\text{ADJ}} @ \frac{1.25\text{V}}{R1}$$

$$I_{O\text{MAX}} = \left( \frac{V_{\text{REF}}}{R1+R2} \right) + I_{\text{ADJ}} @ \frac{1.25\text{V}}{R1+R2}$$

$$5\text{mA} < I_O < 500\text{mA}$$

**Physical Dimensions**

**TO-92 Bulk Type**



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

| PIN | 92 |   |   | 94 |   |   | 96 |   |   | 97 |   |   | 98 |   |   |
|-----|----|---|---|----|---|---|----|---|---|----|---|---|----|---|---|
|     | P  | F | M | P  | F | M | B  | F | M | P  | F | M | P  | F | M |
| 1   | E  | S |   | E  | S |   | B  | D |   | G  | C |   | G  | D |   |
| 2   | B  | D |   | G  | C |   | G  | D |   | E  | S |   | S  | B |   |
| 3   | C  | G |   | D  | B |   | D  | G |   | C  | G |   | D  | E |   |

LEGEND:

- P - BIPOLAR
- F - JFET
- M - DMOS
- E - EMITTER
- B - BASE
- C - COLLECTOR
- D - DRAIN
- S - SOURCE
- G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

**Figure 5. 3-Lead, TO-92, Molded, Standard Straight Lead**

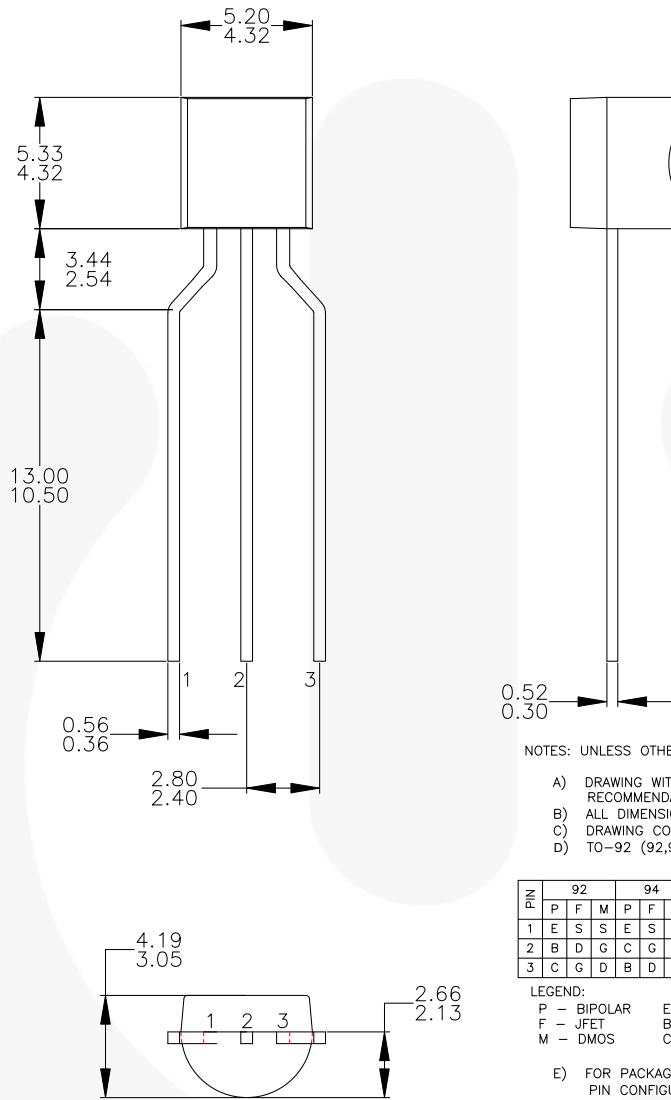
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**Physical Dimensions**

**TO-92 Tape and Reel Type**



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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

| PIN | 92 |   |   | 94 |   |   | 96 |   |   | 97 |   |   | 98 |   |   |
|-----|----|---|---|----|---|---|----|---|---|----|---|---|----|---|---|
|     | P  | F | M | P  | F | M | B  | F | M | P  | F | M | P  | F | M |
| 1   | E  | S | S | E  | S | S | B  | D | G | C  | G | D | C  | G | D |
| 2   | B  | D | G | C  | G | D | E  | S | S | B  | D | G | E  | S | S |
| 3   | C  | G | D | B  | D | G | C  | G | D | E  | S | S | B  | D | G |

LEGEND:

- P - BIPOLAR
- F - JFET
- M - DMOS
- E - EMITTER
- B - BASE
- C - COLLECTOR
- D - DRAIN
- S - SOURCE
- G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03FREV2.

**Figure 6. 3-Lead, TO-92, Molded, 0.200 in Line Spacing Lead Form**

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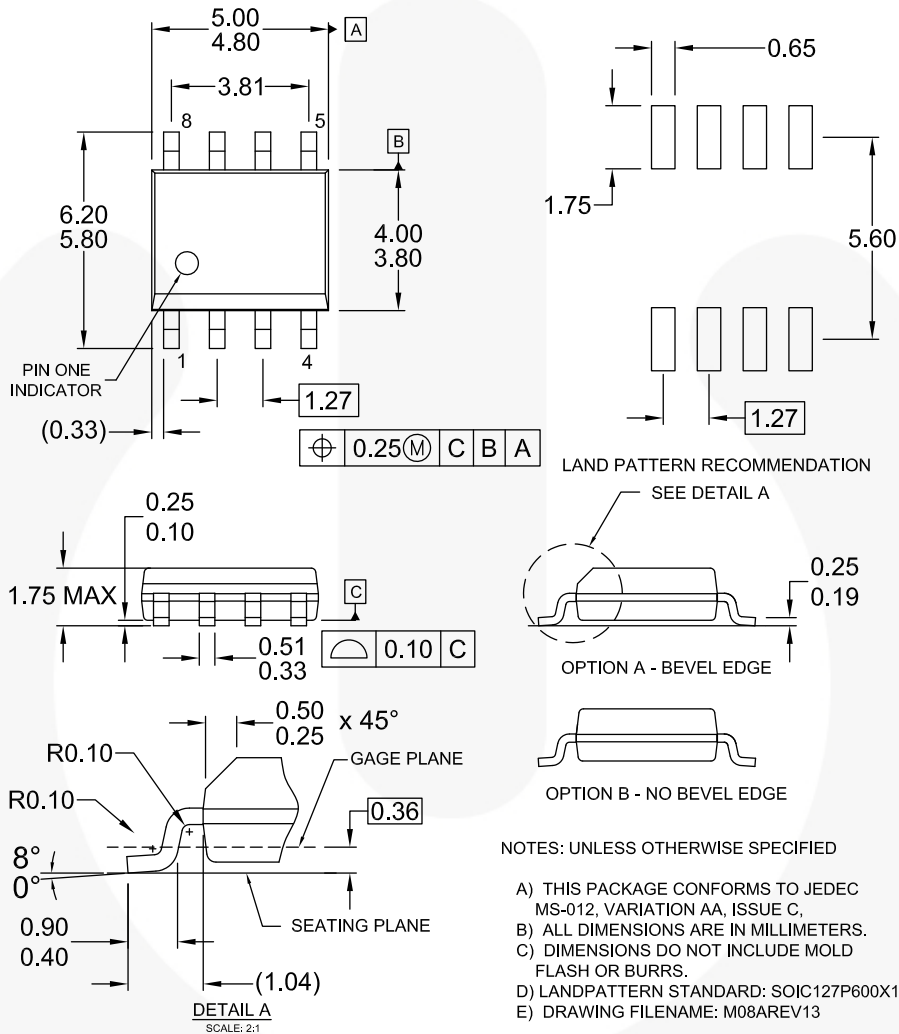
<http://www.fairchildsemi.com/packaging/>

For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:

[http://www.fairchildsemi.com/products/discrete/pdf/to92\\_tr.pdf](http://www.fairchildsemi.com/products/discrete/pdf/to92_tr.pdf)

**Physical Dimensions** (Continued)

**8-SOIC**



**Figure 7. 8-Lead, SOIC, JEDEC MS 0-12, 0.150 inch Narrow Body**

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