Dual Low-Leakage Pico–Amp Diodes

DPAD1 **SSTDPAD5**
DPAD5 **SSTDPAD100**
DPAD50

PRODUCT SUMMARY	
Part Number	**I_R Max (pA)**
DPAD1	–1
DPAD5/SSTDPAD5	–5
DPAD50	–50
SSTDPAD100	–100

FEATURES

- Ultralow Leakage: DPAD1 <1 pA
- Ultralow Capacitance: DPAD1 <0.8 pF

BENEFITS

- Negligible Circuit Leakage Contribution
- Circuit “Transparent” Except to Shunt High-Frequency Spikes

APPLICATIONS

- Op Amp Input Protection
- Multiplexer Overvoltage Protection

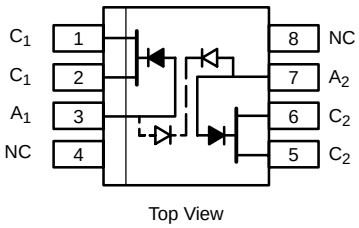
DESCRIPTION

The DPAD/SSTDPAD series of extremely low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. These devices feature leakage currents ranging from –1 pA (DPAD1) to –100 pA (SSTDPAD100) to support a wide range of applications.

The low-cost, compact, narrow-body SO-8 (SSTDPAD) package allows maximum circuit performance. Tape- and-reel options are avaliable for automated assembly (see Packaging Information).

The TO-78 and TO-71 (DPAD) hermetically sealed metal cans are available with full military processing per MIL-S-19500 (see Military Information).

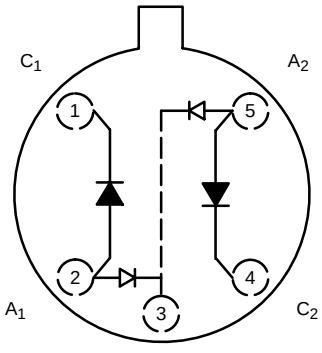
Narrow Body SOIC



Top View

SSTDPAD5
SSTDPAD100

TO-78



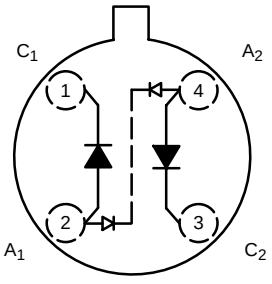
Case*
Substrate

Top View

DPAD1

*Case and Pin 3 must be floating

TO-71 Modified



Top View

DPAD5
DPAD50

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ABSOLUTE MAXIMUM RATINGS[a]

Forward Current . . . . . 50 mA
Storage Temperature . . . . . –55 to 150°C
Operating Junction Temperature . . . . . –55 to 150°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300°C
Total Device Dissipation[b] . . . . . 500 mW

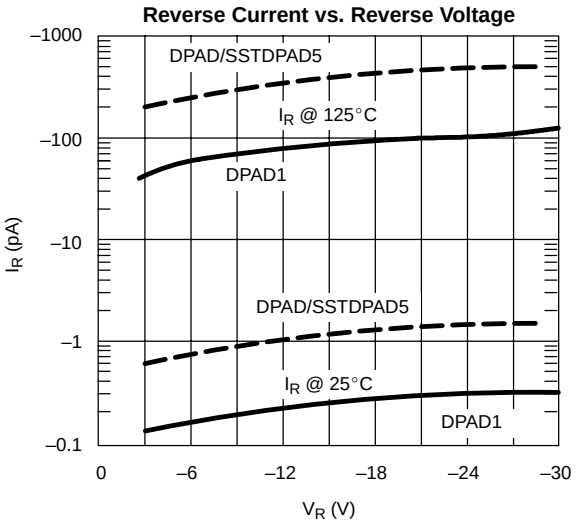
Notes:
a. T_A = 25°C unless otherwise noted.
b. Derate 4 mW/°C at 25°C.

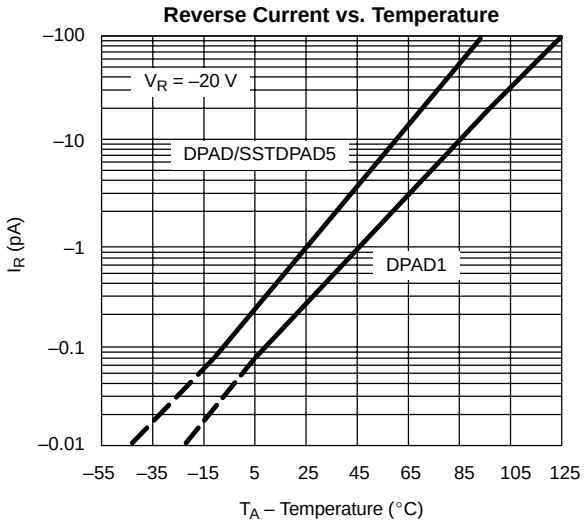
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions		Limits Min	Limits Typ[a]	Limits Max	Unit
Static							
Reverse Current	I_R	V_R = –20 V	DPAD1		–0.2	–1	pA
			DPAD5/SSTDPAD5		–2	–5	
			DPAD5/SSTDPAD5DPAD50		–5	–50	
			SSTDPAD100		–10	–100	
Reverse Breakdown Voltage	BV_R	I_R = –1 μA	DPAD1	–45	–60		V
			DPAD5/DPAD50	–45	–55		
			SSTDPAD5/SSTDPAD100	–30	–50		
Forward Voltage Drop	V_F	I_F = 1 mA			0.8	1.5	
Dynamic							
Reverse Capacitance	C_R	V_R = –5V, f = 1 MHz	DPAD1		**0.6**	0.8	pF
			DPAD5/DPAD50		1.0	2.0	
			SSTDPAD5/SSTDPAD100		2.0	4.0	
Differential Capacitance	$\lvert C_{R1} - C_{R2} \rvert$	$V_{R1} = V_{R2}$ = –5 V, f = 1 MHz	DPAD1		0.07	0.2	
			All Others		0.1	0.5	

Notes:
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)





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