Document Title

32Kx8 bit Low Power CMOS Static RAM

Revision History

Revision No.	History	Draft Data	Remark
0.0	Initial draft	October 09, 2002	Preliminary
1.0	Finalized - Changed I_{CC} from 10mA to 5mA - Changed I_{CC1} from 8mA to 7mA - Changed I_{CC2} from 35mA to 25mA - Changed I_{SB} from 3mA to 0.4mA - Changed I_{DR} for K6X0808C1D-F 15μA to 10μA - Changed I_{DR} for K6X0808C1D-Q 25μA to 20μA - Errata correction	December 16, 2003	Final
2.0	Revised - Changed I_{SB1} of Automotive product from 25μA to 30μA - Deleted 55ns Automotive product	July 15, 2004	Final
3.0	Revised - Changed I_{SB1} of Automotive product from 30μA to 50μA - Changed I_{DR} of Automotive product from 20μA to 25μA - Added Lead Free Products	March 27, 2005	Final

32Kx8 bit Low Power full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 32K x 8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 28-DIP-600B, 28-SOP-450, 28-TSOP1-0813.4F/R

GENERAL DESCRIPTION

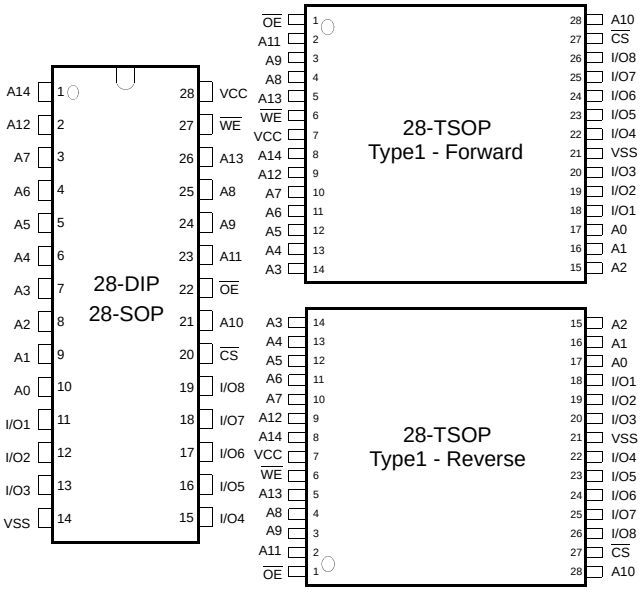
The K6X0808C1D families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support verious operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
K6X0808C1D-F	Industrial(-40~85°C)	4.5~5.5V	55[1]/70ns	15μA	25mA	28-DIP-600B, 28-SOP-450, 28-TSOP1-0813.4F/R
K6X0808C1D-Q	Automotive(-40~125°C)		70ns	50μA		28-SOP-450, 28-TSOP1-0813.4F

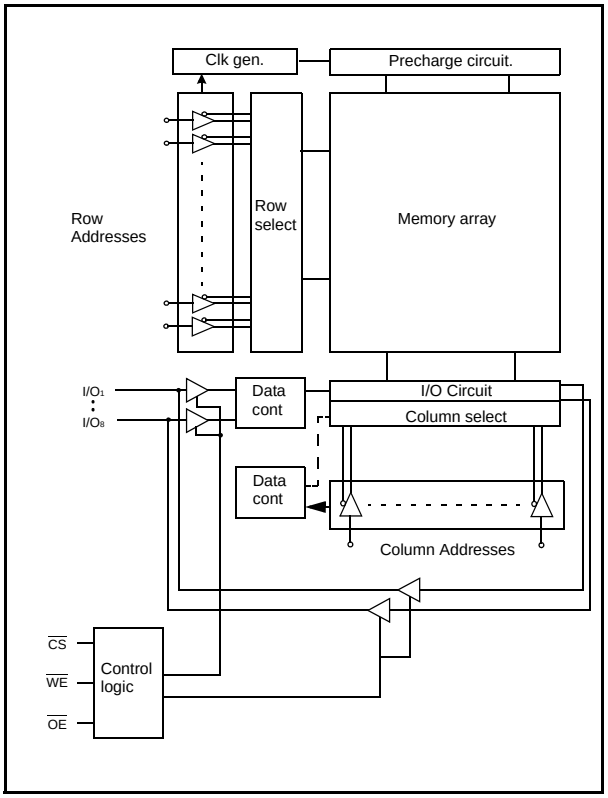
1. The parameters are tested with 50pF test load

PIN DESCRIPTION



Pin Name	Function	Pin Name	Function
$\overline{CS}$	Chip Select Input	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
A_0~A_{14}	Address Inputs	NC	No connect

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

PRODUCT LIST

Industrial Temp. Products(-40~85°C)		Automotive Temp. Products(-40~125°C)	
Part Name	**Function**	**Part Name**	**Function**
K6X0808C1D-DF55	28-DIP, 55ns, LL Pwr	K6X0808C1D-GQ70	28-SOP, 70ns, L Pwr
K6X0808C1D-DF70	28-DIP, 70ns, LL Pwr	K6X0808C1D-BQ70[1)]	28-SOP, 70ns, L Pwr, LF
K6X0808C1D-GF55	28-SOP, 55ns, LL Pwr	K6X0808C1D-TQ70	28-TSOP-F, 70ns, L Pwr
K6X0808C1D-GF70	28-SOP, 70ns, LL Pwr	K6X0808C1D-LQ70[1)]	28-TSOP-F, 70ns, L Pwr, LF
K6X0808C1D-BF55[1)]	28-SOP, 55ns, LL Pwr, LF		
K6X0808C1D-BF70[1)]	28-SOP, 70ns, LL Pwr, LF		
K6X0808C1D-TF55	28-TSOP-F, 55ns, LL Pwr		
K6X0808C1D-TF70	28-TSOP-F, 70ns, LL Pwr		
K6X0808C1D-LF55[1)]	28-TSOP-F, 55ns, LL Pwr, LF		
K6X0808C1D-LF70[1)]	28-TSOP-F, 70ns, LL Pwr, LF		
K6X0808C1D-RF55	28-TSOP-R, 55ns, LL Pwr		
K6X0808C1D-RF70	28-TSOP-R, 70ns, LL Pwr		

1.Lead Free Products

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1)]	X[1)]	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X[1)]	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5V(Max. 7.0V)	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	-40 to 85	°C	K6X0808C1D-F
		-40 to 125	°C	K6X0808C1D-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5[2)]	V
Input low voltage	V_{IL}	-0.5[3)]	-	0.8	V

Note:
1. Industrial Product: T_A=-40 to 85°C, Otherwise specified
   Automotive Product: T_A=-40 to 125°C, Otherwise specified
2. Overshoot: Vcc+3.0V in case of pulse width≤30ns.
3. Undershoot: -3.0V in case of pulse width≤30ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

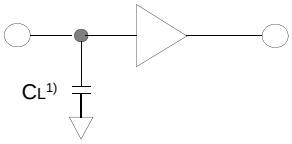
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, Read		-	-	5	mA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, V_{IN}≤0.2V_{IN}≥Vcc -0.2V		-	-	7	mA
	I_{CC2}	Cycle time=Min,100% duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	-	25	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs=V_{IH} or V_{IL}		-	-	0.4	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc	K6X0808C1D-F	-	-	15	μA
			K6X0808C1D-Q	-	-	50	μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.8 to 2.4V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load (See right): C_L=100pF+1TTL
C_L=50pF+1TTL



1. Including scope and jig capacitance

AC CHARACTERISTICS (Vcc=4.5~5.5V, Industrial product: T_A=-40 to 85°C, Automotive product: T_A=-40 to 125°C)

Parameter List		Symbol	Speed Bins				Units
			55[1]ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	55	-	70	-	ns
	Address access time	t_{AA}	-	55	-	70	ns
	Chip select to output	t_{CO}	-	55	-	70	ns
	Output enable to valid output	t_{OE}	-	25	-	35	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	20	0	30	ns
	Output disable to high-Z output	t_{OHZ}	0	20	0	30	ns
	Output hold from address change	t_{OH}	10	-	10	-	ns
Write	Write cycle time	t_{WC}	55	-	70	-	ns
	Chip select to end of write	t_{CW}	45	-	60	-	ns
	Address set-up time	t_{AS}	0	-	0	-	ns
	Address valid to end of write	t_{AW}	45	-	60	-	ns
	Write pulse width	t_{WP}	40	-	50	-	ns
	Write recovery time	t_{WR}	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	0	25	ns
	Data to write time overlap	t_{DW}	25	-	30	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	ns

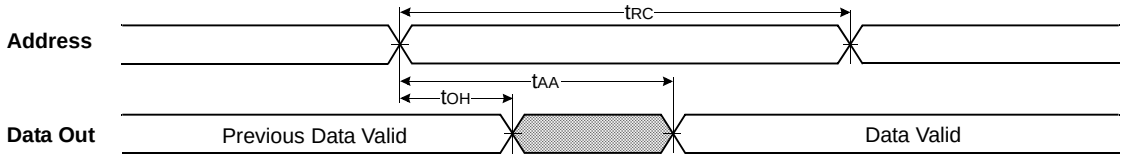
1. The parameter is tested with 50pF test load. Industrial Product only.

DATA RETENTION CHARACTERISTICS

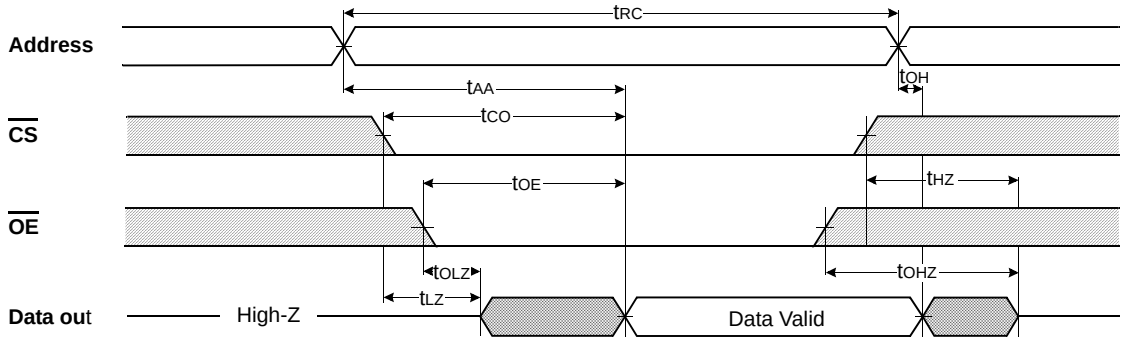
Item	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V	K6X0808C1D-F	-	-	10	µA
			K6X0808C1D-Q	-	-	25	
Data retention set-up time	t_{SDR}	See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}			5	-	-	

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



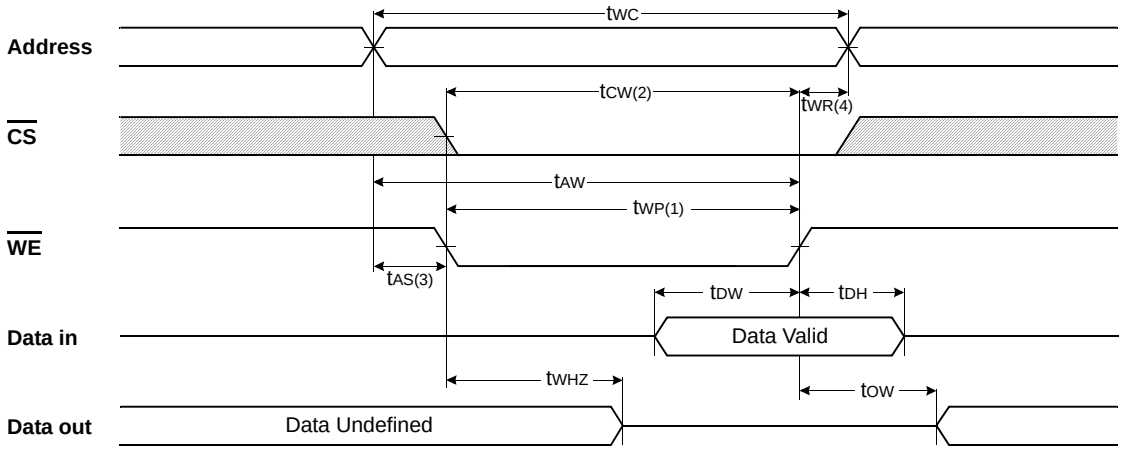
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



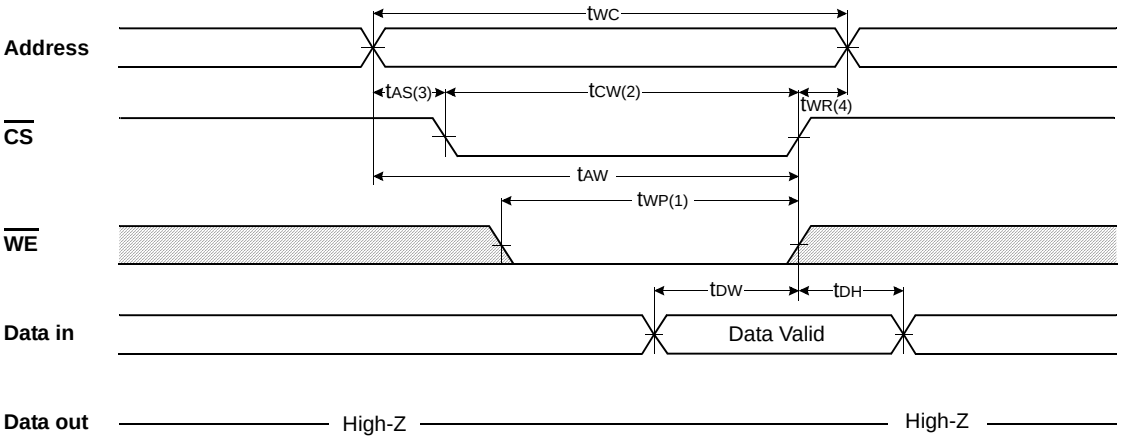
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

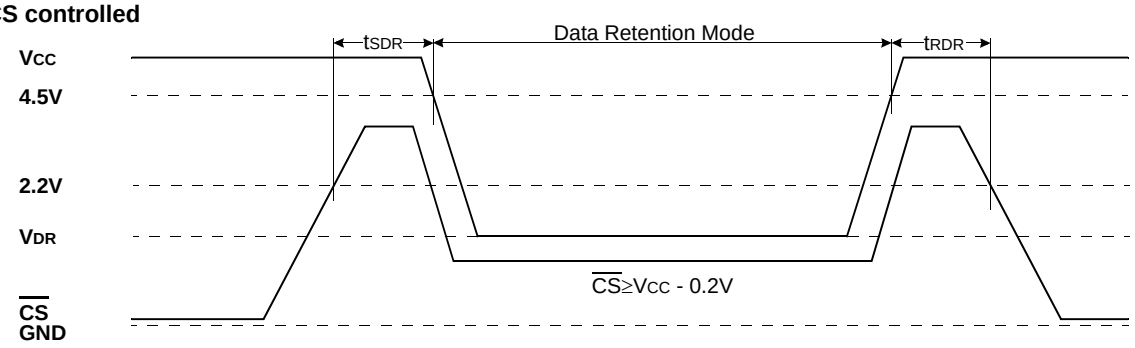


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

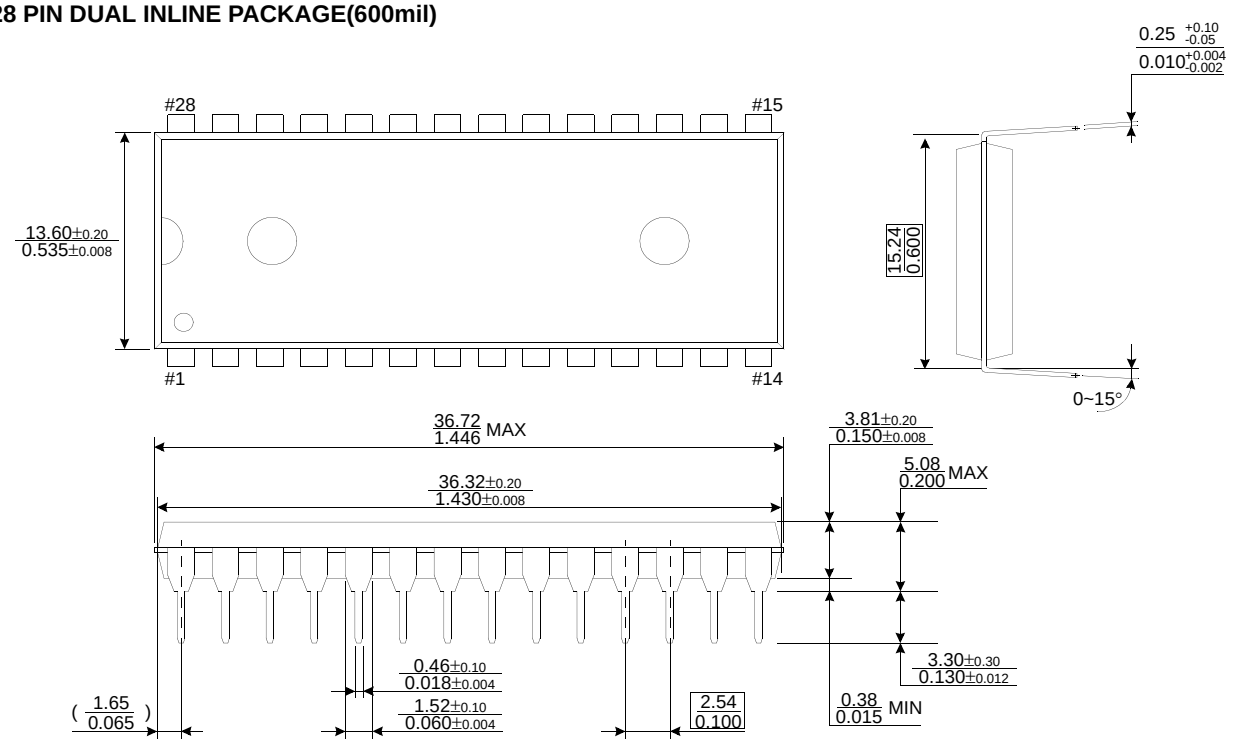
$\overline{CS}$ controlled



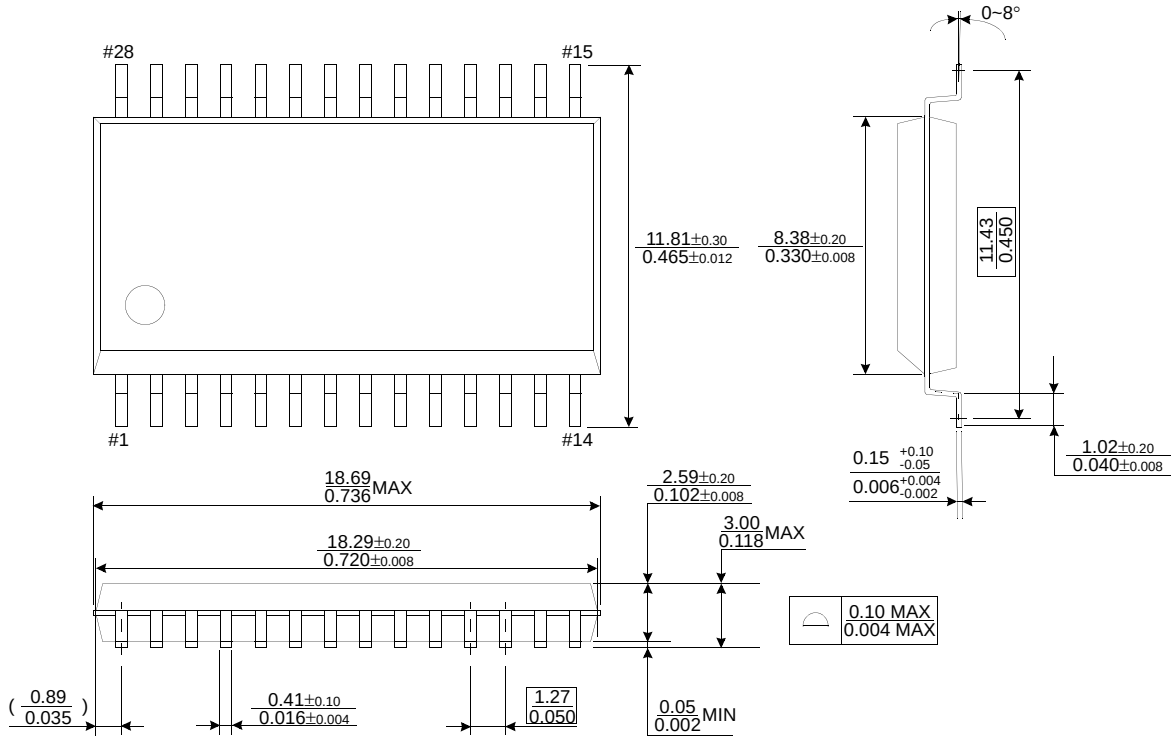
PACKAGE DIMENSIONS

Units: millimeter(inch)

28 PIN DUAL INLINE PACKAGE(600mil)



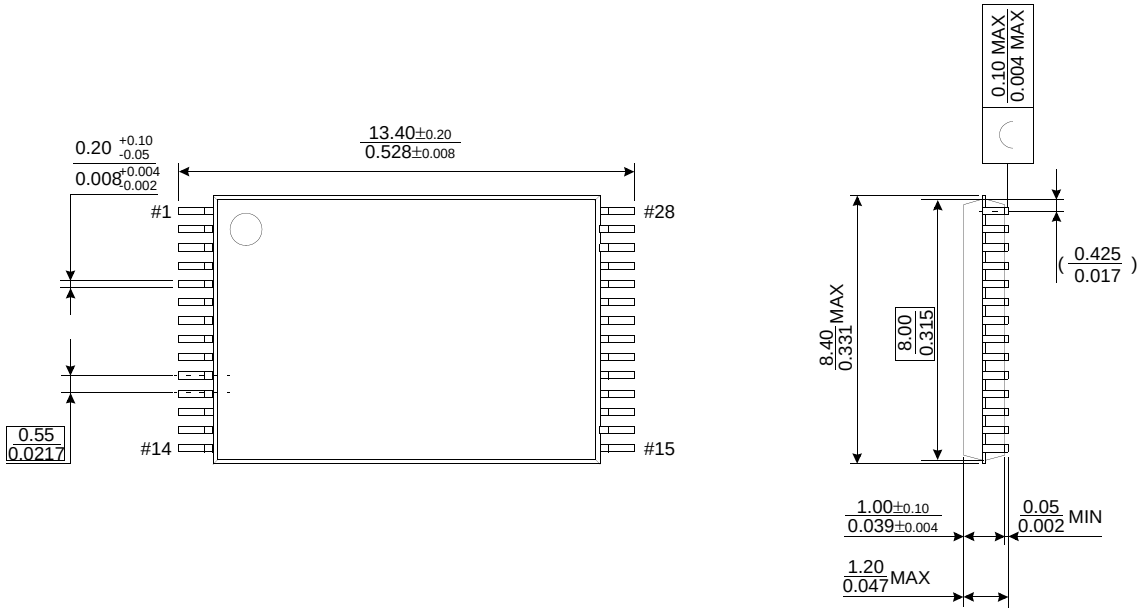
28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



PACKAGE DIMENSIONS

Units: millimeter(inch)

28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)