Rev. 1.7, Feb. 2017

M471A5644EB0
M471A5143EB0
M471A5143EB1

260pin Unbuffered SODIMM based on 4Gb E-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

SAMSUNG

Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First SPEC. Release	4th Jun. 2015	-	J.Y.Lee
1.1	- Addition of Module line up (2GB Non-ECC SODIMM) without IDD	30th Sep. 2015	-	J.Y.Lee
1.2	- Addition of IDD values (2GB)	19th Oct. 2015	-	J.Y.Lee
1.3	- Change of VDDSPD tolerance on page 8	5th Nov. 2015	-	J.Y.Lee
1.4	- Change of PCB gerber (only 1Rx8, 2400Mbps)	9th Dec. 2015	-	S.H.Kim
1.5	- Change of Physical Dimensions on page 37~39	15th Mar. 2016	-	S.H.Kim
1.6	- Addition of Functional Block Diagram on page 12~13	14th Apr. 2016	-	S.H.Kim
1.61	- Correction of typo	29th Jun. 2016	-	J.Y.Lee
1.7	- Change of Physical Dimensions on page 41~43	24th Feb. 2017	-	J.Y.Lee

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260pin Unbuffered SODIMM based on 4Gb E-die

1. DDR4 Unbuffered SODIMM Ordering Information

Part Number[2]	Density	Organization	Component Composition[1]	Number of Rank	Height
M471A5644EB0-CPB/RC	2GB	256Mx64	256Mx16(K4A4G165WE-BC##)*4	1	30mm
M471A5143EB0-CPB	4GB	512Mx64	512Mx8(K4A4G085WE-BCPB)*8	1	30mm
M471A5143EB1-CPB/RC	4GB	512Mx64	512Mx8(K4A4G085WE-BCRC)*8	1	30mm

NOTE :
1. "##" - PB/RC
2. PB(2133Mbps 15-15-15)/RC(2400Mbps 17-17-17)
   - DDR4-2400(17-17-17) is backward compatible to DDR4-2133(15-15-15)

2. Key Features

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	
tCK(min)	1.25	1.071	0.938	0.833	ns
CAS Latency	11	13	15	17	nCK
tRCD(min)	13.75	13.92	14.06	14.16	ns
tRP(min)	13.75	13.92	14.06	14.16	ns
tRAS(min)	35	34	33	32	ns
tRC(min)	48.75	47.92	47.06	46.16	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable $\overline{CAS}$ Latency: 10,11,12,13,14,15,16,17,18
- Programmable Additive Latency(Posted $\overline{CAS}$) : 0, CL - 2, or CL - 1 clock
- Programmable $\overline{CAS}$ Write Latency(CWL) = 9,11 (DDR4-1600) , 10,12 (DDR4-1866) ,11,14 (DDR4-2133) and 12,16 (DDR4-2400)
- Burst Length: 8 , 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95°C
- Asynchronous Reset

3. Address Configuration

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
256Mx16(4Gb) based Module	A0-A14	A0-A9	BG0	BA0-BA1	A10/AP
512Mx8(4Gb) based Module	A0-A14	A0-A9	BG0-BG1	BA0-BA1	A10/AP

4. Unbuffered SODIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	79	DQ30	80	DQ31	157	CS1_n1	158	A13	235	VSS	236	DQ57
3	DQ5	4	DQ4	81	VSS	82	VSS	159	VDD	160	VDD	237	DQ56	238	VSS
5	VSS	6	VSS	83	DQ26	84	DQ27	161	ODT1	162	C0,CS2_n,NC	239	VSS	240	DQS7_c
7	DQ1	8	DQ0	85	VSS	86	VSS	163	VDD	164	VREFCA	241	DM7_n/ DBI7_n	242	DQS7_t
9	VSS	10	VSS	87	CB5,NC	88	CB4,NC	165	C1,CS3_n,NC	166	SA2	243	VSS	244	VSS
11	DQS0_c	12	DM0_n/ DBI0_n	89	VSS	90	VSS	167	VSS	168	VSS	245	DQ62	246	DQ63
13	DQS0_t	14	VSS	91	CB1,NC	92	CB0,NC	169	DQ37	170	DQ36	247	VSS	248	VSS
15	VSS	16	DQ6	93	VSS	94	VSS	171	VSS	172	VSS	249	DQ58	250	DQ59
17	DQ7	18	VSS	95	DQS8_c	96	DBI8_n	173	DQ33	174	DQ32	251	VSS	252	VSS
19	VSS	20	DQ2	97	DQS8_t	98	VSS	175	VSS	176	VSS	253	SCL	254	SDA
21	DQ3	22	VSS	99	VSS	100	CB6,NC	177	DQS4_c	178	DM4_n/ DBI4_n	255	VDDSPD	256	SA0
23	VSS	24	DQ12	101	CB2,NC	102	VSS	179	DQS4_t	180	VSS	257	VPP	258	Vtt
25	DQ13	26	VSS	103	VSS	104	CB7,NC	181	VSS	182	DQ39	259	VPP	260	SA1
27	VSS	28	DQ8	105	CB3,NC	106	VSS	183	DQ38	184	VSS				
29	DQ9	30	VSS	107	VSS	108	RESET_n	185	VSS	186	DQ35				
31	VSS	32	DQS1_c	109	CKE0	110	CKE1	187	DQ34	188	VSS				
33	DM1_n/ DBI1_n	34	DQS1_t	111	VDD	112	VDD	189	VSS	190	DQ45				
35	VSS	36	VSS	113	BG1	114	ACT_n	191	DQ44	192	VSS				
37	DQ15	38	DQ14	115	BG0	116	ALERT_n	193	VSS	194	DQ41				
39	VSS	40	VSS	117	VDD	118	VDD	195	DQ40	196	VSS				
41	DQ10	42	DQ11	119	A12	120	A11	197	VSS	198	DQS5_c				
43	VSS	44	VSS	121	A9	122	A7	199	DM5_n/ DBI5_n	200	DQS5_t				
45	DQ21	46	DQ20	123	VDD	124	VDD	201	VSS	202	VSS				
47	VSS	48	VSS	125	A8	126	A5	203	DQ46	204	DQ47				
49	DQ17	50	DQ16	127	A6	128	A4	205	VSS	206	VSS				
51	VSS	52	VSS	129	VDD	130	VDD	207	DQ42	208	DQ43				
53	DQS2_c	54	DM2_n/ DBI2_n	131	A3	132	A2	209	VSS	210	VSS				
55	DQS2_t	56	VSS	133	A1	134	EVENT_n	211	DQ52	212	DQ53				
57	VSS	58	DQ22	135	VDD	136	VDD	213	VSS	214	VSS				
59	DQ23	60	VSS	137	CK0_t	138	CK1_t	215	DQ49	216	DQ48				
61	VSS	62	DQ18	139	CK0_c	140	CK1_c	217	VSS	218	VSS				
63	DQ19	64	VSS	141	VDD	142	VDD	219	DQS6_c	220	DM6_n/ DBI6_n				
65	VSS	66	DQ28	143	Parity	144	A0	221	DQS6_t	222	VSS				
67	DQ29	68	VSS	145	BA1	146	A10/AP	223	VSS	224	DQ54				
69	VSS	70	DQ24	147	VDD	148	VDD	225	DQ55	226	VSS				
71	DQ25	72	VSS	149	CS0_n	150	BA0	227	VSS	228	DQ50				
73	VSS	74	DQS3_c	151	A14/WE_n	152	A16/RAS_n	229	DQ51	230	VSS				
75	DM3_n/ DBI3_n	76	DQS3_t	153	VDD	154	VDD	231	VSS	232	DQ60				
77	VSS	78	VSS	155	$\overline{ODT0}$	156	A15/CAS_n	233	DQ61	234	VSS				

5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I²C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I²C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0~SA2	I²C slave address select for SPD/TS
RAS_n[1]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[2]	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n[3]	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n–CS1_n	Rank Select Lines	C0,C1	Chip ID lines for 3DS components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	TS signals a thermal event has occurred
DM0_n-DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

NOTE :

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.

[Table 1] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

6. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.

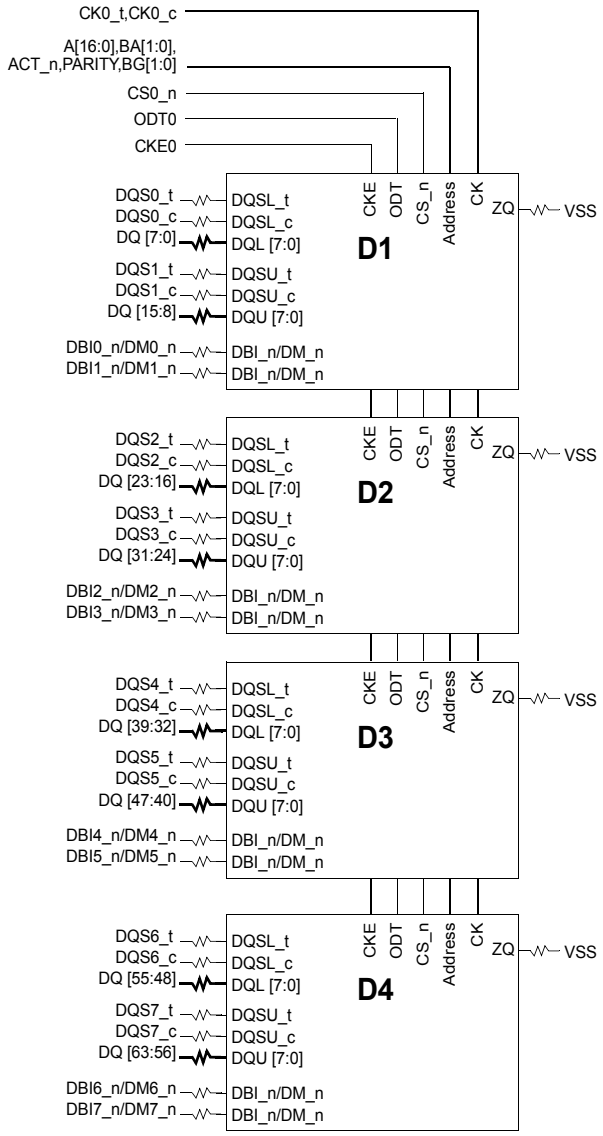
Symbol	Type	Function
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output	ALERT: It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system. In case of not connected as Signal, ALERT_n Pin must be connected to VDD on DIMM.
SA0-SA1	Input	Device address for the SPD.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD[1]	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VTT[2]	Supply	Power Supply: 0.6 V
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD 2.5V or 3.3V.

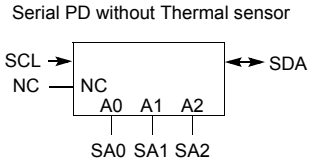
NOTE :

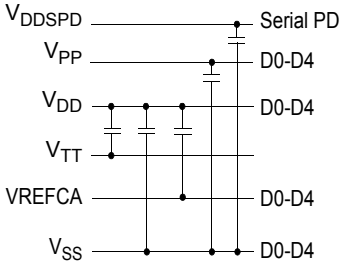
1. For PC4, VDD is 1.2 V. For PC4L VDD is TBD.
2. For PC4, VTT is 0.6 V. For PC4L VTT is TBD.

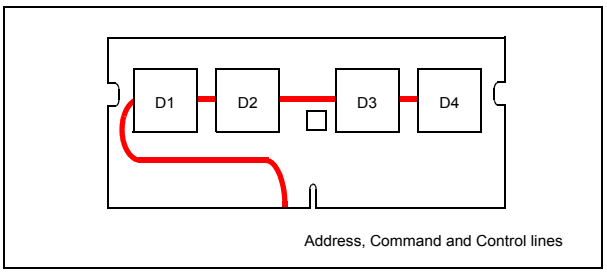
7. Function Block Diagram

7.1 2GB, 256Mx64 Module (Populated as 1 rank of x16 DDR4 SDRAMs)





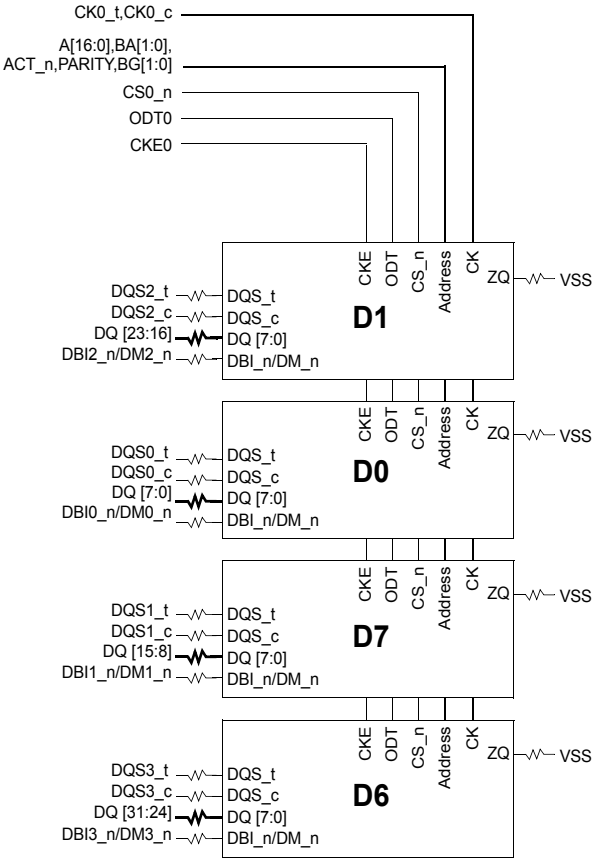


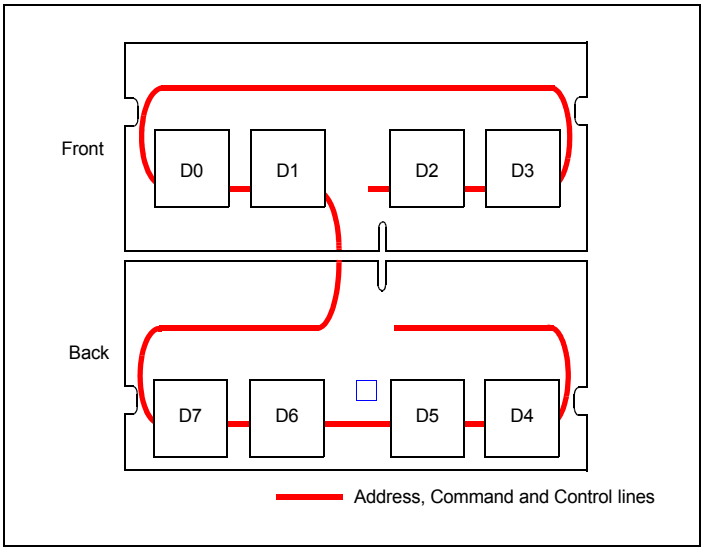


NOTE :

1. Unless otherwise noted, resistor values are 15Ω ± 5%.
2. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
3. CK1_t, CK1_c terminated with 75Ω ± 5% resistor.

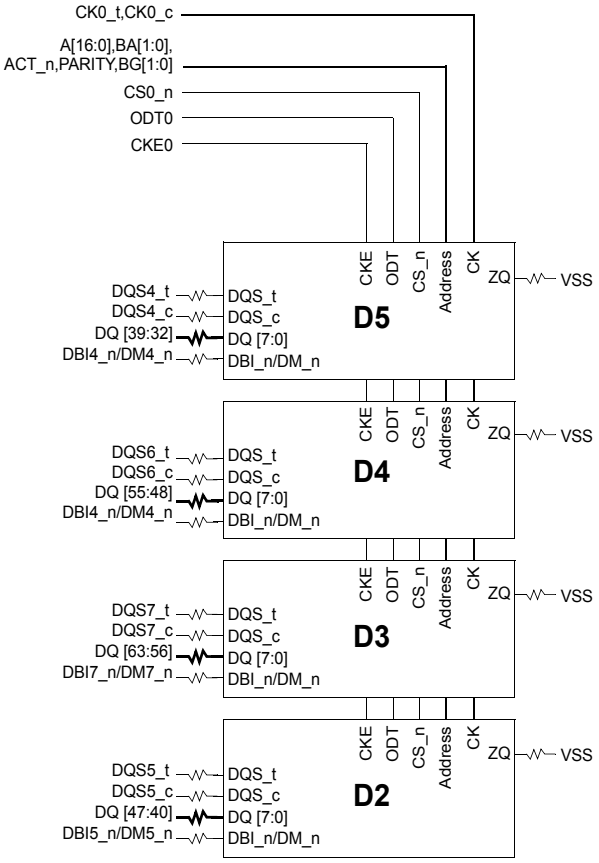
7.2 4GB, 512Mx64 Module (Populated as 1 rank of x8 DDR4 2133Mbps SDRAMs,A0)

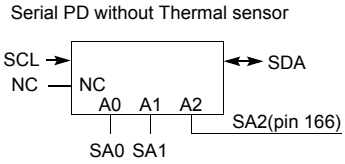


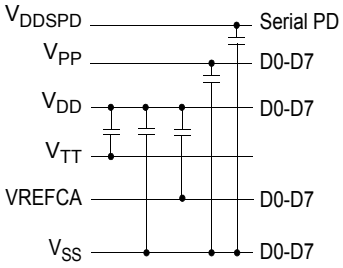


NOTE :

1. Unless otherwise noted, resistor values are 15Ω ± 5%.
2. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.



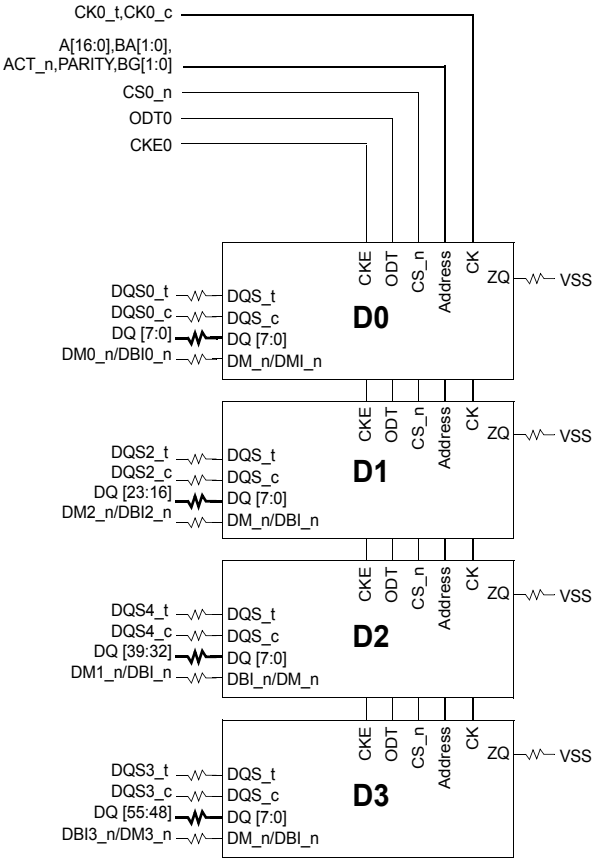


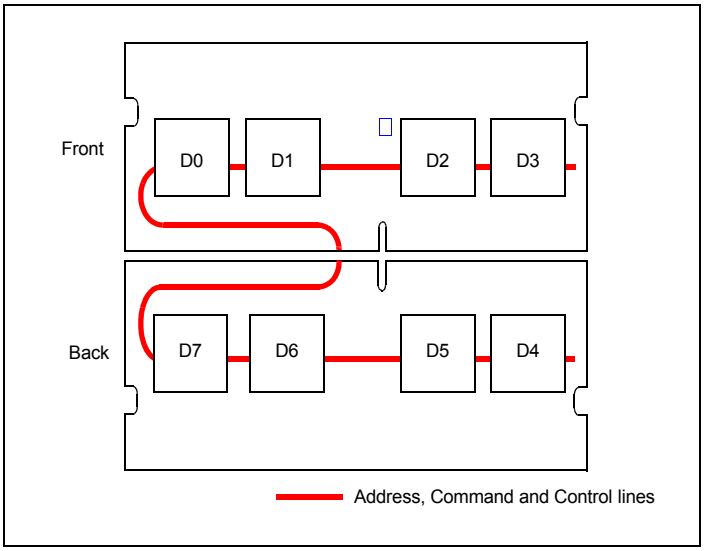


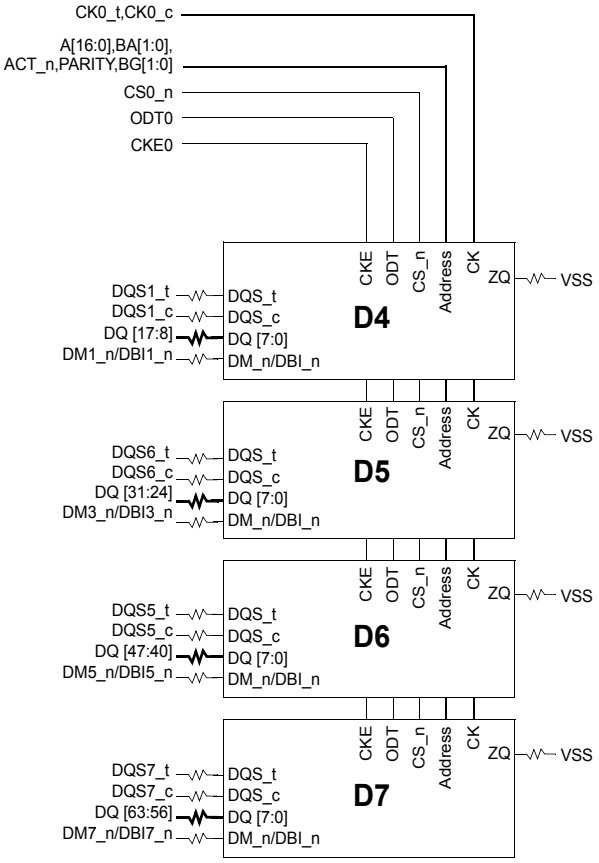
NOTE :

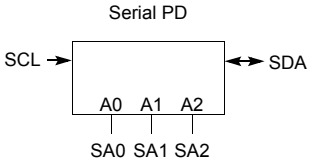
1. Unless otherwise noted, resistor values are 15Ω ± 5%.
2. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
3. To connect the SPD A2 input to the edge connector pin 166 install R1. To tie the SPD input A2 to ground install R2. Do not install both R1 and R2. The values for R1 and R2 are not critical. Any value less than 100 Ohms may be used.

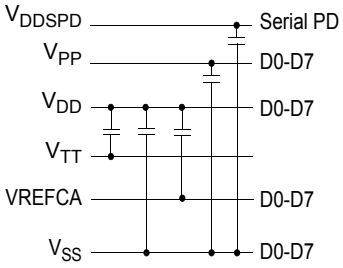
7.3 4GB, 512Mx64 Module (Populated as 1 rank of x8 DDR4 2133/2400Mbps SDRAMs,A1)











NOTE :

1. Unless otherwise noted, resistor values are 15Ω ± 5%.
2. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.

8. Absolute Maximum Ratings

8.1 Absolute Maximum DC Ratings

[Table 2] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA to Vss	-0.3 ~ 1.5	V	1,3
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

9. AC & DC Operating Conditions

9.1 Recommended DC Operating Conditions

[Table 3] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. DC bandwidth is limited to 20MHz.

10. AC & DC Input Measurement Levels

10.1 AC & DC Logic Input Levels for Single-Ended Signals

[Table 4] Single-ended AC & DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		Unit	NOTE
		Min.	Max.		
$V_{IH.CA}$(DC75)	DC input logic high	V_{REFCA}+ 0.075	V_{DD}	V	
$V_{IL.CA}$(DC75)	DC input logic low	V_{SS}	V_{REFCA}-0.075	V	
$V_{IH.CA}$(AC100)	AC input logic high	V_{REF} + 0.1	Note 2	V	1
$V_{IL.CA}$(AC100)	AC input logic low	Note 2	V_{REF} - 0.1	V	1
V_{REFCA}(DC)	Reference Voltage for ADD, CMD inputs	0.49*V_{DD}	0.51*V_{DD}	V	2,3

NOTE:
1. See “Overshoot and Undershoot Specifications” on section.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference: approx. ± 12mV)
3. For reference: approx. VDD/2 ± 12mV

10.2 AC and DC Input Measurement Levels : V_{REF} Tolerances.

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 1. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA}).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 4. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than ± 1% V_{DD}.

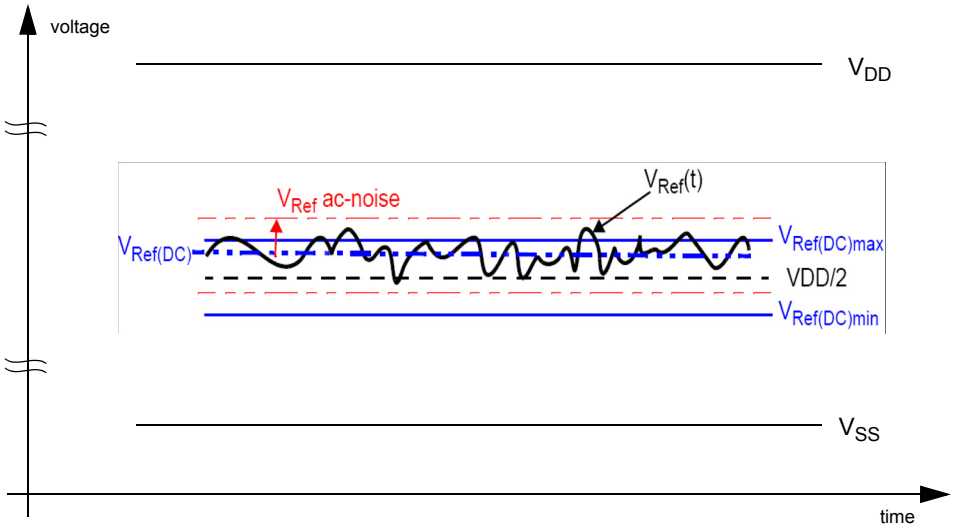


Figure 1. Illustration of V_{REF}(DC) tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

"V_{REF}" shall be understood as V_{REF}(DC), as defined in Figure 1.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

10.3 AC and DC Logic Input Levels for Differential Signals

10.3.1 Differential Signals Definition

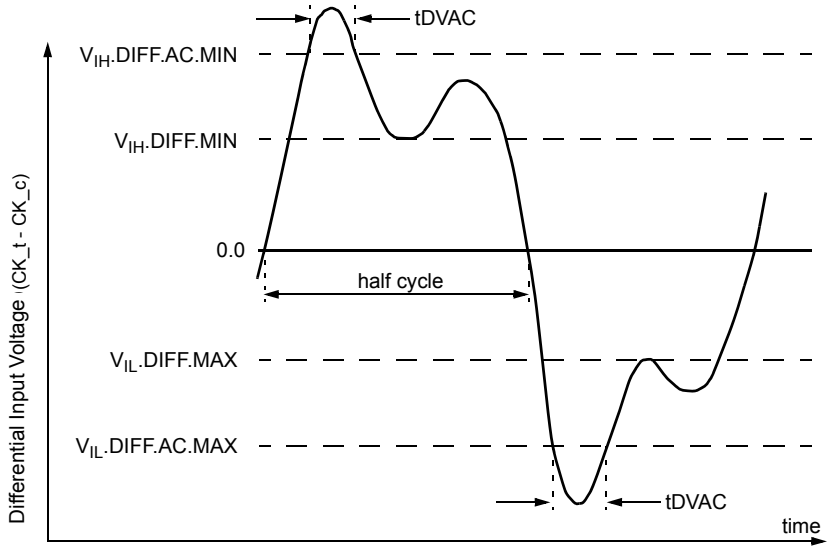


Figure 2. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

NOTE:
1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

10.3.2 Differential Swing Requirements for Clock (CK_t - CK_c)

[Table 5] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400		unit	NOTE
		min	max	min	max		
V_{IHdiff}	differential input high	+0.150	NOTE 3	TBD	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	-0.150	NOTE 3	TBD	V	1
V_{IHdiff}(AC)	differential input high ac	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
V_{ILdiff}(AC)	differential input low ac	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

NOTE:
1. Used to define a differential signal slew-rate.
2. for CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD and V_{REFCA};
3. These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

[Table 6] Allowed Time Before Ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH/Ldiff}(AC)\|$ = 200mV	
	min	max
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-

10.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH.CA(AC) / VIL.CA(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than VIH.CA(AC100)/VIL.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c

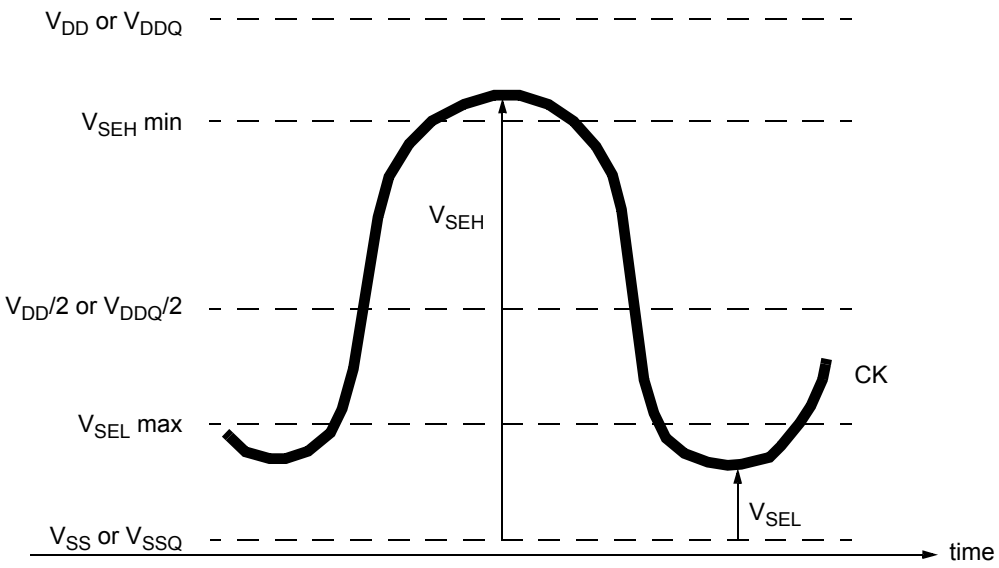


Figure 3. Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 7] Single-ended Levels for CK_t, CK_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	NOTE
		Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t , CK_c	(VDD/2)+0.100	NOTE3	TBD	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t , CK_c	NOTE3	(VDD/2)-0.100	NOTE3	TBD	V	1, 2

NOTE:

1. For CK_t - CK_c use $V_{IH.CA}/V_{IL.CA}$(AC) of ADD/CMD;
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

10.4 Slew Rate Definitions

10.4.1 Slew Rate Definitions for Differential Input Signals (CK)

[Table 8] Differential Input Slew Rate Definition

Description			Defined by
	from	to	
Differential input slew rate for rising edge(CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge(CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff
NOTE: The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.			

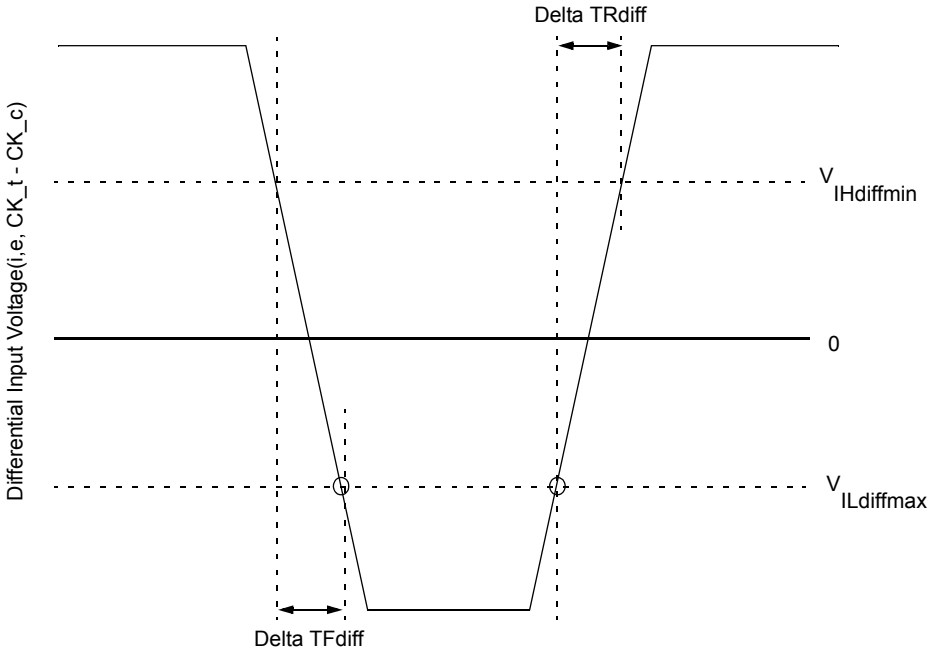


Figure 4. Differential Input Slew Rate Definition for CK_t, CK_c

10.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

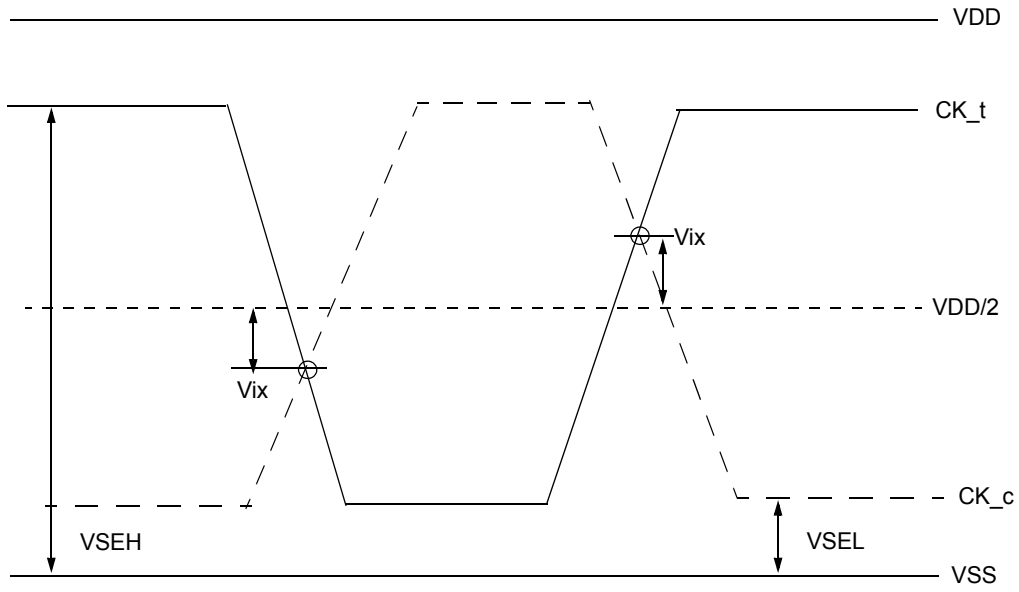


Figure 5. Vix Definition (CK)

[Table 9] Cross Point Voltage for Differential Input Signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133			
		min		max	
-	Area of VSEH, VSEL	VSEL =< VDD/2 - 145mV	VDD/2 - 145mV =< VSEL =< VDD/2 - 100mV	VDD/2 + 100mV =< VSEH =< VDD/2 + 145mV	VDD/2 + 145mV =< VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	-(VDD/2 - VSEL) + 25mV	(VSEH - VDD/2) - 25mV	120mV

Symbol	Parameter	DDR4-2400			
		min		max	
-	Area of VSEH, VSEL	TBD	TBD	TBD	TBD
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	TBD	TBD	TBD	TBD

10.6 Single-ended AC & DC Output Levels

[Table 10] Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400	Units	NOTE
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1

NOTE :
1. The swing of ± 0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

10.7 Differential AC & DC Output Levels

[Table 11] Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400	Units	NOTE
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

NOTE :
1. The swing of ± 0.3 × V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

10.8 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 12 and Figure 6.

[Table 12] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TFse

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

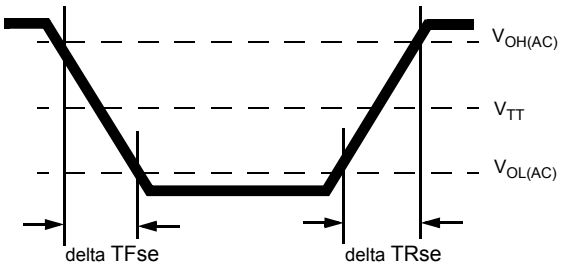


Figure 6. Single-ended Output Slew Rate Definition

[Table 13] Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

NOTE :
1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

10.9 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 14 and Figure 7.

[Table 14] Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TFdiff

NOTE:
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

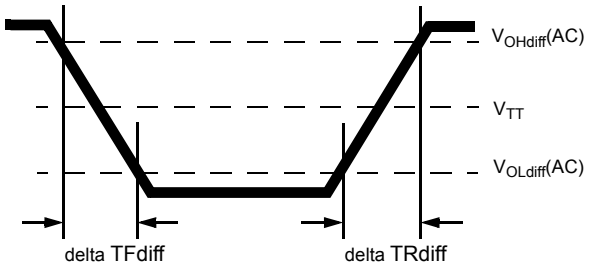


Figure 7. Differential Output Slew Rate Definition

[Table 15] Differential Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

10.10 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[Table 16] Single-ended AC & DC Output Levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

NOTE:
1. The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.

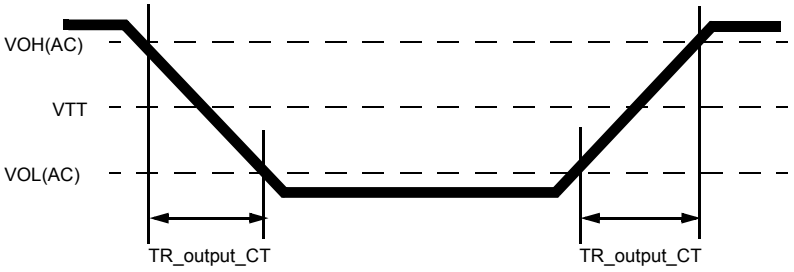


Figure 8. Output Slew Rate Definition of Connectivity Test Mode

[Table 17] Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

10.11 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 9.

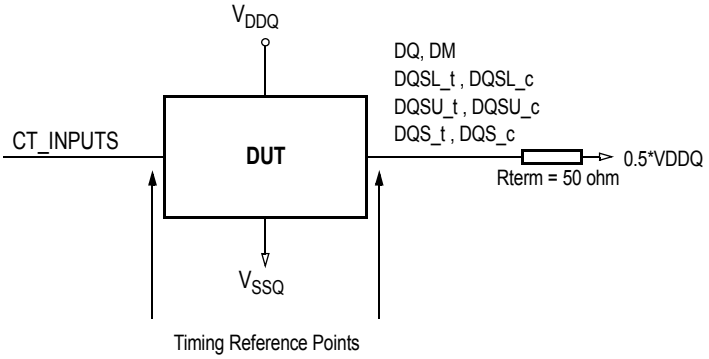


Figure 9. Connectivity Test Mode Timing Reference Load

11. DIMM IDD Specification Definition

[Table 18] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD2NA	**Precharge Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according ; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3,5]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0

Symbol	Description
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:**Refer to Component Datasheet for detail pattern
IDD3NA	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: sRefer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless read data burst with different data between one burst and the next one according ; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD4RA	**Operating Burst Read Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI** **Read DBI enabled[3], Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless write data burst with different data between one burst and the next one ; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD4WA	**Operating Burst Write Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4W
IDD4WB	**Operating Burst Write Current with Write DBI** **Write DBI enabled[3], Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3], Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP5B	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**

Symbol	Description
IDD5F4	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**
IDD6N	**Self Refresh Current: Normal Temperature Range** **T_{CASE}:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range**) **T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** **T_{CASE}:** 0 - 45°C; **Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current** **T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** read data bursts with different data between one burst and the next one ; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
IDD8	**Maximum Power Down Current TBD**
IPP8	**Maximum Power Down IPP Current Same condition with IDD8**

NOTE :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00]
2. Output Buffer Enable
   - set MR1 [A12 = 0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7

   RTT_Nom enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6

   RTT_WR enable
   - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2

   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
   010] : 1866MT/s, 2133MT/s
   011] : 2400MT/s

   Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate

   DLL disabled : set MR1 [A0 = 0]

   CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
   010] : 2400MT/s

   Read DBI enabled : set MR5 [A12 = 1]

   Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Auto Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
   01] : Reduced Temperature range
   10] : Extended Temperature range
   11] : Auto Self Refresh
5. IDD2NG should be measured after sync pules(NOP) input.

12. IDD SPEC Table

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[Table 19] I_{DD} and I_{DDQ} Specification

Symbol	M471A5644EB0 : 2GB(256Mx64) Module				Unit	NOTE
	DDR4-2133		DDR4-2400			
	15-15-15		17-17-17			
	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V		
	IDD Max.	IPP Max.	IDD Max.	IPP Max.		
I_{DD0}	140	16	140	16	mA	
I_{DD0A}	144	16	148	16	mA	
I_{DD1}	212	16	212	16	mA	
I_{DD1A}	220	16	224	16	mA	
I_{DD2N}	60	12	60	12	mA	
I_{DD2NA}	72	12	72	12	mA	
I_{DD2NT}	64	12	64	12	mA	
I_{DD2NL}	44	12	44	12	mA	
I_{DD2NG}	60	12	60	12	mA	
I_{DD2ND}	48	12	48	12	mA	
I_{DD2N_par}	60	12	60	12	mA	
I_{DD2P}	40	12	40	12	mA	
I_{DD2Q}	52	12	52	12	mA	
I_{DD3N}	108	12	108	12	mA	
I_{DD3NA}	112	12	112	12	mA	
I_{DD3P}	52	12	52	12	mA	
I_{DD4R}	472	12	516	12	mA	
I_{DD4RA}	488	12	532	12	mA	
I_{DD4RB}	484	12	532	12	mA	
I_{DD4W}	348	12	344	12	mA	
I_{DD4WA}	364	12	400	12	mA	
I_{DD4WB}	348	12	384	12	mA	
I_{DD4WC}	320	12	332	12	mA	
I_{DD4W_par}	372	12	412	12	mA	
I_{DD5B}	776	76	780	76	mA	
I_{DD5F2}	640	64	640	64	mA	
I_{DD5F4}	480	48	480	48	mA	
I_{DD6N}	52	16	52	16	mA	
I_{DD6E}	80	16	80	16	mA	
I_{DD6R}	40	16	40	16	mA	
I_{DD6A}	52	16	52	16	mA	
I_{DD7}	740	48	744	48	mA	
I_{DD8}	26	8	26	8	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-actived rank(IDLE) is IDD2N. Please refer to Table21.
2. IDD current measure method and detail patterns are described on DDR4 component datasheet.
3. VDD and VDDQ are merged on module PCB (IDDQ values are not considered by Qoff condition)
4. DIMM IDD Values are calculated based on the component IDD spec and Register power.

[Table 20] I_{DD} and I_{DDQ} Specification

Symbol	M471A5143EB0 : 4GB(512Mx64) Module		M471A5143EB1 : 4GB(512Mx64) Module				Unit	NOTE
	DDR4-2133		DDR4-2133		DDR4-2400			
	15-15-15		17-17-17		17-17-17			
	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V		
	IDD Max.	IPP Max.	IDD Max.	IPP Max.	IDD Max.	IPP Max.		
I_{DD0}	240	32	240	32	248	32	mA	
I_{DD0A}	256	32	256	32	264	32	mA	
I_{DD1}	320	24	320	24	336	24	mA	
I_{DD1A}	344	24	344	24	360	24	mA	
I_{DD2N}	120	24	120	24	120	24	mA	
I_{DD2NA}	144	24	144	24	152	24	mA	
I_{DD2NT}	128	24	128	24	136	24	mA	
I_{DD2NL}	88	24	88	24	96	24	mA	
I_{DD2NG}	120	24	120	24	128	24	mA	
I_{DD2ND}	96	24	96	24	96	24	mA	
I_{DD2N_par}	120	24	120	24	120	24	mA	
I_{DD2P}	80	24	80	24	80	24	mA	
I_{DD2Q}	104	24	104	24	104	24	mA	
I_{DD3N}	216	24	216	24	224	24	mA	
I_{DD3NA}	224	24	224	24	232	24	mA	
I_{DD3P}	104	24	104	24	104	24	mA	
I_{DD4R}	672	24	672	24	720	24	mA	
I_{DD4RA}	696	24	696	24	760	24	mA	
I_{DD4RB}	696	24	696	24	752	24	mA	
I_{DD4W}	576	24	576	24	624	24	mA	
I_{DD4WA}	608	24	608	24	648	24	mA	
I_{DD4WB}	576	24	576	24	616	24	mA	
I_{DD4WC}	528	24	528	24	560	24	mA	
I_{DD4W_par}	624	24	624	24	680	24	mA	
I_{DD5B}	1520	144	1520	144	1536	144	mA	
I_{DD5F2}	1280	120	1280	120	1296	120	mA	
I_{DD5F4}	960	88	960	88	976	88	mA	
I_{DD6N}	104	32	104	32	104	32	mA	
I_{DD6E}	160	32	160	32	160	32	mA	
I_{DD6R}	80	32	80	32	80	32	mA	
I_{DD6A}	104	32	104	32	104	32	mA	
I_{DD7}	1168	72	1168	72	1184	72	mA	
I_{DD8}	52	16	52	16	52	16	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-actived rank(IDLE) is IDD2N. Please refer to Table21.
2. IDD current measure method and detail patterns are described on DDR4 component datasheet.
3. VDD and VDDQ are merged on module PCB (IDDQ values are not considered by Qoff condition)
4. DIMM IDD Values are calculated based on the component IDD spec and Register power.

[Table 21] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
I_{DD0}	I_{DD0}	I_{DD2N}
I_{DD1}	I_{DD1}	I_{DD2N}
I_{DD2P}	I_{DD2P}	I_{DD2P}
I_{DD2N}	I_{DD2N}	I_{DD2N}
I_{DD2Q}	I_{DD2Q}	I_{DD2Q}
I_{DD3P}	I_{DD3P}	I_{DD3P}
I_{DD3N}	I_{DD3N}	I_{DD3N}
I_{DD4R}	I_{DD4R}	I_{DD2N}
I_{DD4W}	I_{DD4W}	I_{DD2N}
I_{DD5B}	I_{DD5B}	I_{DD2N}
I_{DD6}	I_{DD6}	I_{DD6}
I_{DD7}	I_{DD7}	I_{DD2N}
I_{DD8}	I_{DD8}	I_{DD8}

13. Input/Output Capacitance

[Table 22] Silicon Pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	1,3,4
C_{I}	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

NOTE:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM_n, DQS_T, DQS_c, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_c)
6. CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_c))
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case C_{TEN} might not be valid and system shall verify TEN signal with Vendor specific information.

14. Electrical Characterisitics and AC Timing

14.1 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

[Table 23] DDR4-1600 Speed Bins and Operations

Speed Bin				DDR4-1600		Unit	NOTE
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75[12] (13.50)[5,10]	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	10
ACT to internal read or write delay time			tRCD	13.75 (13.50)[5,10]	-	ns	10
PRE command period			tRP	13.75 (13.50)[5,10]	-	ns	10
ACT to PRE command period			tRAS	35	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	48.75 (48.50)[5,10]	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5	1.6	ns	1,2,3,4,10,13
				(Optional)[5,10]		ns	
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				9,11,12		nCK	12,13
Supported CL Settings with read DBI				11,13,14		nCK	12
Supported CWL Settings				9,11		nCK	

[Table 24] DDR4-1866 Speed Bins and Operations

Speed Bin				DDR4-1866		Unit	NOTE
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.92[12] (13.50)[5,10]	18.00	ns	11
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	11
ACT to internal read or write delay time			tRCD	13.92[12] (13.50)[5,10]	-	ns	11
PRE command period			tRP	13.92[12] (13.50)[5,10]	-	ns	11
ACT to PRE command period			tRAS	34	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	47.92 (47.50)[5,10]	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional)[5,10]	1.6	ns	1,2,3,4,10,12
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional)[5,10]	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings				9,11,12,13,14		nCK	11,12
Supported CL Settings with read DBI				11,13,14,15,16		nCK	11
Supported CWL Settings				9,10,11,12		nCK	

[Table 25] DDR4-2133 Speed Bins and Operations

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.06[12] (13.75)[5,10]	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10
ACT to internal read or write delay time			tRCD	14.06[12] (13.75)[5,10]	-	ns	10
PRE command period			tRP	14.06 (13.75)[5,10]	-	ns	10
ACT to PRE command period			tRAS	33	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	47.06 (46.75)[5,10]	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional)[5,10]	1.6	ns	1,2,3,4,9,11 2
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,9
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional)[5,11]	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071 (Optional)[5,10]	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings				9,11.12,13,14,15,16		nCK	11,12
Supported CL Settings with read DBI				11,13,14,15,16,18,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

[Table 26] DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400		Unit	NOTE
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.16 (13.75)[5,10]	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10
ACT to internal read or write delay time			tRCD	14.16 (13.75)[5,10]	-	ns	10
PRE command period			tRP	14.16 (13.75)[5,10]	-	ns	10
ACT to PRE command period			tRAS	32	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	46.16 (45.75)[5,10]	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
				(Optional)[5,10]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
				(Optional)[5,10]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
				(Optional)[5,10]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18		nCK	12
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		nCK	

14.2 Speed Bin Table Note

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133,2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section "Rounding Algorithms".
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
9. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
10. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
11. CL number in parentheses, it means that these numbers are optional.
12. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
13. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

15. Timing Parameters by Speed Grade

[Table 27] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2400

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot tCK(avg)m ax + tJIT(per)max_tot								tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	^{t}ERR(nper)min = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total min) ^{t}ERR(nper)max = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total max)								ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps	
Command and Address Timing											
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.625 ns)	-	max(5 nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6 ns)	-	Max(4nCK,5 .3ns)	-	Max(4nCK,5 .3ns)	-	Max(4nCK,5 .3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5 ns)		Max(4nCK,4 .2ns)		Max(4nCK,3 .7ns)		Max(4nCK,3 .3ns)	-	nCK	34

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5 ns)		Max(4nCK,4 .2ns)		Max(4nCK,3 .7ns)		Max(4nCK,3 .3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7. 5ns)		Max(4nCK,6 .4ns)		Max(4nCK,6 .4ns)		Max(4nCK,6 .4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6 ns)		Max(4nCK,5 .3ns)		Max(4nCK,5 .3ns)		Max(4nCK,4 .9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6 ns)		Max(4nCK,5 .3ns)		Max(4nCK,5 .3ns)		Max(4nCK,4 .9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 35ns)		Max(28nCK, 30ns)		Max(28nCK, 30ns)		Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 25ns)		Max(20nCK, 23ns)		Max(20nCK, 21ns)		Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 20ns)		Max(16nCK, 17ns)		Max(16nCK, 15ns)		Max(16nCK, 13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2. 5ns)	-	max(2nCK,2 .5ns)	-	max(2nCK,2 .5ns)	-	max (2nCK, 2.5ns)	-		1,2,e,3 4
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7. 5ns)	-	max(4nCK,7 .5ns)	-	max(4nCK,7 .5ns)	-	max (4nCK,7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7. 5ns)	-	max(4nCK,7 .5ns)	-	max(4nCK,7 .5ns)	-	max (4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (4nCK,3.75n s)	-	tWR+max (5nCK,3.75n s)	-	tWR+max (5nCK,3.75n s)	-	tWR+max (5nCK,3.75n s)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+ma x (4nCK,3.75n s)	-	tWTR_S+ma x (5nCK,3.75n s)	-	tWTR_S+ma x (5nCK,3.75n s)	-	tWTR_S+ma x (5nCK,3.75n s)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+ma x (4nCK,3.75n s)	-	tWTR_L+ma x (5nCK,3.75n s)	-	tWTR_L+ma x (5nCK,3.75n s)	-	tWTR_L+ma x (5nCK,3.75n s)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-		50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-		
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	5	-	nCK	
Mode Register Se commandt cycle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL		tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL		tMOD+ tCAL	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.16	tCK(avg)/ 2	13,18,3 9,49
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	tCK(avg)/ 2	13,17,1 8,39,49
Data Valid Window per device: (tQH - tD-QSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	UI	17,18,3 9,49
Data Valid Window per pin per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	UI	17,18,3 9,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-390	180	-330	175	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	ps	39
Data Strobe Timing											
DQS_t, DQS_c differential READ Pre-am-ble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE 44	tCK	39,40

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ Pre-amble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	NOTE 44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Pre-amble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Pre-amble (2 clock preamble)	tWPRE2	NA		NA		NA		1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	-175	175	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		370		330		310		290	ps	37,38,39
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-		
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max (5nCK,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max (5nCK,10ns)	-	nCK	
Power Down Timing											
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		nCK	
ODT Timing											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		4		5		nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CRC Error Reporting											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
Geardown timing											
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	-	-	-	-	-	-		
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-		
MRS command to Sync pulse time(T3)	tSYNC_GEAR	-	-	-	-	-	-	-	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	-	-	-	-	-	-	-	-		27
Geardown setup time	tGEAR_setup	-	-	-	-	-	-	-	-	nCK	
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	nCK	
tREFI											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	ns	34

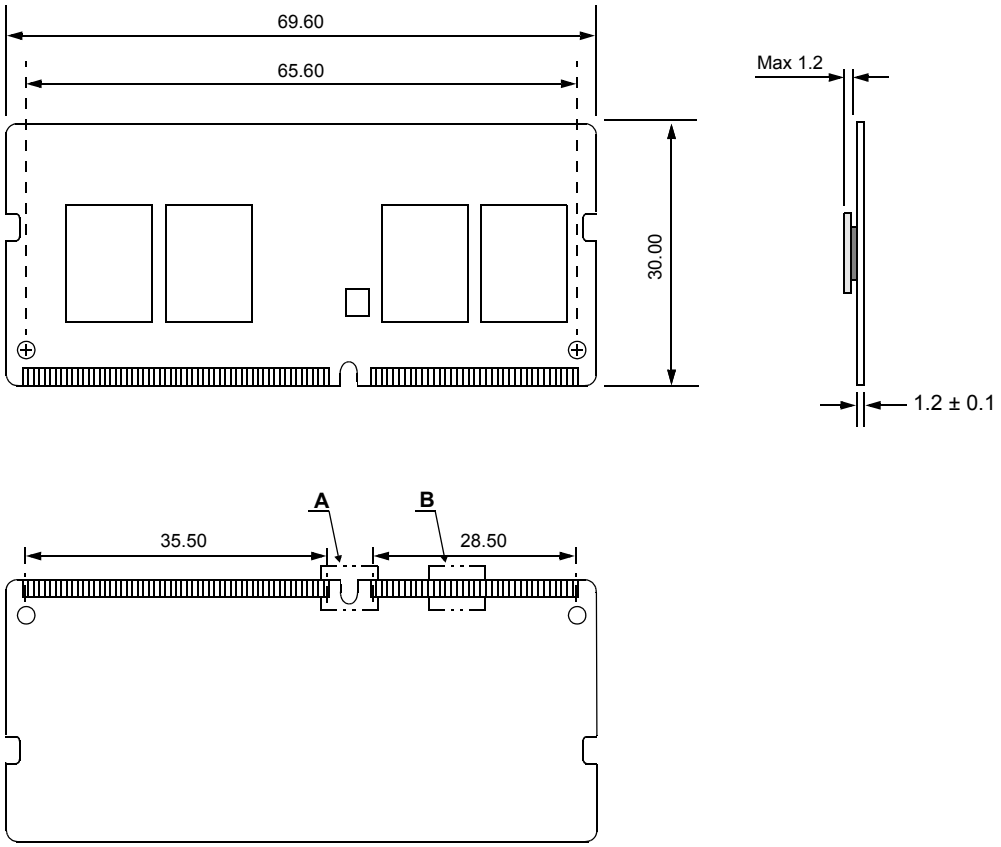
NOTE :

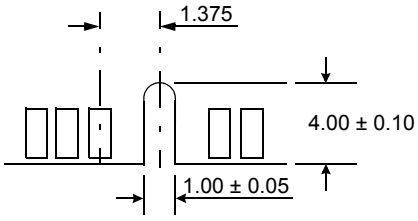
1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables .
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
    UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7 RONNOM = 34 ohms
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ .
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

16. Physical Dimensions

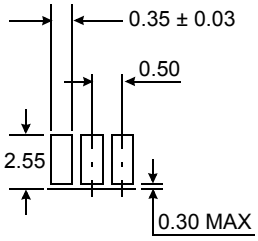
16.1 256Mx16 based 256Mx64 Module (1 Rank) - M471A5644EB0

Units : Millimeters





Detail A



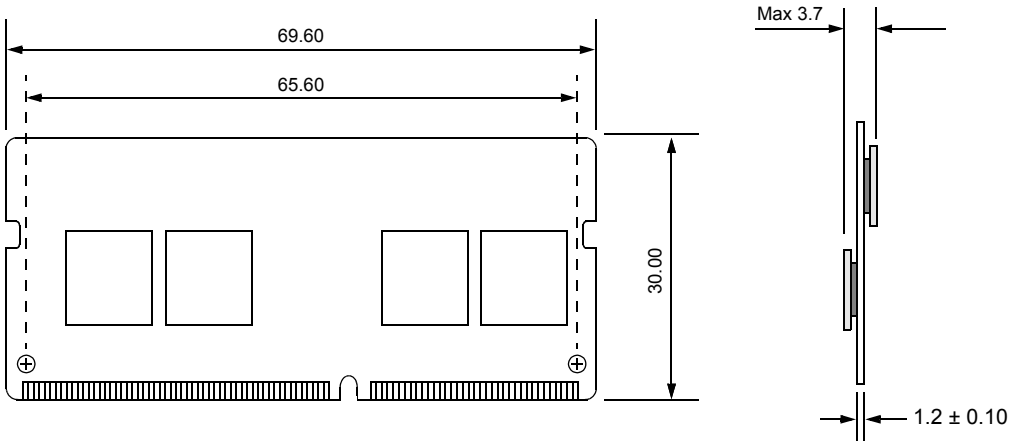
Detail B

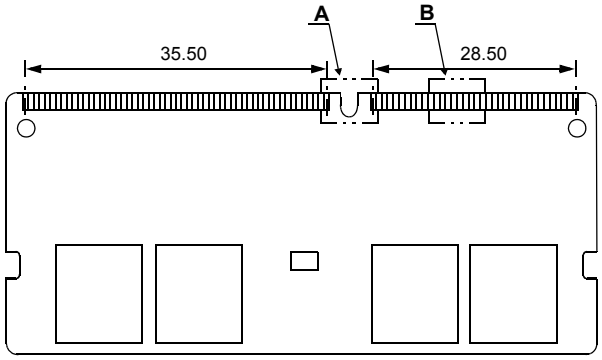
The used device is 256M x16 DDR4 SDRAM, Flip-Chip.
DDR4 SDRAM Part NO : K4A4G165WE - BC**

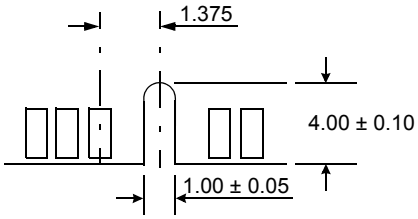
* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.

16.2 512Mx8 based 512Mx64 2133Mbps Module (1 Rank,A0) - M471A5143EB0

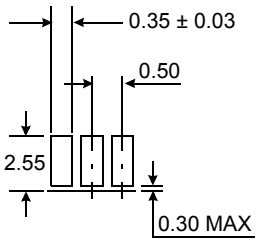
Units : Millimeters







Detail A



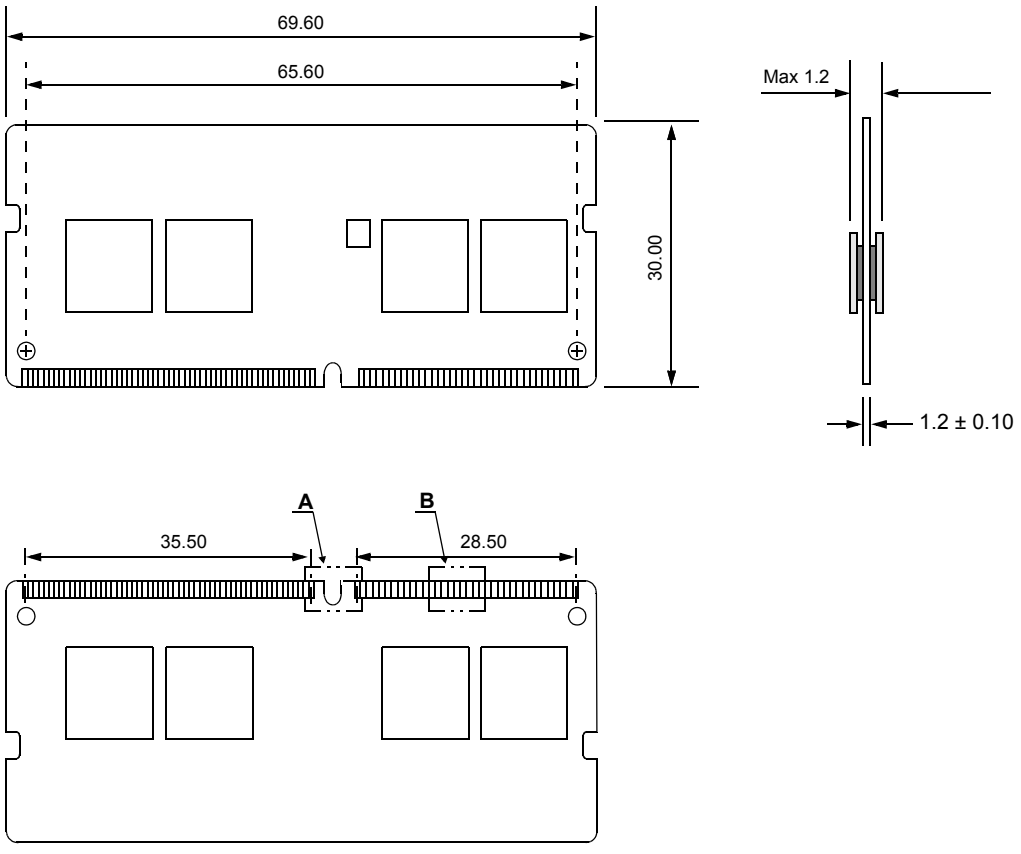
Detail B

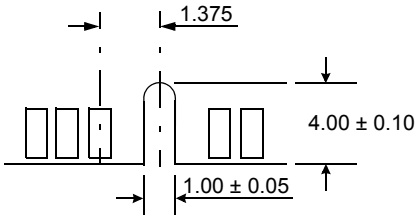
The used device is 512M x8 DDR4 SDRAM, Flip-Chip.
DDR4 SDRAM Part NO : K4A4G085WE - BCPB

* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.

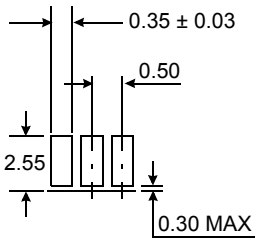
16.3 512Mx8 based 512Mx64 2133/2400Mbps Module (1 Rank,A1) - M471A5143EB1

Units : Millimeters





Detail A



Detail B

The used device is 512M x8 DDR4 SDRAM, Flip-Chip.
DDR4 SDRAM Part NO : K4A4G085WE - BCRC

* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.