

SMPS MOSFET

IRLR8203PbF
IRLU8203PbF

HEXFET® Power MOSFET

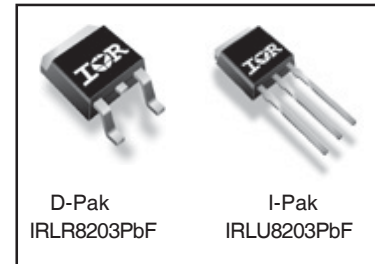
Applications

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Computer Processor Power
- Lead-Free

V_{DSS}	R_{DS(on)} max	I_D
30V	6.8mΩ	110A^④

Benefits

- Ultra-Low Gate Impedance
- Very Low RDS(on) at 4.5V V_{GS}
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	110 ^④	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	76 ^④	
I _{DM}	Pulsed Drain Current ^①	120	
P _D @ T _C = 25°C	Maximum Power Dissipation ^③	140	W
P _D @ T _C = 100°C	Maximum Power Dissipation ^③	69	W
	Linear Derating Factor	0.92	W/°C
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	1.09	°C/W
R _{θJA}	Junction-to-Ambient (PCB mount)*	—	50	
R _{θJA}	Junction-to-Ambient	—	110	

* When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

Notes ^① through ^④ are on page 10

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.027	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	5.6	6.8	mΩ	V _{GS} = 10V, I _D = 15A ③
		—	7.1	9.0		V _{GS} = 4.5V, I _D = 12A ③
V _{GS(th)}	Gate Threshold Voltage	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	100		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V

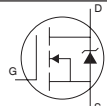
Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	35	—	—	S	V _{DS} = 15V, I _D = 12A
Q _g	Total Gate Charge	—	33	50	nC	I _D = 12A
Q _{gs}	Gate-to-Source Charge	—	5.7	8.5		V _{DS} = 24V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	17	25		V _{GS} = 4.5V ③
Q _{oss}	Output Gate Charge	—	23	34		V _{GS} = 0V, V _{DS} = 10V
t _{d(on)}	Turn-On Delay Time	—	15	—	ns	V _{DD} = 15V
t _r	Rise Time	—	99	—		I _D = 12A
t _{d(off)}	Turn-Off Delay Time	—	30	—		R _G = 6.8Ω
t _f	Fall Time	—	69	—		V _{GS} = 4.5V ③
C _{iss}	Input Capacitance	—	2430	—		V _{GS} = 0V
C _{oss}	Output Capacitance	—	1200	—	V _{DS} = 15V	
C _{rss}	Reverse Transfer Capacitance	—	250	—	pF	f = 1.0MHz

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	310	mJ
I _{AR}	Avalanche Current①	—	30	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	110④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	120		
V _{SD}	Diode Forward Voltage	—	0.75	1.3	V	T _J = 25°C, I _S = 12A, V _{GS} = 0V ③
		—	0.65	—		T _J = 125°C, I _S = 12A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	48	72	ns	T _J = 25°C, I _F = 12A, V _R = 15V
Q _{rr}	Reverse Recovery Charge	—	62	92	nC	di/dt = 100A/μs ③
t _{rr}	Reverse Recovery Time	—	49	74	ns	T _J = 125°C, I _F = 12A, V _R = 15V
Q _{rr}	Reverse Recovery Charge	—	67	100	nC	di/dt = 100A/μs ③

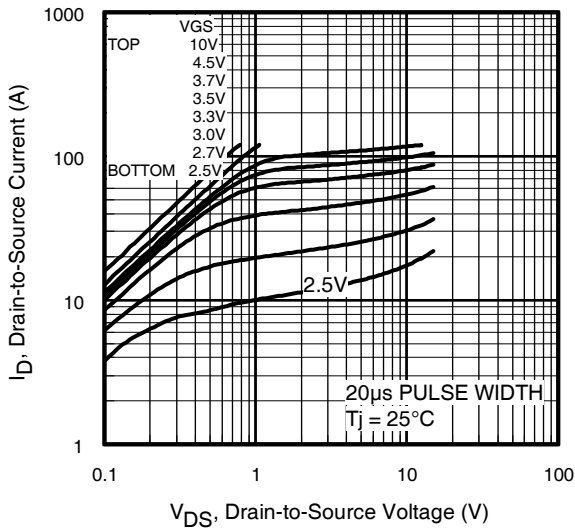


Fig 1. Typical Output Characteristics

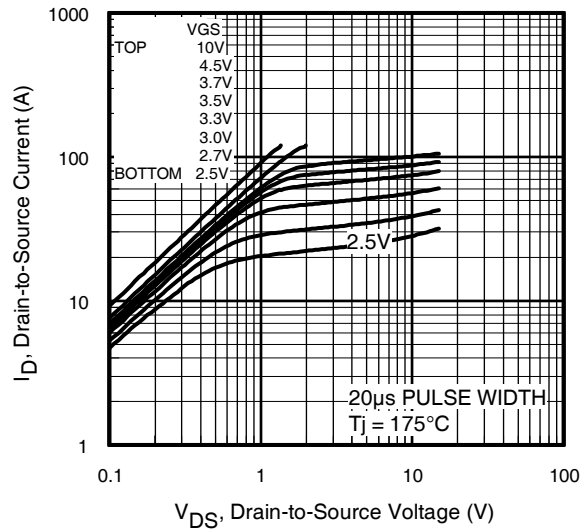


Fig 2. Typical Output Characteristics

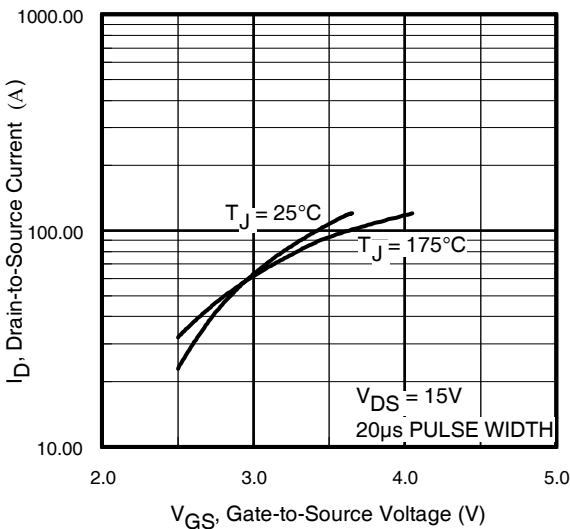


Fig 3. Typical Transfer Characteristics

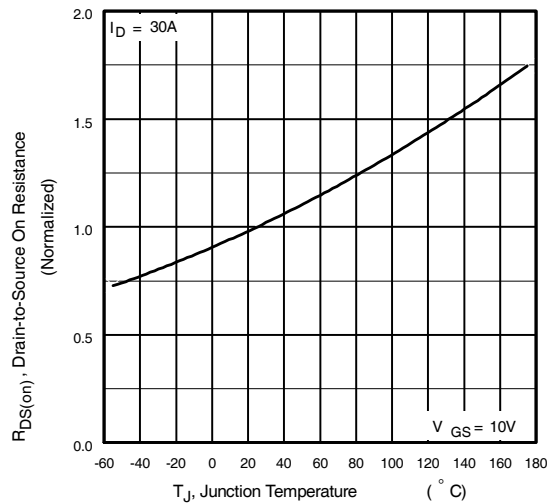


Fig 4. Normalized On-Resistance Vs. Temperature

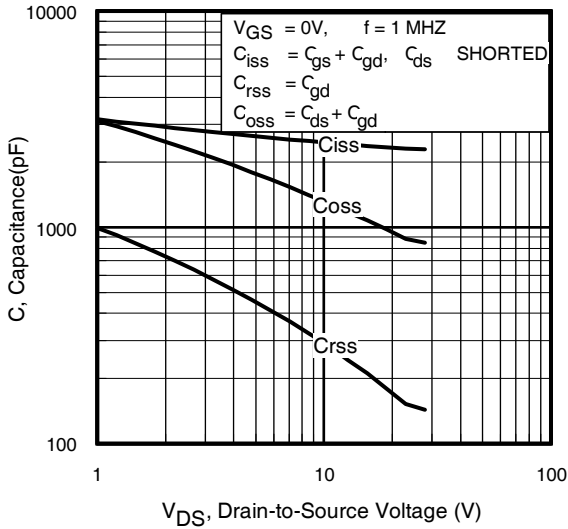


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

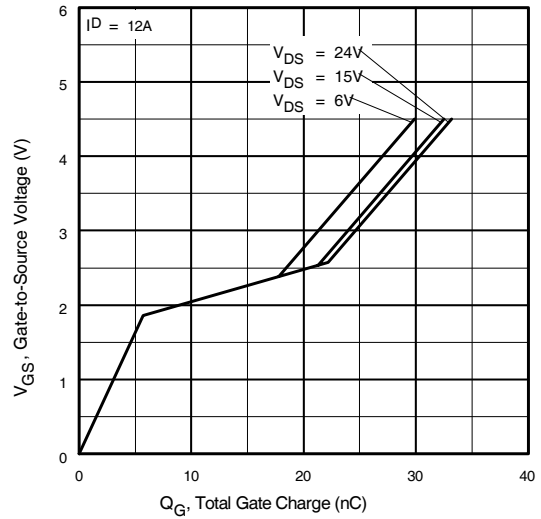


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

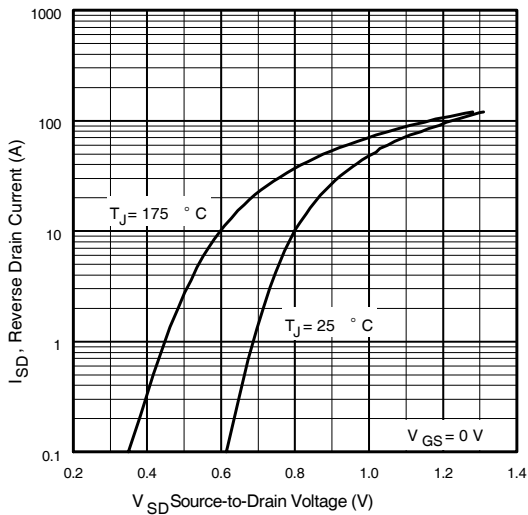


Fig 7. Typical Source-Drain Diode Forward Voltage

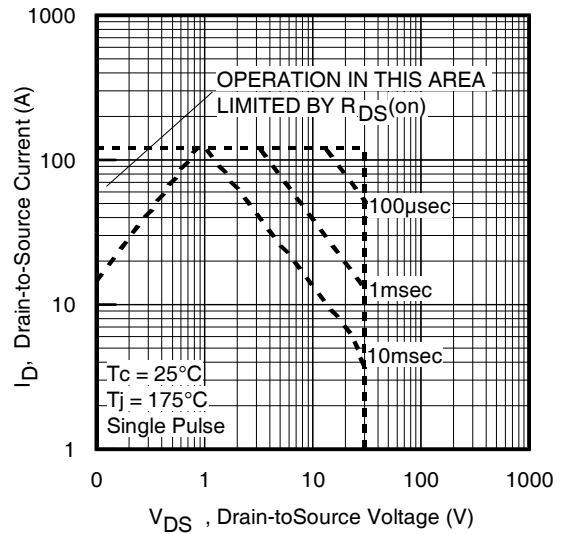


Fig 8. Maximum Safe Operating Area

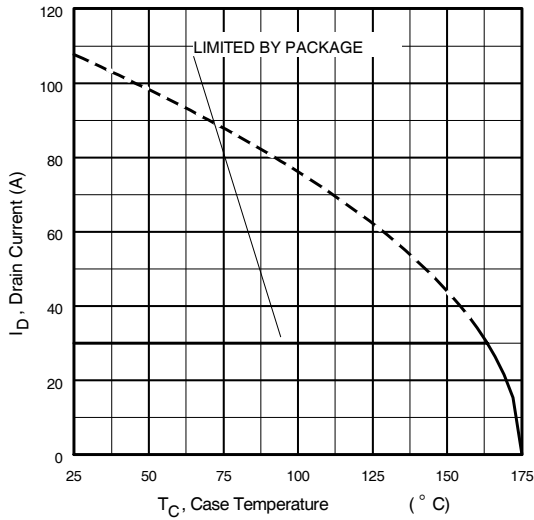


Fig 9. Maximum Drain Current Vs. Case Temperature

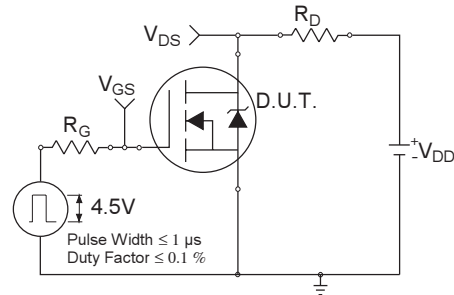


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

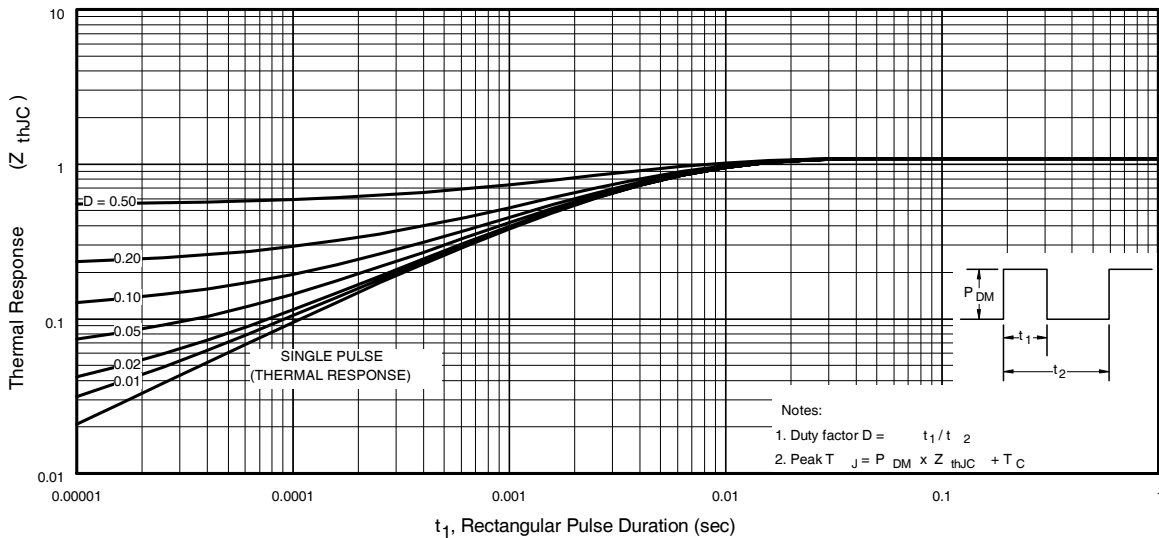


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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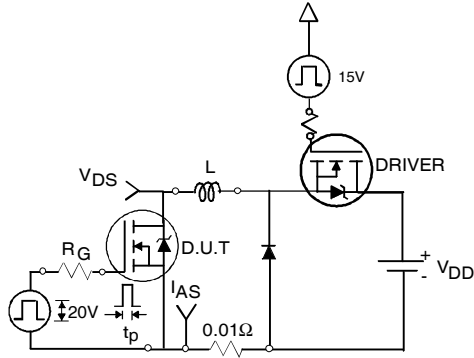


Fig 12a. Unclamped Inductive Test Circuit

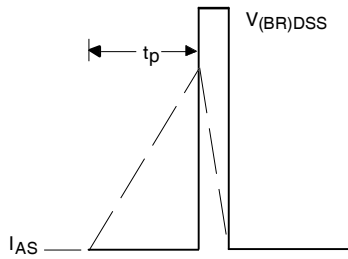


Fig 12b. Unclamped Inductive Waveforms

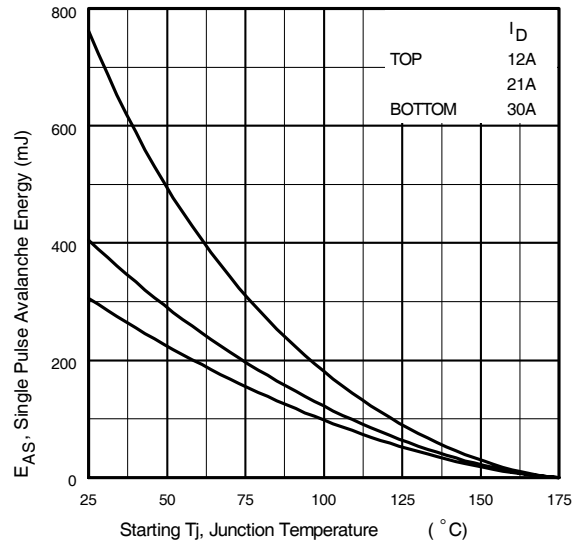


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

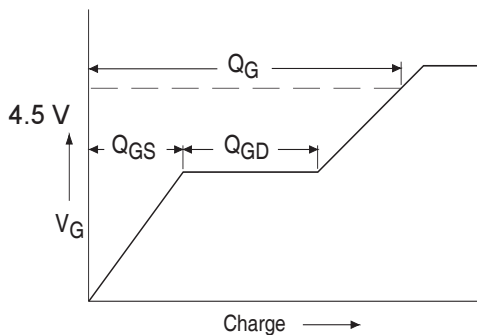


Fig 13a. Basic Gate Charge Waveform

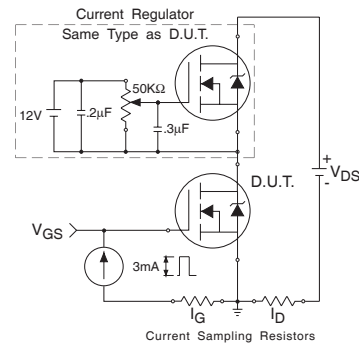
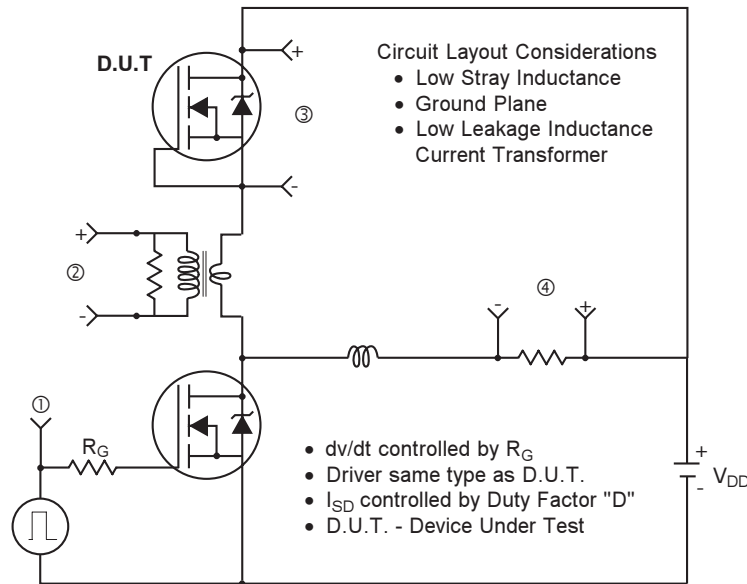


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

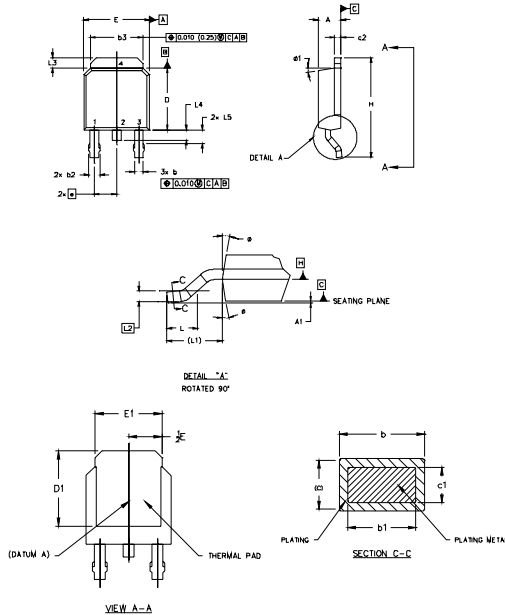
Fig 14. For N-Channel HEXFET® Power MOSFETs

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D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:
 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M-1994.
 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
 3.0 LEAD DIMENSION UNCONTROLLED IN L5.
 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.254] FROM THE LEAD TIP.
 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" [0.127] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

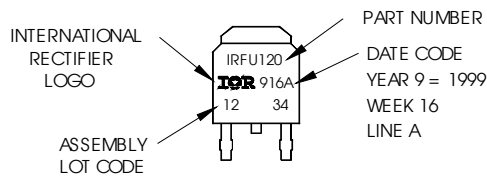
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.28	.086	.091	
A1	0.15	0.15	.005	.005	
b	0.64	0.68	.025	.026	5
b1	0.64	0.78	.025	.031	5
b2	0.76	1.04	.030	.041	
b3	4.76	5.46	.190	.215	
c	0.46	0.50	.018	.020	3
c1	0.41	0.56	.016	.022	5
c2	.346	0.89	.018	.035	5
D	1.87	6.37	.735	.251	6
D1	5.31	-	.209	-	4
E	4.36	6.73	.172	.265	6
E1	4.32	-	.170	-	4
e	2.28	-	.090 BSC	-	
H	8.40	10.41	.330	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.	-	.108 REF.	-	
L2	0.051 BSC	-	.020 BSC	-	
L3	0.89	1.27	.035	.050	
L4	1.14	1.52	.045	.060	
L5	1.14	1.52	.045	.060	
ø	0"	10"	0"	10"	
ø1	0"	10"	0"	10"	

LEAD ASSIGNMENTS
 HEXFET
 1.- GATE
 2.- DRAIN
 3.- SOURCE
 4.- DRAIN
 IGBTs, CO-PAK
 1.- GATE
 2.- COLLECTOR
 3.- EMITTER
 4.- COLLECTOR

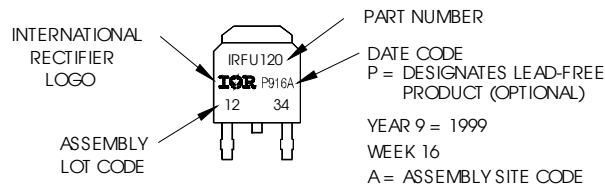
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 1234
 ASSEMBLED ON WW 16, 1999
 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"



OR

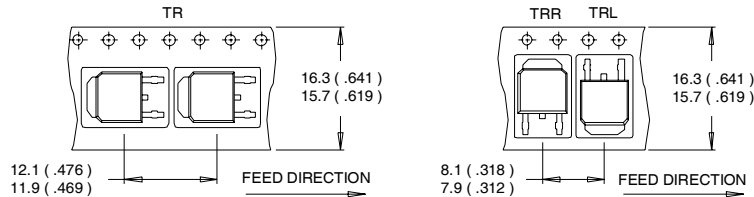


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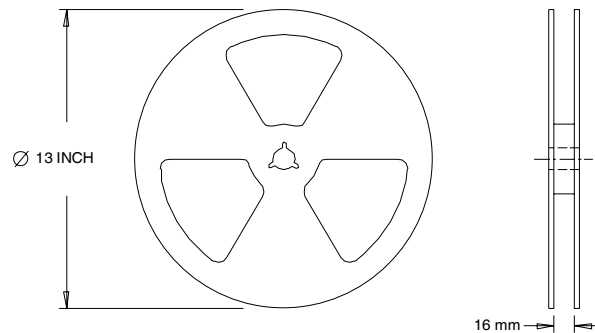
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D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.68\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 30\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>