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NCP729

200 mA Ultra-Low Noise Very-Low Iq, High PSRR, LDO Linear Voltage Regulator

The NCP729 is a 200 mA LDO suitable to provide clean analog power supply rails for noise sensitive applications. This device features Ultra−Low Noise performance, High Power Supply Rejection Ratio and Very good transient response characteristics. Very Low Dropout and Very Low Quiescent Current makes this LDO an attractive choice for wide range of battery powered, portable products. Current Limit and Thermal Shutdown provide protection during failure conditions. NCP729 is available in 1.06 mm x 1.06 mm Chip Scale Package and it is stable with small 1 μF Ceramic capacitors.

Features

- Operating Input Voltage Range: 2.0 V to 5.5 V
- Fixed Voltage Options Available: 0.8 V to 3.5 V
- Very Low Quiescent Current: Max. 50 μA over Temperature
- Ultra Low Noise: 10 μV_{RMS} from 100 Hz to 100 kHz
- Very Low Dropout: 86 mV Typical at 200 mA
- ±2% Accuracy over Full Load, Line and Temperature Variations
- High PSRR: 72 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Available in 1.06 mm x 1.06 mm 4−bump CSP Package
- Active Output Discharge for Fast Turn−Off
- These are Pb−free Devices

Typical Applications

- PDAs, Tablets, GPS, Smartphones
- Wireless Handsets, Wireless LAN, Bluetooth, Zigbee
- Portable Medical Equipment
- Other Battery Powered Applications

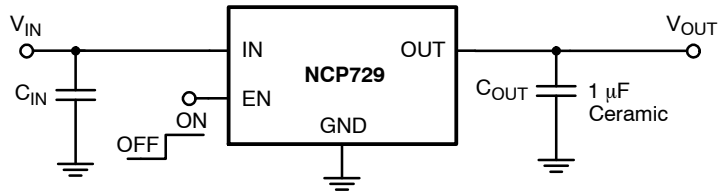

Figure 1. Typical Application Schematic

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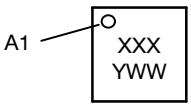
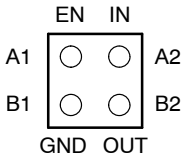
4 BUMP CSP
FC SUFFIX
CASE 568AD

DEVICE MARKING INFORMATION



XXX = Specific Device Code
Y = Year
WW = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

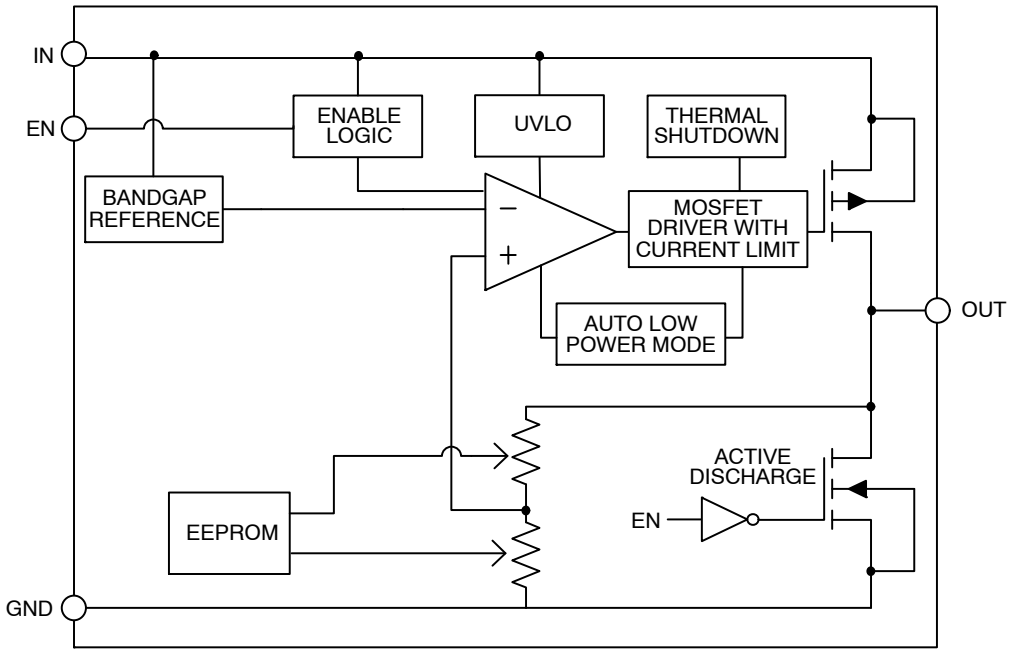


Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. 4−bump CSP	Pin Name	Description
B2	OUT	Regulated output voltage pin. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
B1	GND	Power supply ground. Soldered to large copper plane allows for better heat dissipation.
A1	EN	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
A2	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6 V	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V	V
Enable Input	V_{EN}	−0.3 V to V_{IN} + 0.3 V	V
Output Short Circuit Duration	t_{SC}	∞	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, 4−bump CSP package Thermal Resistance, Junction−to−Air (Note 3) Thermal Resistance, Junction−to−Air (Note 4)	$R_{\theta JA}$	 90 157	°C/W

3. Specified according to JEDEC 51.7 4−Layer Board.
4. Single component mounted on 4−Layer Board, 480 mm^2, Top Layer thickness: 1 oz, Cu Area: 100 mm^2.

Table 4. ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 0.3$ V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, $C_{IN} = C_{OUT}$ = 1 μF unless otherwise noted. Typical values are at T_J = +25°C. (Note 5)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	2.0		5.5	V
Output Voltage Accuracy	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 5.5 V 0 mA ≤ I_{OUT} ≤ 200 mA		V_{OUT}	−2		+2	%
Line Regulation	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 5.5 V		Reg_{LINE}		150		μV/V
Load Regulation	I_{OUT} = 0 mA to 200 mA		Reg_{LOAD}		2		μV/mA
Dropout Voltage (Note 6)	$V_{DO} = V_{IN} - (V_{OUT(NOM)} - 100$ mV) I_{OUT} = 200 mA	V_{OUT} = 1.8 V V_{OUT} = 2.5 V V_{OUT} = 2.6 V V_{OUT} = 2.8 V V_{OUT} = 2.85 V V_{OUT} = 3.0 V V_{OUT} = 3.3 V	V_{DO}		170 100 90 80 80 70 65	220 140 130 120 120 110 100	mV
Quiescent Current	I_{OUT} = 0 mA		I_Q		35	50	μA
Ground Current	I_{OUT} = 200 mA	V_{OUT} < 1.8 V V_{OUT} ≥ 1.8 V	I_{GND}		255 155	300 200	μA
Disable Current	V_{EN} = 0 V		I_{DIS}		0.3	1	μA
Output Current Limit	$V_{OUT} = V_{OUT(NOM)} - 100$ mV		I_{OUT}	250	400	530	mA
Output Short Circuit Current	V_{OUT} = 0 V		I_{SC}	250	400	530	mA
EN Pin Threshold Voltage High Threshold Low Threshold	 V_{EN} Voltage increasing V_{EN} Voltage decreasing		 V_{EN_HI} V_{EN_LO}	 0.9		 0.4	V
EN Pin Input Current	V_{EN} = 5.5 V		I_{EN}		100	500	nA
Turn−on Time	V_{OUT} = 0 V to 98% $V_{OUT(NOM)}$, after assertion of the EN		t_{ON}		150		μs
Power Supply Rejection Ratio	V_{IN} = 3.8 V, V_{OUT} = 3.3 V V_{PP} = 100 mV I_{OUT} = 200 mA	f = 100 Hz f = 1 kHz f = 10 kHz	PSRR		74 72 56		dB
Output Noise Voltage	V_{OUT} = 1.8 V, I_{OUT} = 200 mA f = 100 Hz to 100 kHz		V_N		10		μV_{rms}
Line Transient	V_{OUT} + 0.3 V ≤ V_{IN} ≤ V_{OUT} + 1.3 V or V_{OUT} + 0.3 V ≤ V_{IN} ≤ V_{OUT} + 1.3 V in 1 μs				±20		mV
Load Transient	I_{OUT} = 1 mA to 200 mA or I_{OUT} = 200 mA to 1 mA in 1 μs		ΔV_{OUT}		±80		mV
Undervoltage Lock−out	V_{IN} rising from 0 V to 5.5 V		UVLO	1.3	1.6	1.9	V
Thermal Shutdown Temperature	Temperature increasing from T_J = +25°C		T_{SD}		165		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}	−	20	−	°C

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. Characterized when V_{OUT} falls 100 mV below the regulated voltage at $V_{IN} = V_{OUT(NOM)} + 0.3$ V.

TYPICAL CHARACTERISTICS

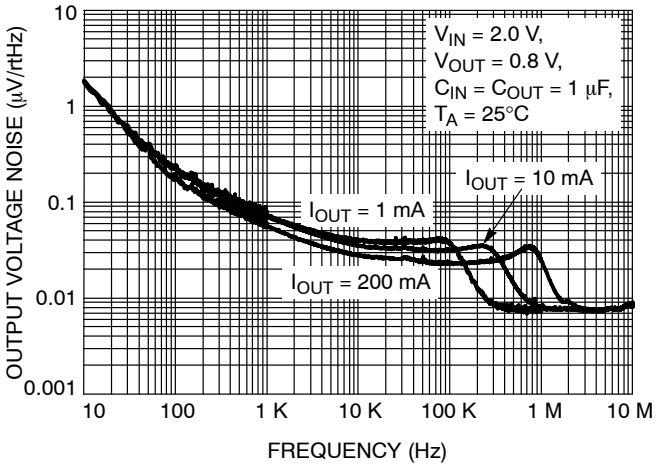


Figure 3. Output Voltage Noise, V_{OUT} = 0.8 V, C_{OUT} = 1 μF

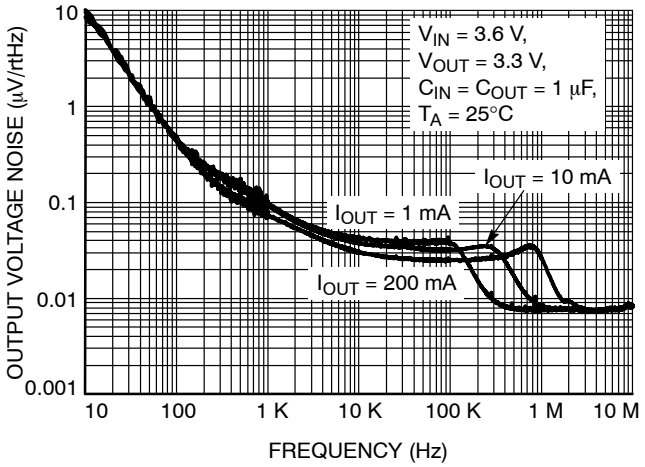


Figure 4. Output Voltage Noise, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

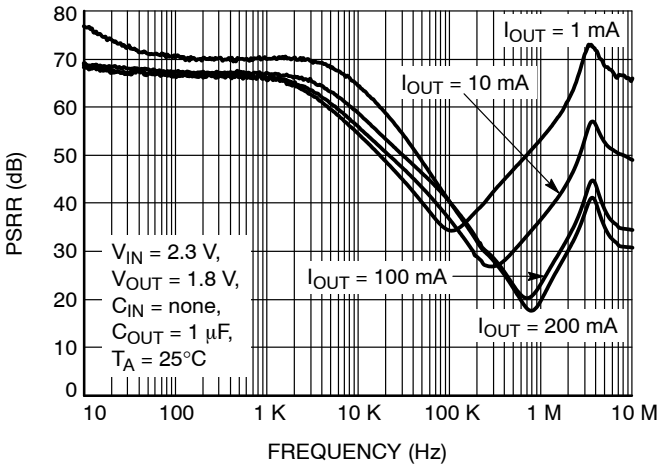


Figure 5. PSRR, V_{OUT} = 1.8 V, C_{OUT} = 1 μF

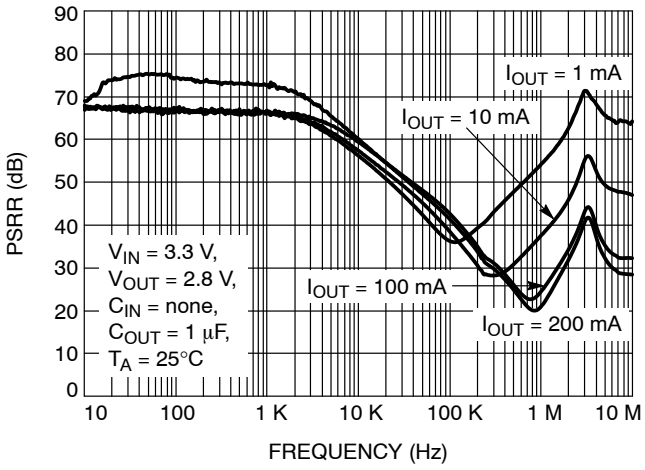


Figure 6. PSRR, V_{OUT} = 2.8 V, C_{OUT} = 1 μF

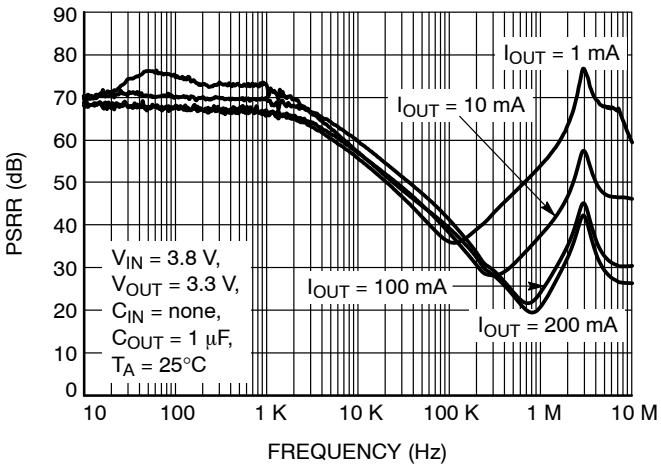


Figure 7. PSRR, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

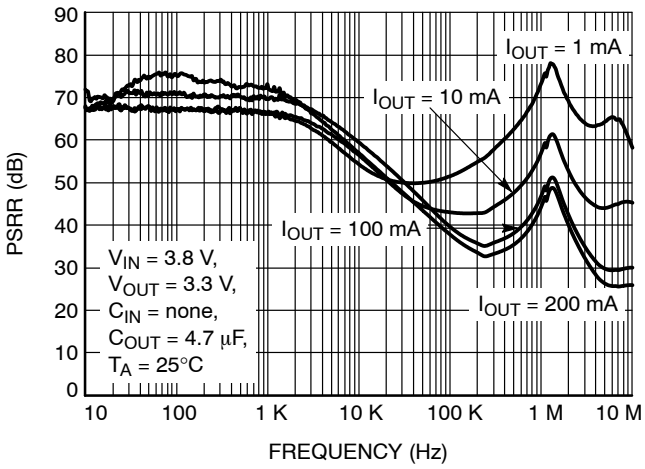


Figure 8. PSRR, V_{OUT} = 3.3 V, C_{OUT} = 4.7 μF

TYPICAL CHARACTERISTICS

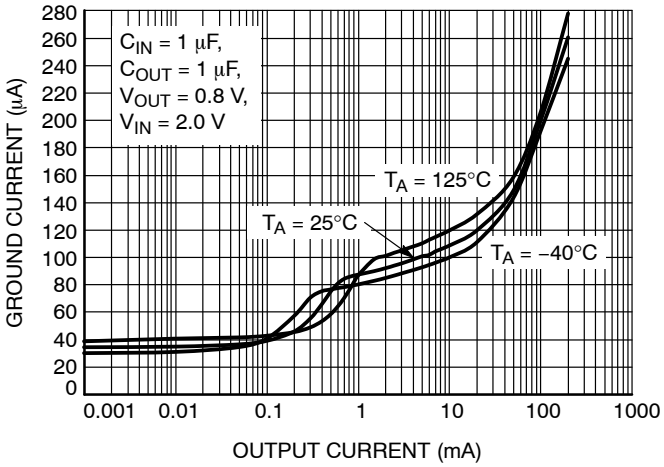


Figure 9. Ground Current vs. Output Current, V_{OUT} = 0.8 V

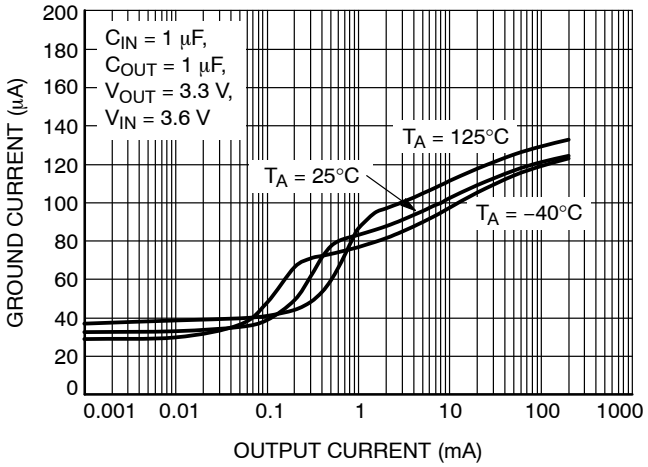


Figure 10. Ground Current vs. Output Current, V_{OUT} = 3.3 V

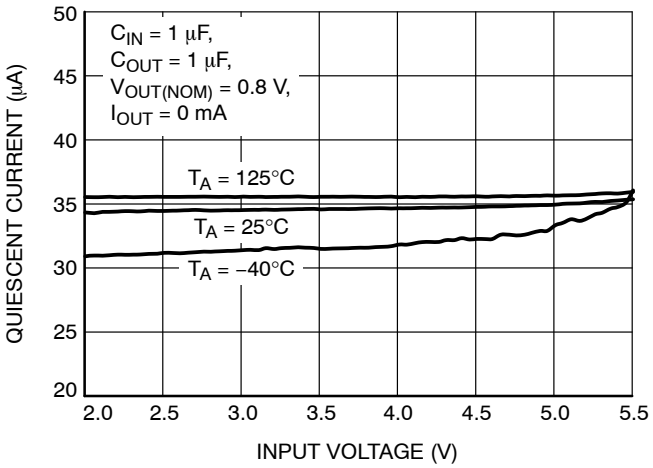


Figure 11. Quiescent Current vs. Input Voltage, V_{OUT} = 0.8 V

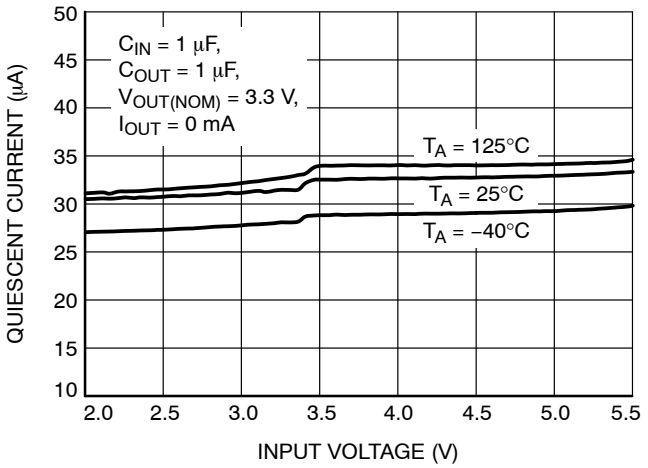


Figure 12. Quiescent Current vs. Input Voltage, V_{OUT} = 3.3 V

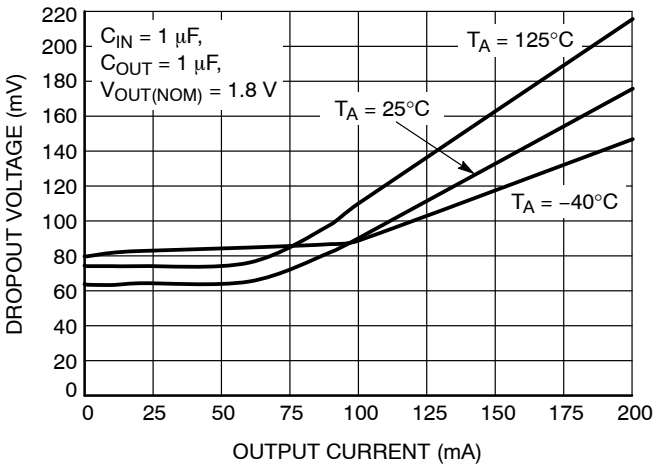


Figure 13. Dropout Voltage vs. Output Current, V_{OUT} = 1.8 V

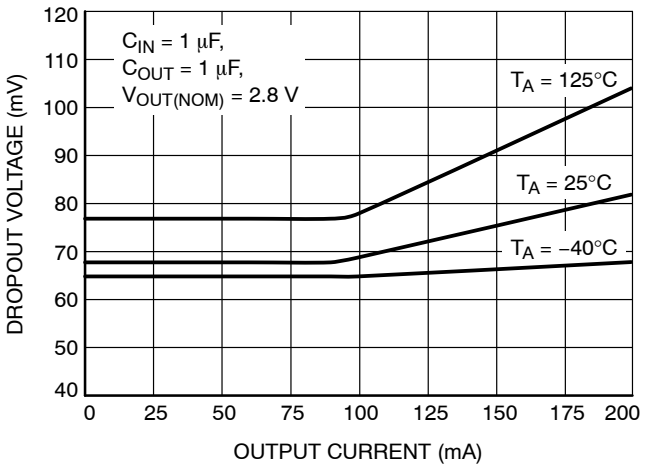


Figure 14. Dropout Voltage vs. Output Current, V_{OUT} = 2.8 V

TYPICAL CHARACTERISTICS

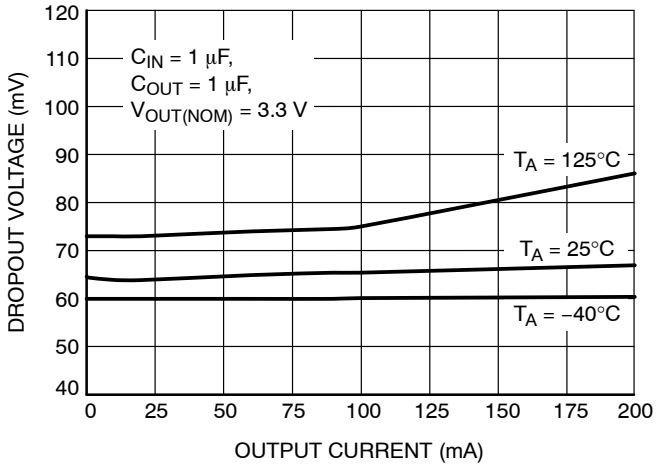


Figure 15. Dropout Voltage vs. Output Current, V_{OUT} = 3.3 V

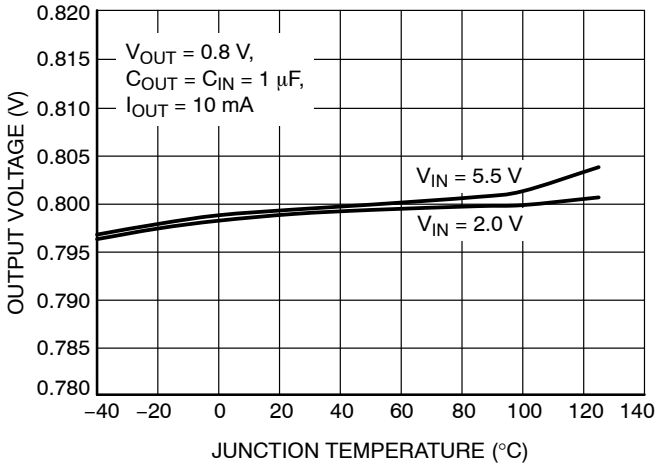


Figure 16. Output Voltage vs. Temperature, V_{OUT} = 0.8 V

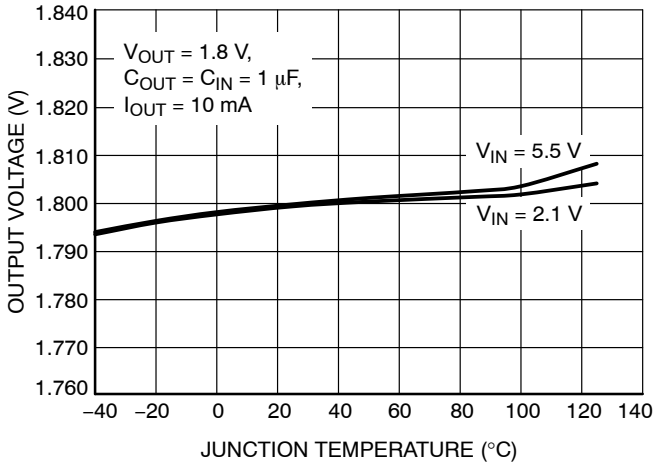


Figure 17. Output Voltage vs. Temperature, V_{OUT} = 1.8 V

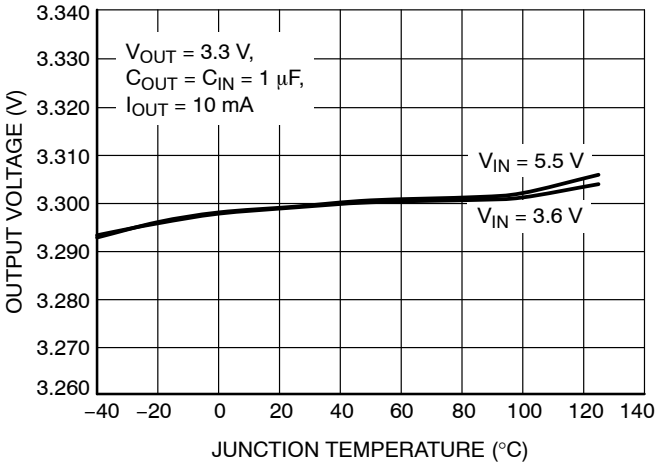


Figure 18. Output Voltage vs. Temperature, V_{OUT} = 3.3 V

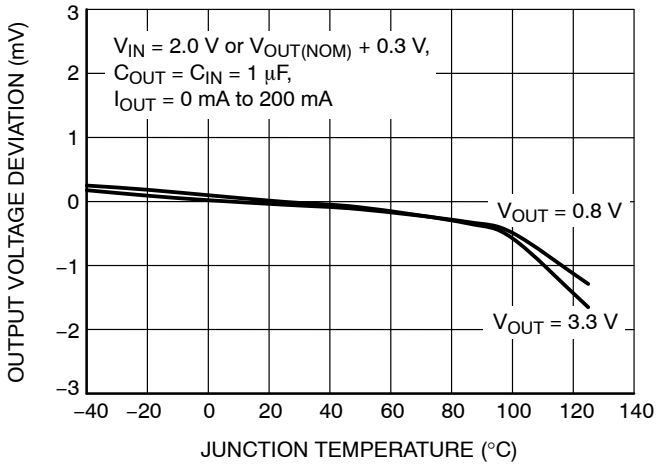


Figure 19. Load Regulation vs. Temperature

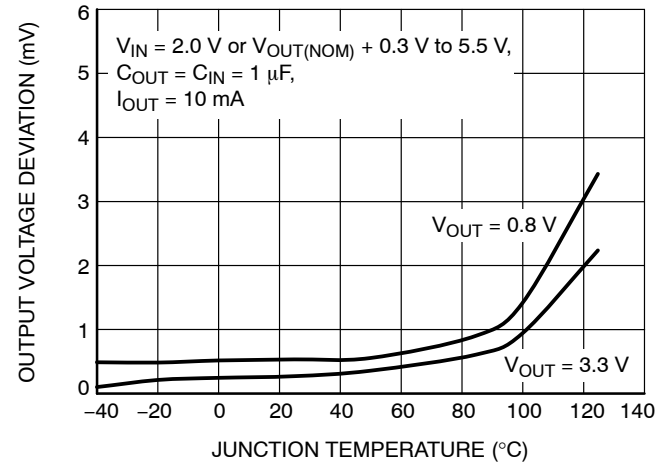


Figure 20. Line Regulation vs. Temperature

TYPICAL CHARACTERISTICS

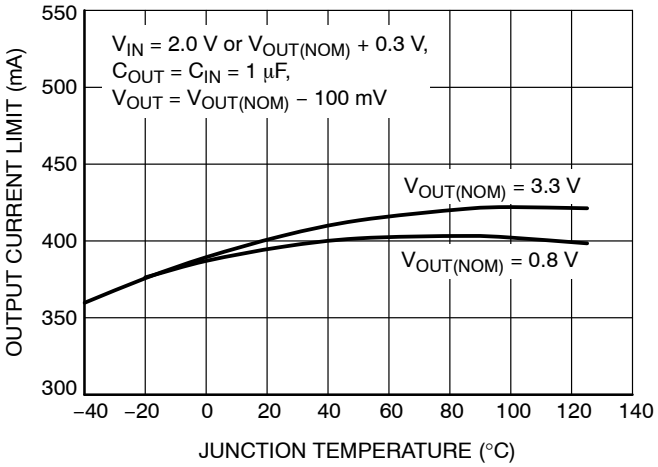


Figure 21. Output Current Limit vs. Temperature

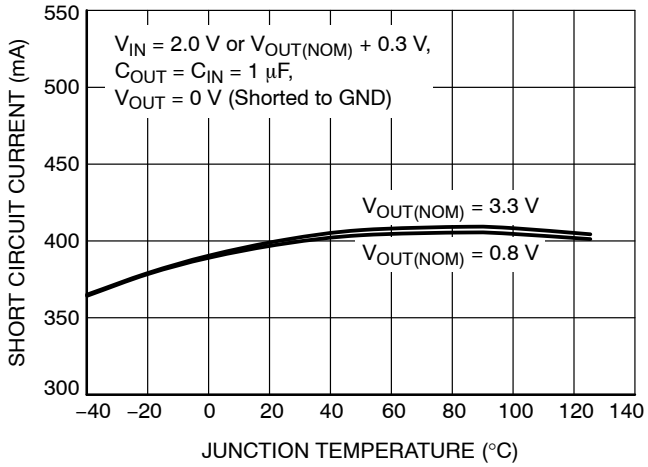


Figure 22. Short Circuit Current vs. Temperature

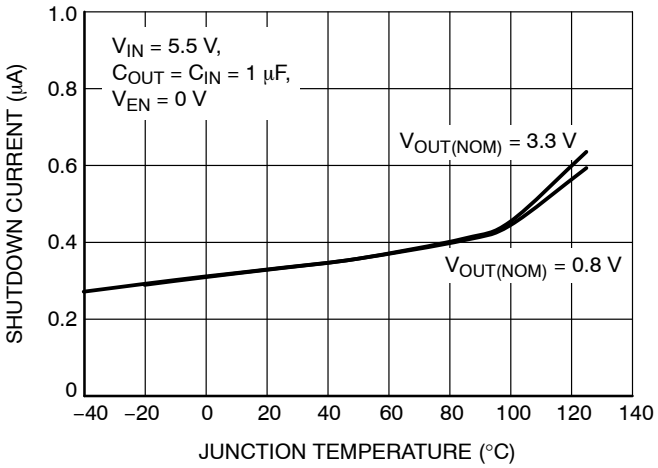


Figure 23. Shutdown Current vs. Temperature

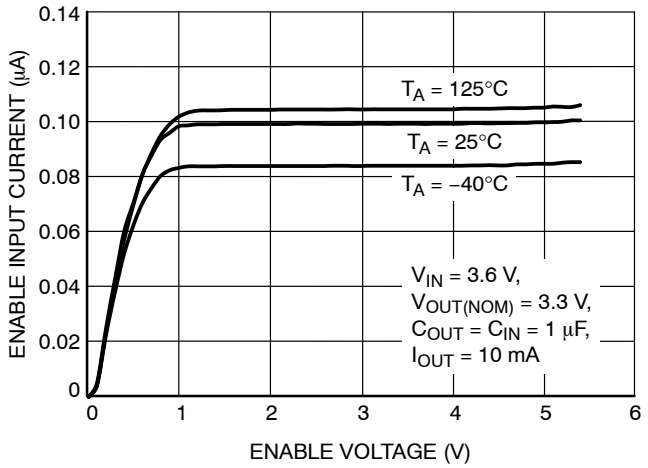


Figure 24. Enable Input Current vs. Enable Voltage

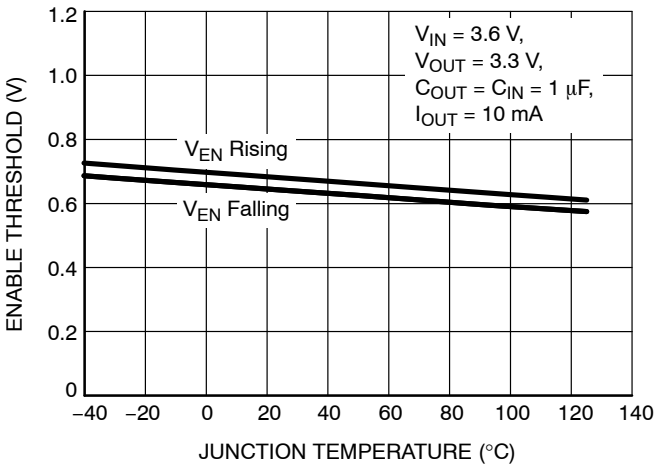


Figure 25. Enable Threshold vs. Temperature

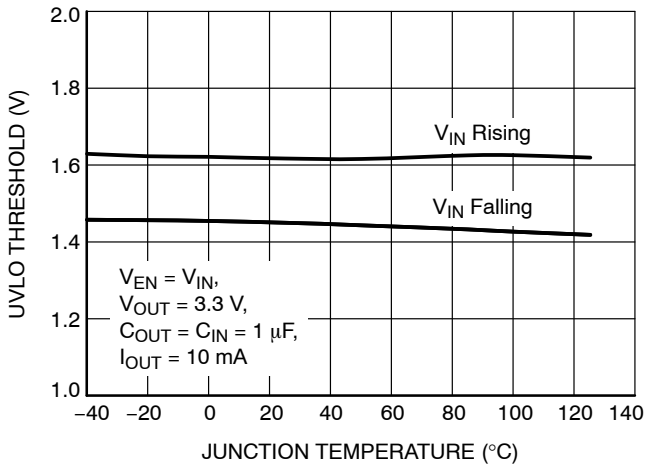


Figure 26. UVLO Threshold vs. Temperature

TYPICAL CHARACTERISTICS

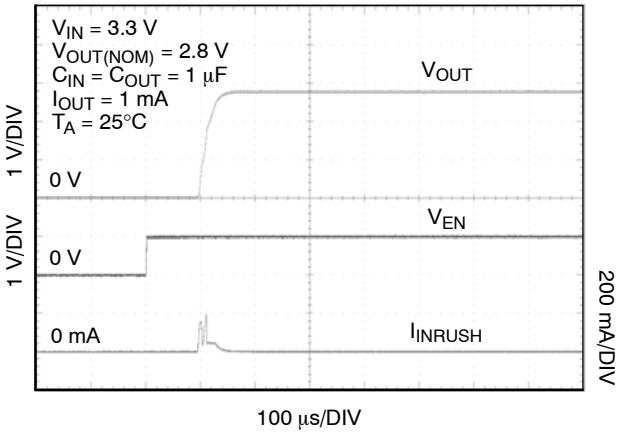


Figure 27. Turn−On Response, V_{OUT} = 2.8 V

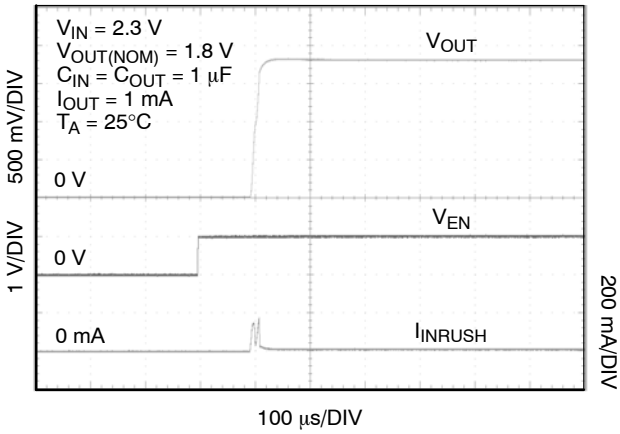


Figure 28. Turn−On Response, V_{OUT} = 1.8 V

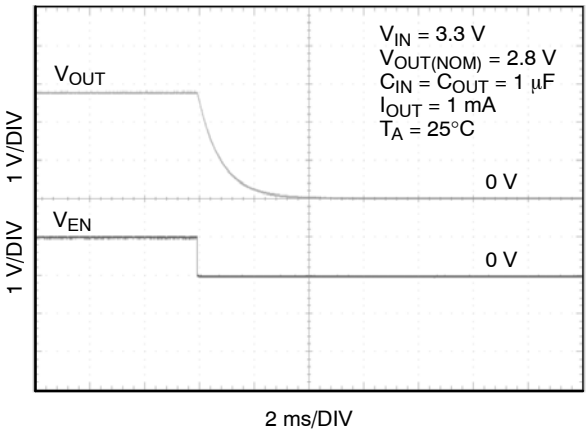


Figure 29. Turn−Off Response, V_{OUT} = 2.8 V

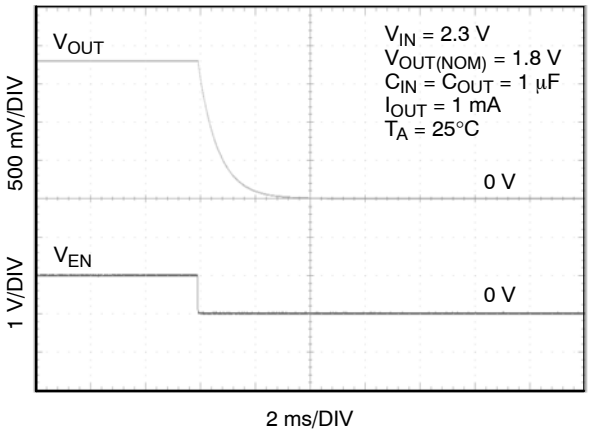


Figure 30. Turn−Off Response, V_{OUT} = 1.8 V

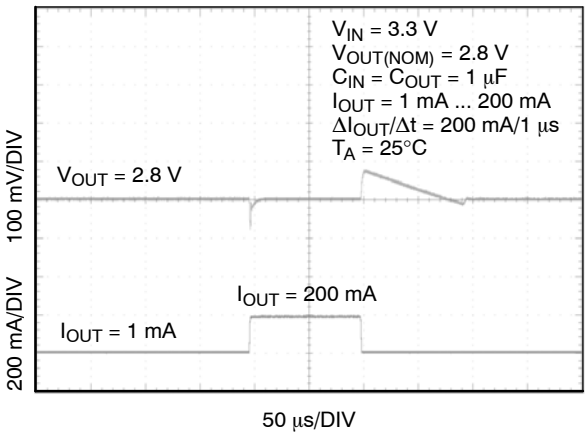


Figure 31. Load Transient Response, V_{OUT} = 2.8 V,
I_{OUT} = 1 mA to 200 mA

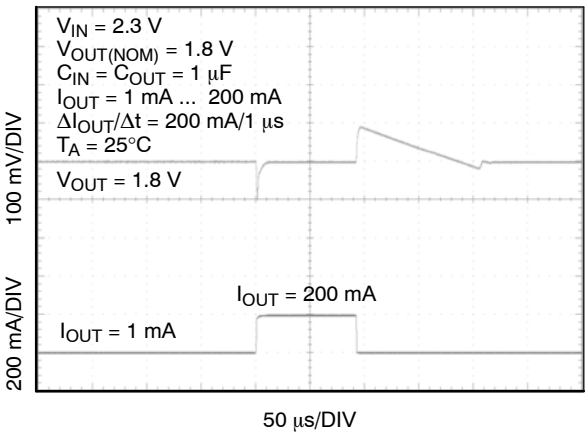


Figure 32. Load Transient Response, V_{OUT} = 1.8 V,
I_{OUT} = 1 mA to 200 mA

TYPICAL CHARACTERISTICS

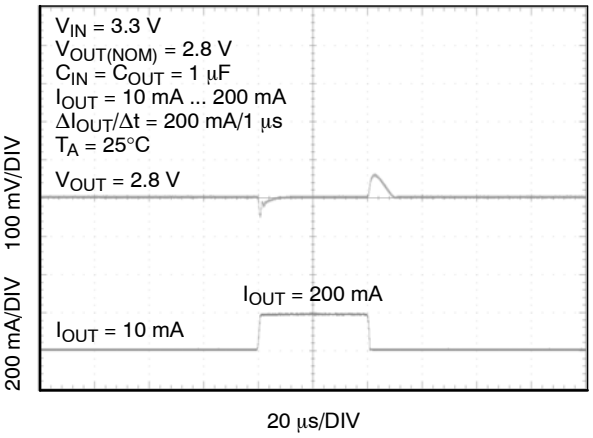


Figure 33. Load Transient Response, V_{OUT} = 2.8 V, I_{OUT} = 10 mA to 200 mA

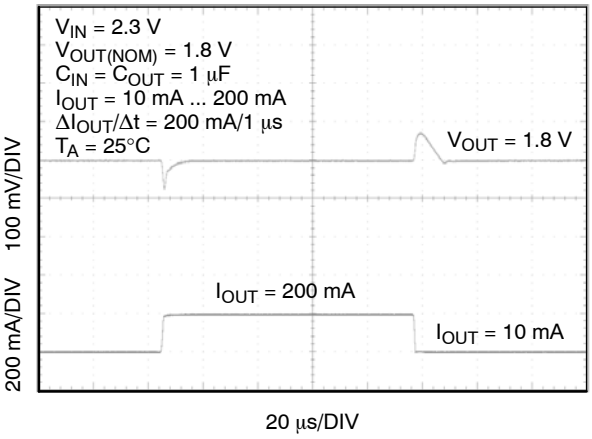


Figure 34. Load Transient Response, V_{OUT} = 1.8 V, I_{OUT} = 10 mA to 200 mA

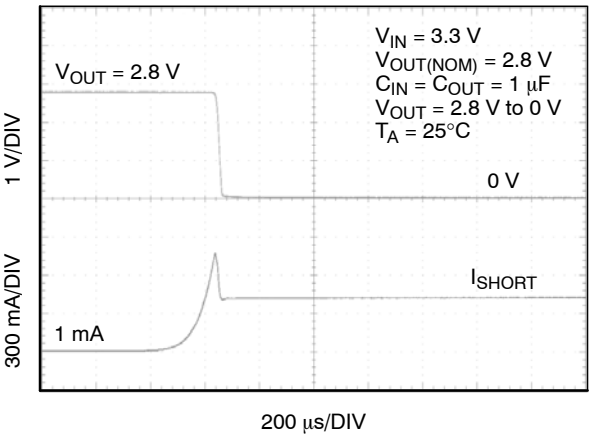


Figure 35. Short−Circuit Response, V_{OUT} = 2.8 V

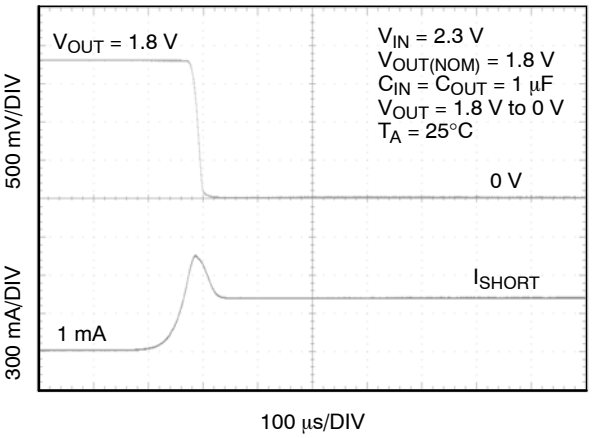


Figure 36. Short−Circuit Response, V_{OUT} = 1.8 V

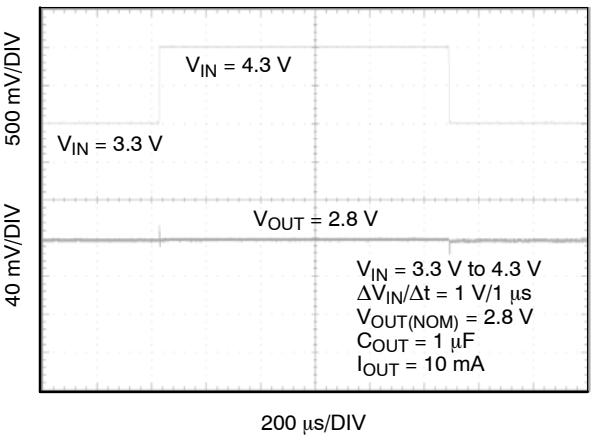


Figure 37. Line Transient Response, V_{OUT} = 2.8 V

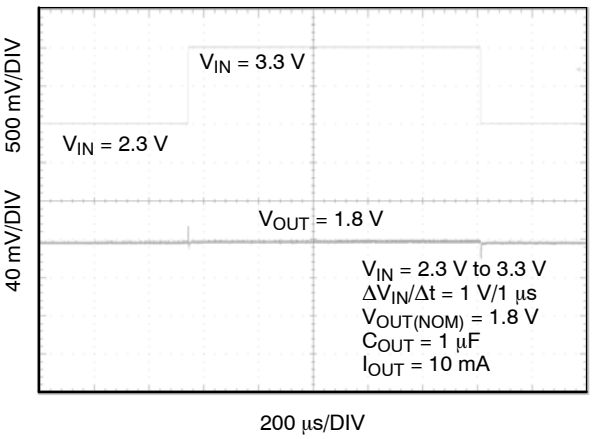


Figure 38. Line Transient Response, V_{OUT} = 1.8 V

TYPICAL CHARACTERISTICS

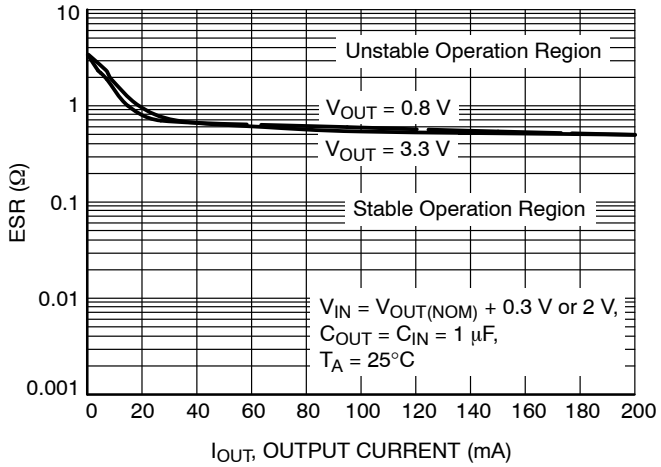


Figure 39. ESR vs. Output Current

APPLICATIONS INFORMATION

General

The NCP729 is a high performance 200 mA Very Low Dropout Linear Regulator. This device delivers excellent noise and dynamic performance. It features typical quiescent current of 35 μA at no−load, ultra−low noise of 10 μV_{RMS} and high PSRR of 72 dB at 1 kHz. Such excellent dynamic parameters and small package size make the device an ideal choice for powering the precision analog and noise sensitive circuitry in portable applications. NCP729 requires very small voltage headroom for correct operation. The dropout for 3.3 V voltage option is only 68 mV (typ.) A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 300 nA from the IN pin.

The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor (C_{IN})

It is recommended to connect a minimum of 1 μF Ceramic X5R or X7R capacitor close to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage.

There is no requirement for the min./max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and power source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large line/load transients are encountered in the application.

Output Capacitor (C_{OUT})

The NCP729 is designed to operate with a small 1.0 μF ceramic capacitor on the output. To assure proper operation it is recommended to use min. 1.0 μF capacitor with the initial tolerance of ±10%, made of X7R or X5R dielectric material types.

NCP729 is internally compensated so there is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 500 mΩ.

Larger output capacitors could be used to improve the load transient response or high frequency PSRR. This part is not designed to work with tantalum or electrolytic capacitors on the output due to their large ESR and ESL. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperatures. The tantalum capacitors are generally more costly than ceramic capacitors.

The table below lists examples of suitable output capacitors:

Part Number	Description
C0402C105K8PACTU	1 μF Ceramic ±10%, 10 V, 0402, X5R
C1005X5R1A105K	-||-
GRM155R61A105KE15D	-||-
0402ZD105KAT2A	-||-
MCCA000571	1 μF Ceramic ±10%, 50 V, 1206, X7R
ECJ−0EB0J475M	4.7 μF Ceramic ±20%, 6.3 V, 0402, X5R

No−load Operation

The regulator remains stable and regulates the output voltage properly within the ±2% tolerance limits with no external load applied to the output.

Enable Operation

The NCP729 uses the EN pin to enable, disable its output and to deactivate, activate the active output discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off and the active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 1 kΩ resistor. In the disable state the device consumes as low as typ. 300 nA from the V_{IN}.

If the EN pin voltage > 0.9 V the device is guaranteed to be enabled. The output voltage is regulated at the nominal value and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 110 nA which assures that the device is turned−off when the EN pin is not connected. A build in 2 mV of hysteresis in the EN prevents from periodic on/off oscillations that can occur due to noise.

In the case where the EN function isn't required the EN pin should be tied directly to IN.

Undervoltage Lockout

The internal UVLO circuitry assures that the device becomes disabled when the V_{IN} falls below typ. 1.5 V. When the V_{IN} voltage ramps−up the NCP729 becomes enabled for $V_{IN} \geq 1.6$ V. The 100 mV hysteresis prevents from on/off oscillations that can occur due to noise on V_{IN} line.

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases where the extended reverse current condition is anticipated the device may require additional external protection.

Output Current Limit

Output Current is internally limited within the IC to a typical 400 mA. The NCP729 will source this amount of current measured with the output voltage 100 mV lower than the nominal V_{OUT}. The short circuit current flowing to the IN pin when the Output Voltage is directly shorted to ground will be just slightly above 400 mA – typ. 410 mA. The current limit and short circuit were verified to work properly and to secure the part from the damage up to V_{IN} = 5.5 V at T_A = 25°C. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} – 165°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} – 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled. The thermal shutdown feature provides protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP729 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C.

The maximum power dissipation the IC can handle is given by:

$$P_{D(MAX)} = \frac{[125 - T_A]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP729 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND}@I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

Load Regulation

The NCP729 features excellent load regulation of typical 200 μV in the 0 mA to 200 mA range. Due to this fact at large load currents the major contributors to the output voltage shift will be the junction temperature increase and the PCB trace resistance.

Line Regulation

The IC features very good line regulation of typical 150 μV/V measured for the input voltage change from V_{IN} = V_{OUT} + 0.3 V to 5.5 V.

Power Supply Rejection Ratio

The NCP729 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout. Additional Ferrite Bead Input filter will further improve the PSRR.

Output Noise

The IC is designed for ultra−low noise output voltage. Figures 3 and 4 illustrate the noise performance for different V_{OUT}, I_{OUT}, C_{OUT}. Generally the noise performance in the indicated frequency range improves with increasing output current.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. V_{OUT}, V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance for noise pickup.

In order to minimize the solution size use 0402 capacitors. Larger copper area connected to the pins will improve the device thermal resistance. The actual power dissipation can be calculated by the formula given in Equation 2.

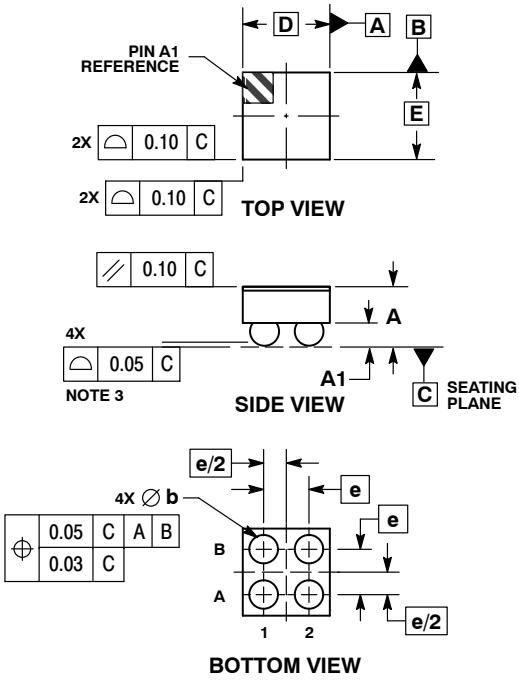
Table 5. ORDERING INFORMATION

Device	Voltage Option	Marking	Package	Shipping †
NCP729FC08T2G	0.8 V	7AA	CSP4 (Pb−Free)	5000 / Tape & Reel
NCP729FC18T2G	1.8 V	7AB		
NCP729FC25T2G	2.5 V	7AG		
NCP729FC26T2G	2.6 V	7AC		
NCP729FC28T2G	2.8 V	7AD		
NCP729FC285T2G	2.85 V	7AE		
NCP729FC30T2G	3.0 V	7AH		
NCP729FC33T2G	3.3 V	7AF		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

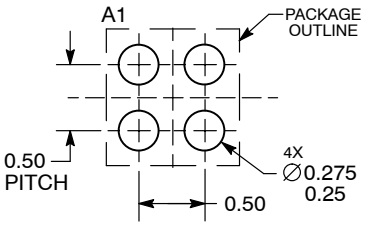
CSP4, 1.06x1.06
CASE 568AD
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.70
A1	0.21	0.26
b	0.30	0.34
D	1.06 BSC	
E	1.06 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
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For additional information, please contact your local Sales Representative

NCP729/D