## Document Title

**128Kx8 bit Low Power CMOS Static RAM**

## Revision History

| Revision No. | History | Draft Data | Remark |
|---|---|---|---|
| 0.0 | Initial draft | July 15, 2002 | Preliminary |
| 0.1 | Revised<br>- Deleted 32-TSOP1-0820R, 32-TSOP1-0813.4F/R Package Type.<br>- Added Commercial product.<br>- Added 55ns product( Vcc = 3.0V~3.6V) | December 4, 2002 | Preliminary |
| 0.2 | Revised<br>- Added Lead Free 32-SOP-525 Product<br>- Added Lead Free 32-TSOP1-0820F Product | June 23, 2003 | Preliminary |
| 1.0 | Finalized<br>- Changed $I_{CC}$ from 3mA to 2mA<br>- Changed $I_{CC}2$ from 25mA to 20mA<br>- Changed $I_{SB}1$(Commercial) from 10μA to 6μA<br>- Changed $I_{SB}1$(industrial) from 10μA to 6μA<br>- Changed $I_{SB}1$(Automotive) from 20μA to 10μA<br>- Changed $I_{DR}$(Commercial) from 10μA to 6μA<br>- Changed $I_{DR}$(industrial) from 10μA to 6μA<br>- Changed $I_{DR}$(Automotive) from 20μA to 10μA | September 16, 2003 | Final |
| 2.0 | Revised<br>- Changed $I_{SB}1$ of Automotive product from 10μA to 25μA<br>- Changed $I_{DR}$ of Automotive product from 10μA to 25μA<br>- Added Lead Free Products | March 27, 2005 | Final |

## *128Kx8 bit Super Low Power and Low Voltage full CMOS Static RAM*

### FEATURES

- Process Technology: Full CMOS
- Organization: 128K x 8
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three state outputs
- Package Type: 32-SOP-525, 32-TSOP1-0820F
  32-SOP-525, 32-TSOP1-0820F

### GENERAL DESCRIPTION

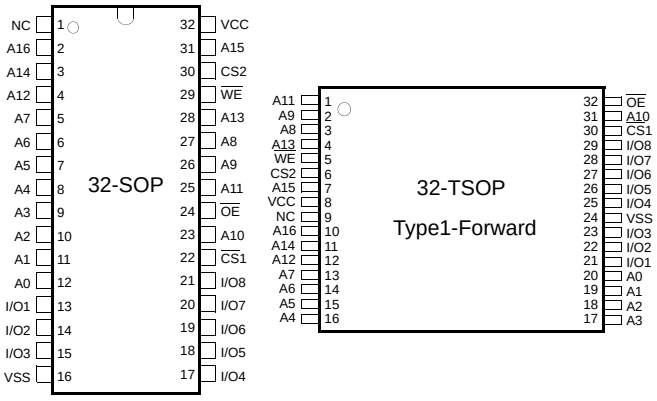
The K6X1008T2D families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support verious operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | | PKG Type |
|---|---|---|---|---|---|---|
| | | | | Standby ($I_{SB1}$, Max) | Operating ($I_{CC2}$, Max) | |
| K6X1008T2D-B | Commercial(0~70°C) | 2.7~3.6V | 55[1]/70[2]/85ns | 6μA | 20mA | 32-SOP-525<br>32-TSOP1-0820F |
| K6X1008T2D-F | Industrial(-40~85°C) | | | | | |
| K6X1008T2D-Q | Automotive(-40~125°C) | | 70[2]/85ns | 25μA | | |

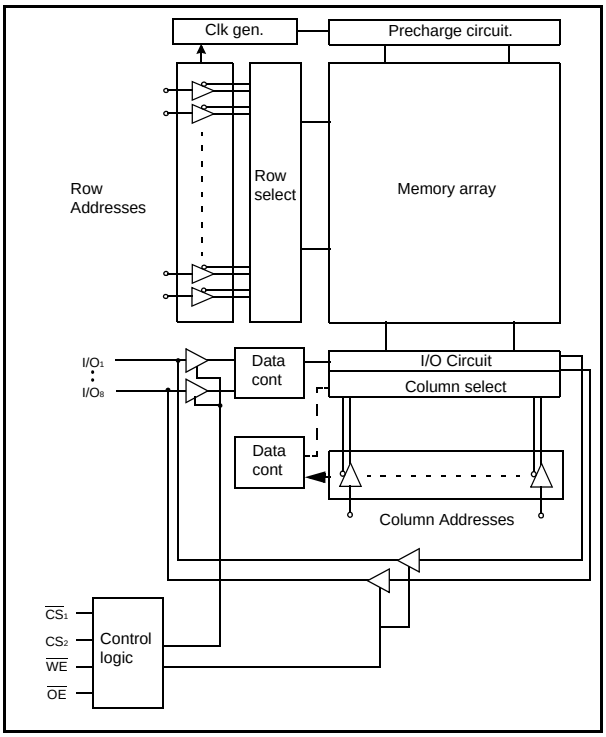
1. This parameter is measured in the voltage range of 3.0V~3.6V with 30pF test load.
2. This parameter is measured with 30pF test load.

### PIN DESCRIPTION




| Name | Function |
|---|---|
| $A_0$~$A_{16}$ | Address Inputs |
| $\overline{WE}$ | Write Enable Input |
| $\overline{CS_1}$,$CS_2$ | Chip Select Input |
| $\overline{OE}$ | Output Enable Input |
| $I/O_1$~$I/O_8$ | Data Inputs/Outputs |
| Vcc | Power |
| Vss | Ground |
| NC | No Connection |

### FUNCTIONAL BLOCK DIAGRAM

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## PRODUCT LIST

| Commercial Products(0~70°C) | | Industrial Products(-40~85°C) | | Atomotive Products(-40~125°C) | |
|---|---|---|---|---|---|
| **Part Name** | **Function** | **Part Name** | **Function** | **Part Name** | **Function** |
| K6X1008T2D-GB55[1)] | 32-SOP, 55ns, LL | K6X1008T2D-GF55[1)] | 32-SOP, 55ns, LL | K6X1008T2D-GQ70 | 32-SOP, 70ns, L |
| K6X1008T2D-GB70 | 32-SOP, 70ns, LL | K6X1008T2D-GF70 | 32-SOP, 70ns, LL | K6X1008T2D-GQ85 | 32-SOP, 85ns, L |
| K6X1008T2D-GB85 | 32-SOP, 85ns, LL | K6X1008T2D-GF85 | 32-SOP, 85ns, LL | K6X1008T2D-BQ70[2)] | 32-SOP, 70ns, L, LF |
| K6X1008T2D-BB55[1,2)] | 32-SOP, 55ns, LL, LF | K6X1008T2D-BF55[1,2)] | 32-SOP, 55ns, LL, LF | K6X1008T2D-BQ85[2)] | 32-SOP, 85ns, L, LF |
| K6X1008T2D-BB70[2)] | 32-SOP, 70ns, LL, LF | K6X1008T2D-BF70[2)] | 32-SOP, 70ns, LL, LF | K6X1008T2D-TQ70 | 32-TSOP-F, 70ns, L |
| K6X1008T2D-BB85[2)] | 32-SOP, 85ns, LL, LF | K6X1008T2D-BF85[2)] | 32-SOP, 85ns, LL, LF | K6X1008T2D-TQ85 | 32-TSOP-F, 85ns, L |
| K6X1008T2D-TB55[1)] | 32-TSOP-F, 55ns, LL | K6X1008T2D-TF55[1)] | 32-TSOP-F, 55ns, LL | K6X1008T2D-PQ70[2)] | 32-TSOP-F, 70ns, L, LF |
| K6X1008T2D-TB70 | 32-TSOP-F, 70ns, LL | K6X1008T2D-TF70 | 32-TSOP-F, 70ns, LL | K6X1008T2D-PQ85[2)] | 32-TSOP-F, 85ns, L, LF |
| K6X1008T2D-TB85 | 32-TSOP-F, 85ns, LL | K6X1008T2D-TF85 | 32-TSOP-F, 85ns, LL | | |
| K6X1008T2D-PB55[1,2)] | 32-TSOP-F, 55ns, LL, LF | K6X1008T2D-PF55[1,2)] | 32-TSOP-F, 55ns, LL, LF | | |
| K6X1008T2D-PB70[2)] | 32-TSOP-F, 70ns, LL, LF | K6X1008T2D-PF70[2)] | 32-TSOP-F, 70ns, LL, LF | | |
| K6X1008T2D-PB85[2)] | 32-TSOP-F, 85ns, LL, LF | K6X1008T2D-PF85[2)] | 32-TSOP-F, 85ns, LL, LF | | |

1. Operating voltage range is 3.0V~3.6V
2. Lead Free Product

## FUNCTIONAL DESCRIPTION

| $\overline{CS_1}$ | $CS_2$ | $\overline{OE}$ | $\overline{WE}$ | I/O | Mode | Power |
|---|---|---|---|---|---|---|
| H | X[1)] | X[1)] | X[1)] | High-Z | Deselected | Standby |
| X[1)] | L | X[1)] | X[1)] | High-Z | Deselected | Standby |
| L | H | H | H | High-Z | Output Disabled | Active |
| L | H | L | H | Dout | Read | Active |
| L | H | X[1)] | L | Din | Write | Active |

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS[1)]

| Item | Symbol | Ratings | Unit | Remark |
|---|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$,$V_{OUT}$ | -0.2 to $V_{CC}$+0.3V(Max. 3.9V) | V | - |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -0.2 to 3.9 | V | - |
| Power Dissipation | $P_D$ | 1.0 | W | - |
| Storage temperature | $T_{STG}$ | -65 to 150 | °C | - |
| Operating Temperature | $T_A$ | 0 to 70 | °C | K6X1008T2D-B |
| | | -40 to 85 | °C | K6X1008T2D-F |
| | | -40 to 125 | °C | K6X1008T2D-Q |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS[1)]

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | Vcc | 2.7 | 3.0/3.3 | 3.6 | V |
| Ground | Vss | 0 | 0 | 0 | V |
| Input high voltage | $V_{IH}$ | 2.2 | - | Vcc+0.2[2)] | V |
| Input low voltage | $V_{IL}$ | -0.2[3)] | - | 0.6 | V |

Note:
1. Commercial Product: $T_A$=0 to 70°C, Otherwise specified
. Industrial Product: $T_A$=-40 to 85°C, Otherwise specified
Automotive Product: $T_A$=-40 to 125°C, Otherwise specified
2. Overshoot: Vcc+3.0V in case of pulse width≤30ns.
3. Undershoot: -3.0V in case of pulse width≤30ns.
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE[1)] (f=1MHz, TA=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 8 | pF |
| Input/Output capacitance | $C_{IO}$ | $V_{IO}$=0V | - | 10 | pF |

1. Capacitance is sampled, not 100% tested

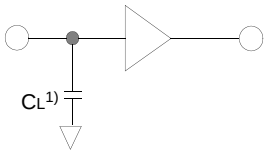
## DC AND OPERATING CHARACTERISTICS

| Item | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=Vss to Vcc | | -1 | - | 1 | μA |
| Output leakage current | $I_{LO}$ | $\overline{CS_1}$=$V_{IH}$ or $CS_2$=$V_{IL}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$, $V_{IO}$=Vss to Vcc | | -1 | - | 1 | μA |
| Operating power supply current | $I_{CC}$ | $I_{IO}$=0mA, $\overline{CS_1}$=$V_{IL}$, $CS_2$=$V_{IH}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$, Read | | - | - | 2 | mA |
| Average operating current | $I_{CC1}$ | Cycle time=1μs, 100%duty, $I_{IO}$=0mA, $\overline{CS_1}$≤0.2V, $CS_2$≥Vcc-0.2V, $V_{IN}$≤0.2V or $V_{IN}$≥$V_{CC}$-0.2V | | - | - | 3 | mA |
| | $I_{CC2}$ | Cycle time=Min, 100% duty, $I_{IO}$=0mA, $\overline{CS_1}$=$V_{IL}$, $CS_2$=$V_{IH}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$ | | - | - | 20 | mA |
| Output low voltage | $V_{OL}$ | $I_{OL}$=2.1mA | | - | - | 0.4 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$=-1.0mA | | 2.4 | - | - | V |
| Standby Current(TTL) | $I_{SB}$ | $\overline{CS_1}$=$V_{IH}$, CS2=$V_{IL}$, Other inputs=$V_{IH}$ or $V_{IL}$ | | - | - | 0.3 | mA |
| Standby Current(CMOS) | $I_{SB1}$ | $\overline{CS_1}$≥Vcc-0.2V, $CS_2$≥Vcc-0.2V or $CS_2$≤0.2V, Other inputs=0~Vcc | K6X1008T2D-B | - | - | 6 | μA |
| | | | K6X1008T2D-F | - | - | 6 | μA |
| | | | K6X1008T2D-Q | - | - | 25 | μA |

## AC OPERATING CONDITIONS

**TEST CONDITIONS**( Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage:1.5V
Output load(see right): $C_L$=100pF+1TTL
$C_L$=30pF+1TTL




1. Including scope and jig capacitance

## AC CHARACTERISTICS

($V_{CC}$=2.7~3.6V, Commercial product:$T_A$=0 to 70°C, Industrial product:$T_A$=-40 to 85°C, Automotive product:$T_A$=-40 to 125°C )

| Parameter List | | Symbol | Speed Bins | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 55ns[1] | | 70ns | | 85ns | | |
| | | | Min | Max | Min | Max | Min | Max | |
| Read | Read Cycle Time | $t_{RC}$ | 55 | - | 70 | - | 85 | - | ns |
| | Address Access Time | $t_{AA}$ | - | 55 | - | 70 | - | 85 | ns |
| | Chip Select to Output | $t_{CO}$ | - | 55 | - | 70 | - | 85 | ns |
| | Output Enable to Valid Output | $t_{OE}$ | - | 25 | - | 35 | - | 40 | ns |
| | Chip Select to Low-Z Output | $t_{LZ}$ | 10 | - | 10 | - | 10 | - | ns |
| | Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | - | 5 | - | 5 | - | ns |
| | Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 25 | 0 | 25 | 0 | 25 | ns |
| | Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 25 | 0 | 25 | 0 | 25 | ns |
| | Output Hold from Address Change | $t_{OH}$ | 10 | - | 10 | - | 15 | - | ns |
| Write | Write Cycle Time | $t_{WC}$ | 55 | - | 70 | - | 85 | - | ns |
| | Chip Select to End of Write | $t_{CW}$ | 45 | - | 60 | - | 70 | - | ns |
| | Address Set-up Time | $t_{AS}$ | 0 | - | 0 | - | 0 | - | ns |
| | Address Valid to End of Write | $t_{AW}$ | 45 | - | 60 | - | 70 | - | ns |
| | Write Pulse Width | $t_{WP}$ | 40 | - | 50 | - | 60 | - | ns |
| | Write Recovery Time | $t_{WR}$ | 0 | - | 0 | - | 0 | - | ns |
| | Write to Output High-Z | $t_{WHZ}$ | 0 | 25 | 0 | 25 | 0 | 30 | ns |
| | Data to Write Time Overlap | $t_{DW}$ | 20 | - | 25 | - | 35 | - | ns |
| | Data Hold from Write Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | ns |
| | End Write to Output Low-Z | $t_{OW}$ | 5 | - | 5 | - | 5 | - | ns |

1. Voltage range is 3.0V~3.6V for commercial and industrial product.

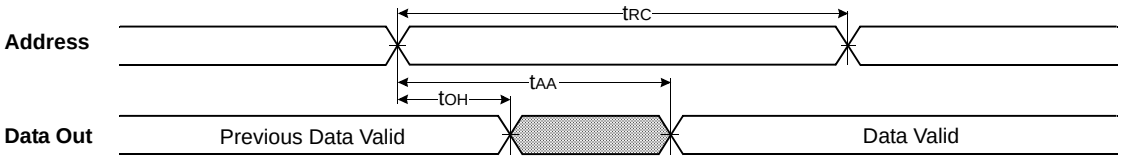
## DATA RETENTION CHARACTERISTICS

| Item | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Vcc for data retention | $V_{DR}$ | $\overline{CS_1}$≥Vcc-0.2V[1] | | 2.0 | - | 3.6 | V |
| Data retention current | $I_{DR}$ | Vcc=3.0V, $\overline{CS_1}$≥Vcc-0.2V[1] | K6X1008T2D-B | - | - | 6 | µA |
| | | | K6X1008T2D-F | - | - | 6 | µA |
| | | | K6X1008T2D-Q | | | 25 | µA |
| Data retention set-up time | $t_{SDR}$ | See data retention waveform | | 0 | - | - | ms |
| Recovery time | $t_{RDR}$ | | | 5 | - | - | |

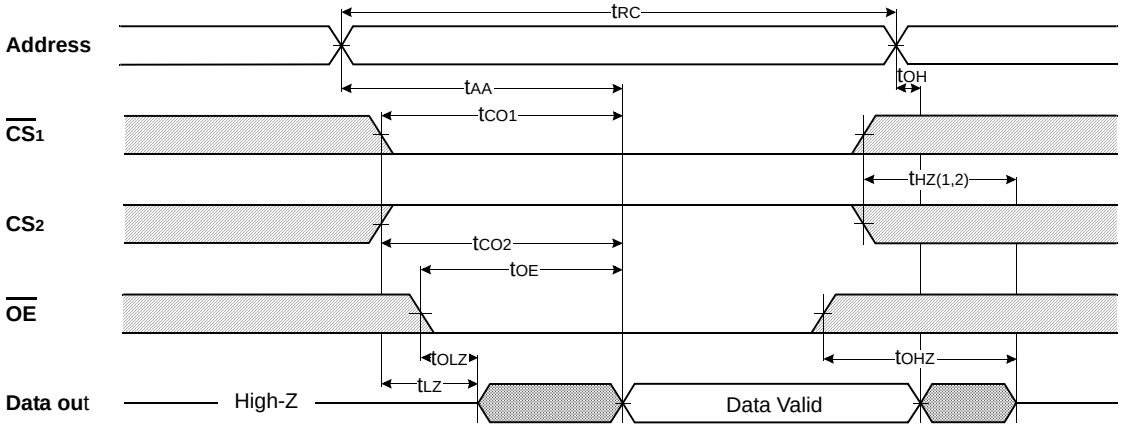
1. $\overline{CS_1}$≥Vcc-0.2V, $CS_2$≥Vcc-0.2V, or $CS_2$≤0.2V

## TIMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}1=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



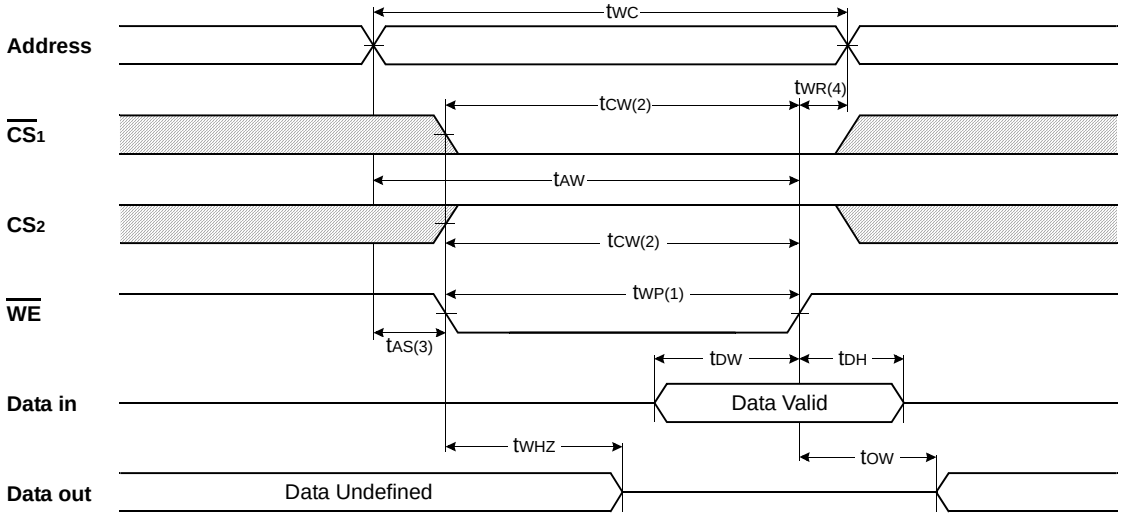

### TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



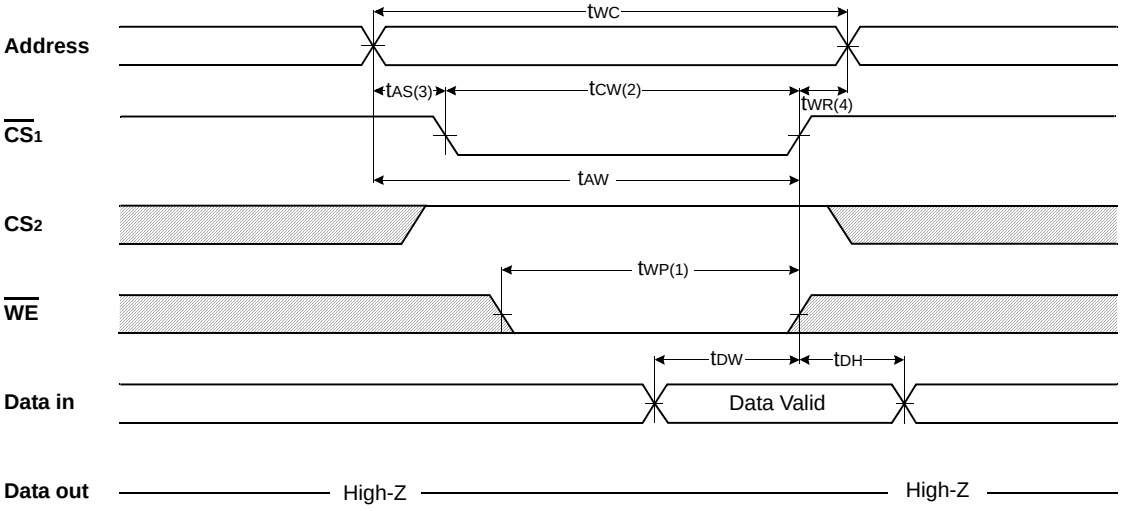

**NOTES (**READ CYCLE)

1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device interconnection.

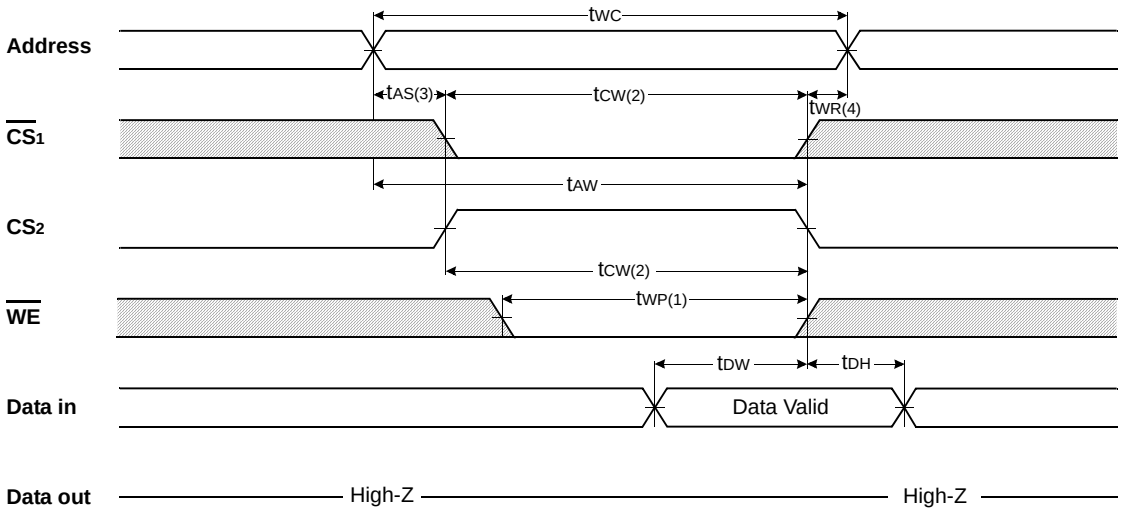
### TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)




### TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



### TIMING WAVEFORM OF WRITE CYCLE(3) ($CS_2$ Controlled)

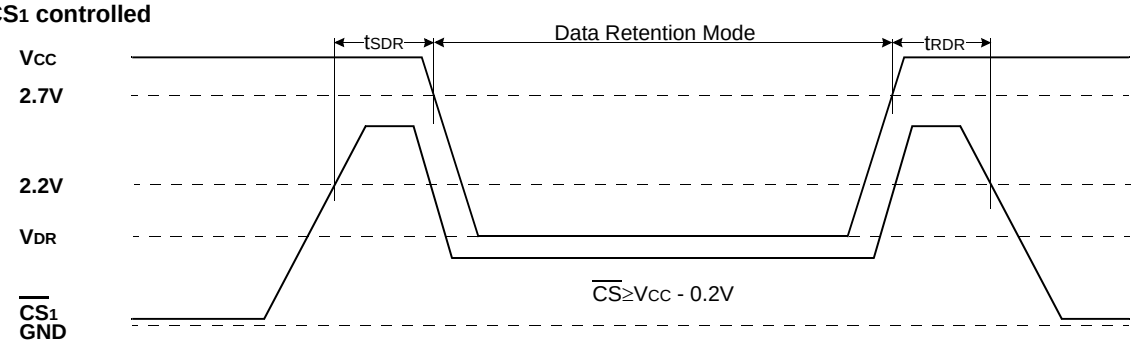



**NOTES** (WRITE CYCLE)

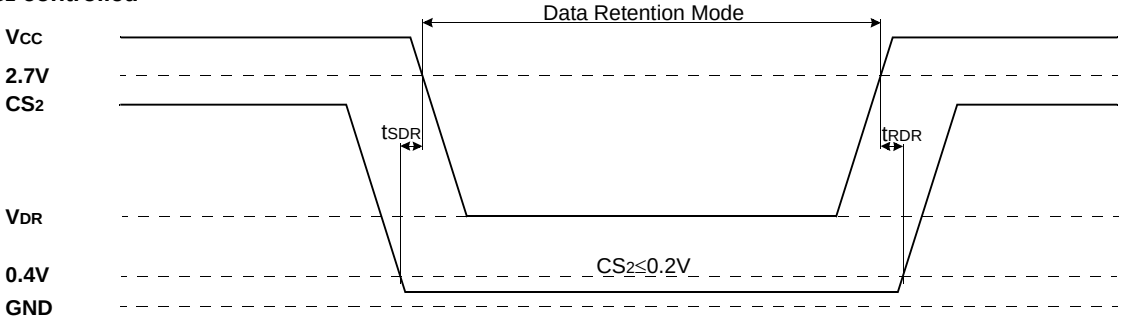
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high $CS_2$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, $CS_2$ going high and $\overline{WE}$ going low: A write end at the earliest transition among $\overline{CS_1}$ going high, $CS_2$ going low and $\overline{WE}$ going high, $t_{WP}$ is measured from the begining of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS_1}$ going low or $CS_2$ going high to the end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR2}$ applied in case a write ends as $CS_2$ going to low.

## DATA RETENTION WAVE FORM

### $\overline{CS_1}$ controlled



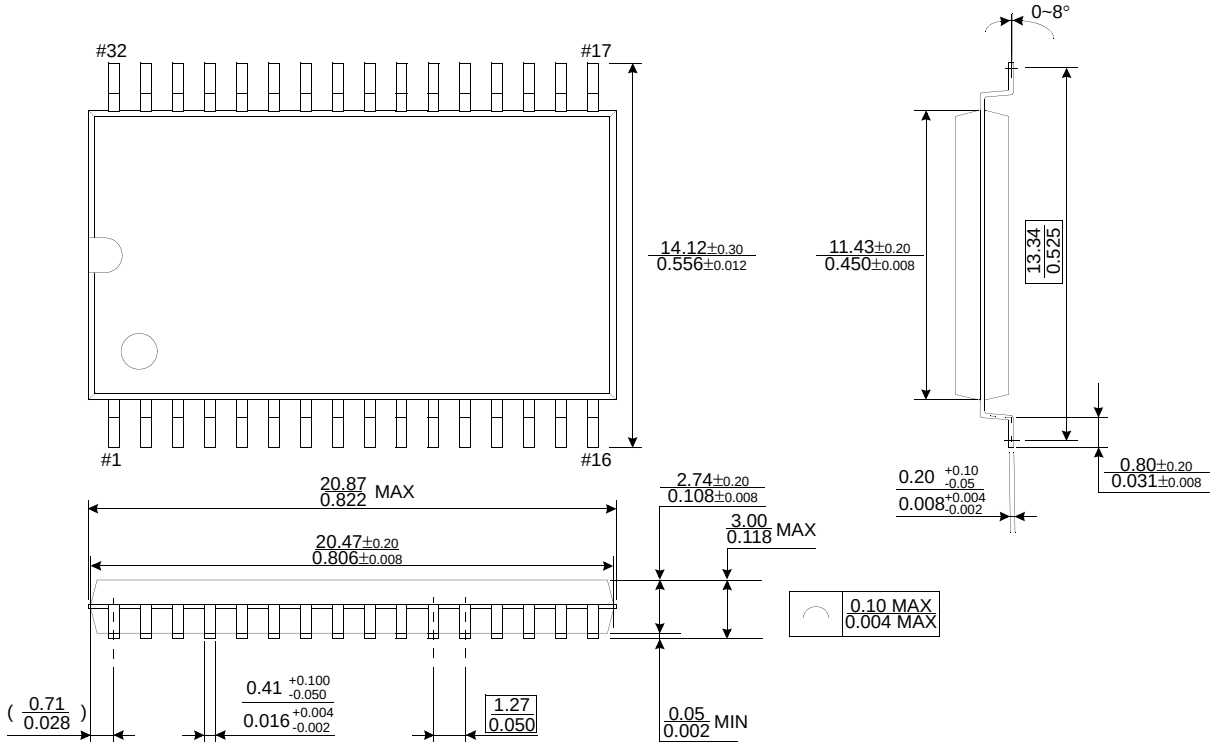

### $CS_2$ controlled



## PACKAGE DIMENSIONS

Units: millimeters(inches)

### 32 PLASTIC SMALL OUTLINE PACKAGE (525mil)




### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)