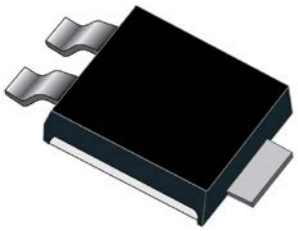
RoHS Compliant

# Nanosecond SCR Switch

## DESCRIPTION

The UPGA301Ae3 is designed for high current narrow-pulse switching applications where size and current handling capability are critical. These devices may be triggered on using low power logic drivers from (+0.8 V at 200 µA). Epoxy packaged, oxide passivated planar SCR chips with metallurgic bonds on both sides to achieve high reliability. Internal wire bond connection allows high current surge capability for narrow pulse applications.



**Powermite 3 Package**

**Important:** For the latest information, visit our website http://www.microsemi.com.

## FEATURES

- Low thermal resistance package for higher current operation
- High speed switching capability
- Efficient heat path with Integral locking bottom metal tab
- Full metallic bottom eliminates flux entrapment
- Compatible with automatic insertion equipment
- Low profile-maximum height of 1mm
- RoHS compliant

## APPLICATIONS / BENEFITS

- Reference Microsemi MicroNote 601 and 602
- Nanosecond SCR switch for reliable high current pulse generators, modulators and photo-flash quenching
- Logic drive capability (0.8 V, 200 µA)
- Ideal for laser range finder and camera applications
- Ideal for automotive collision avoidance applications
- Small 8.45 $mm^2$ foot print (See mounting pad details)

## MAXIMUM RATINGS @ 25 ºC unless otherwise specified

| Parameters/Test Conditions | Symbol | Value | Unit |
|---|---|---|---|
| Storage Temperature | $T_{STG}$ | -50 to +150 | ºC |
| Junction Temperature | $T_J$ | 0 to +125 | ºC |
| Thermal Resistance Junction-to-Case | $R_{\Theta JC}$ | 4.0 | ºC/W |
| Thermal Resistance Junction-to-Ambient (1) | $R_{\Theta JA}$ | 65 | ºC/W |
| Repetitive Peak Off-State Voltage | $V_{DRM}$ | 100 | V |
| Peak On-State Current for 50 ns (max) | $I_{TSM}$ | 100 | A |
| Peak Gate Current | $I_{GM}$ | 250 | mA |
| Reverse Gate Voltage | $V_{GR}$ | 5 | V |
| Solder Temperature @ 10 s | $T_{SP}$ | 260 | °C |

**Notes:** 1. When mounted on 0.06" thick FR-4PC board using 2 oz copper with recommended minimum foot print

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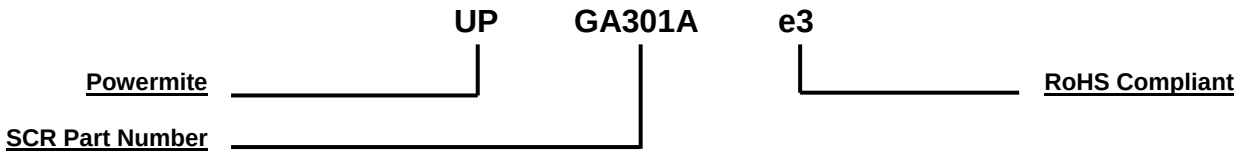
## MECHANICAL and PACKAGING

- CASE: Void-free transfer molded thermosetting epoxy compound meeting UL94V-0
- TERMINALS: Annealed matte-tin plating over copper and readily solderable per MIL-STD-750, method 2026. (Consult factor for tin-lead plating.)
- MARKING: 301A• (dot indicates “e3” designation)
- POLARITY: Cathode designated by TAB 2
- TAPE & REEL option: 16 mm tape per standard EIA-481-B. Consult factory for quantities.
- WEIGHT: Approximately 0.072 gram
- See Package Dimensions on last page.

## PART NOMENCLATURE




## SYMBOLS & DEFINITIONS

| Symbol | Definition |
|---|---|
| $I_G$ | Gate Current: The direct current into the gate terminal. |
| $I_R$ | Reverse Current: The anode current for a negative anode voltage. |
| $I_T$ | On-State Current: The anode, principal or thyristor current when the thyristor is in the on state. |
| $V_D$ | Off-State Voltage: The anode, principal, or thyristor voltage when the thyristor is in the off state. |
| $V_{RRM}$ | Reverse Voltage, Repetitive Peak: The peak reverse voltage including all repetitive transient voltages but excluding all nonrepetitive transient voltages. |
| $V_{DRM}$ | Repetitive Peak Off-State Voltage: The highest instantaneous value of the off-state voltage, including all repetitive transient voltages but excluding all nonrepetitive transient voltages. |

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## ELECTRICAL CHARACTERISTICS @ $T_A$ = +25 ºC unless otherwise noted

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **On characteristics (up to 100 A w/ 100 ns pulse @ Duty Cycle = 0.0001% or less)** | | | | | | |
| Forward Blocking Current | $I_{DRM}$ | $V_{DRM}$ = 100 V, $R_{GK}$ = 1 kΩ | | | 1.0 | µA |
| On - State Voltage | $V_T$ | $I_T$ = 1 A, Ig =10 mA | | 1.1 | 1.5 | V |
| Gate Trigger Voltage | $V_{GT}$ | $V_D$ = 5 V, $R_{GS}$ = 100 Ω | | 0.5 | 0.75 | V |
| Gate Trigger Current | $I_{GT}$ | $V_D$ = 5 V, $R_{GS}$ = 10 kΩ | | 10 | 200 | µA |
| Reverse Gate Current | $I_{GR}$ | $V_{GR}$ = 5 V | | 0.01 | 0.1 | mA |
| Holding Current | $I_H$ | $V_D$ = 5 V, $R_{GK}$ = 1 kΩ | 1.0 | 3.0 | 5.0 | mA |
| Reverse Current (Note 1) | $I_{RRM}$ | $V_{RRM}$ = 30 V, $R_{GK}$ = 1 kΩ | | 1 | 10 | mA |
| **Switching characteristics (Tc = 25 °C)** | | | | | | |
| Delay Time | td | Ig = 20 mA, $I_T$ = 1 A | | 20 | 30 | ns |
| Rise Time | tr | $V_D$ = 60 V, $I_T$ =1 A, Ig =10 mA dc < 1% | | 15 | 25 | ns |
| Circuit Commutated Turn—off Time | tq | $I_T$ = 1.0 A , $I_R$ = 1.0 A max, $R_{GK}$ = 1 kΩ | | 0.3 | 0.5 | µs |
| Gate Trigger—on Pulse Width | tpg(on) | Ig = 10 mA, $I_T$ = 1 A | | 20 | 50 | ns |
| Critical Rate of Rise Off –State Voltage | dv/dt | $V_D$ = 30 V, $R_{GK}$ = 1 kΩ | 15 | 30 | | V/µs |

**Note 1:** Pulse Test intended to guarantee reverse anode voltage capability for pulse commutation. The device should not be operated in the reverse blocking mode on a continuous basis.




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## GRAPHS

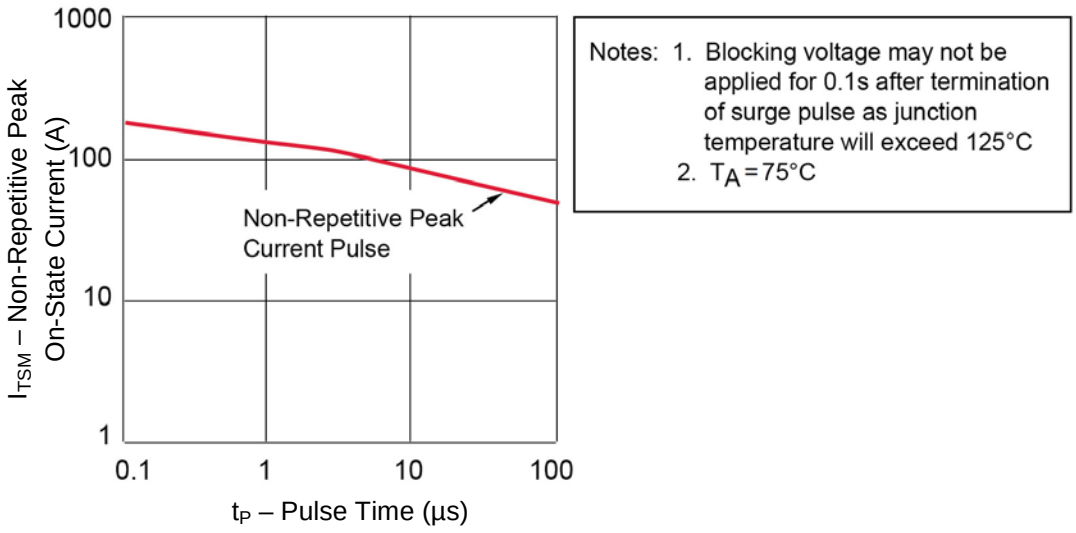


**FIGURE 1**
Surge Rating

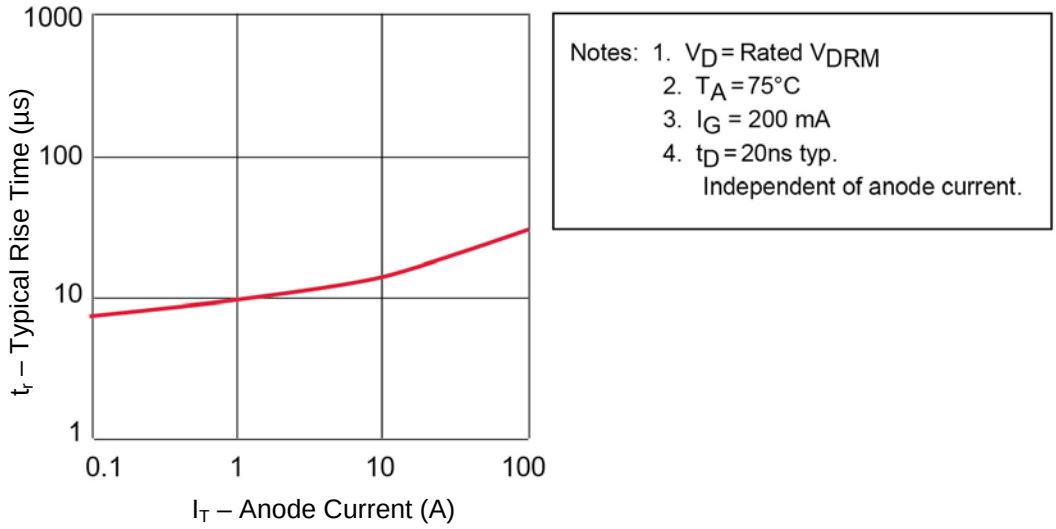


**FIGURE 2**
Switching Speed vs. Current




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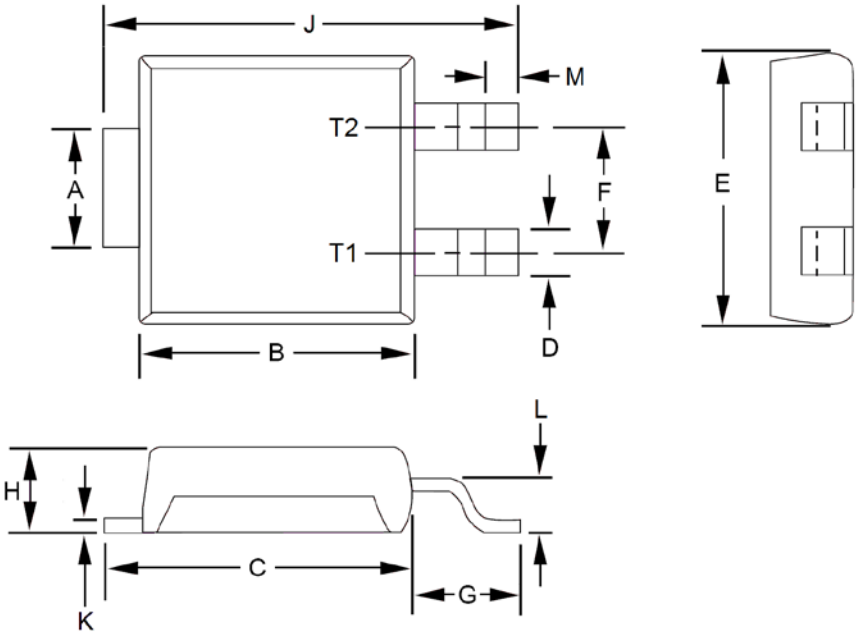
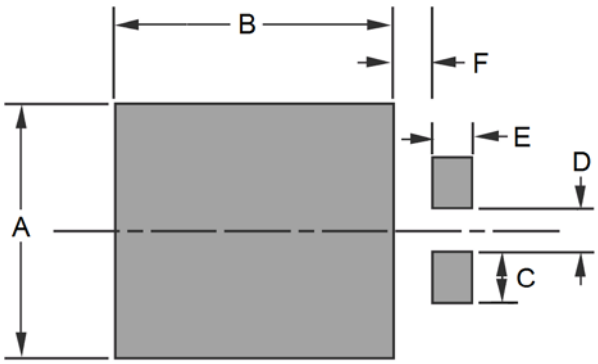
## PACKAGE DIMENSIONS



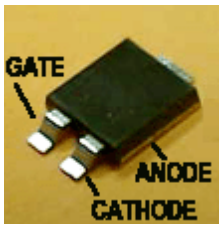

| | INCH | | MILLIMETERS | |
|---|---|---|---|---|
| **DIM** | **MIN** | **MAX** | **MIN** | **MAX** |
| **A** | 0.068 | 0.072 | 1.73 | 1.83 |
| **B** | 0.172 | 0.174 | 4.37 | 4.43 |
| **C** | 0.197 | 0.204 | 5.01 | 5.17 |
| **D** | 0.035 NOM | | 0.889 NOM | |
| **E** | 0.159 | 0.161 | 4.03 | 4.09 |
| **F** | 0.072 NOM | | 1.83 NOM | |
| **G** | 0.056 NOM | | 1.422 NOM | |
| **H** | 0.043 | 0.045 | 1.10 | 1.14 |
| **J** | 0.252 | 0.260 | 6.40 | 6.61 |
| **K** | 0.007 NOM | | 0.178 NOM | |
| **L** | 0.028 | 0.030 | 0.71 | 0.77 |
| **M** | 0.014 | 0.018 | 0.36 | 0.46 |
| **T1** | Gate (Tab 1) | | | |
| **T2** | Cathode (Tab 2) | | | |
| **Base** | Anode | | | |

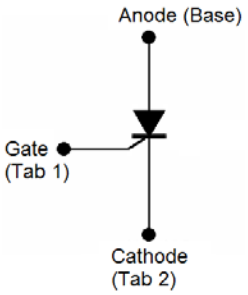
## PAD LAYOUT




| | INCH | MILLIMETERS |
|---|---|---|
| **DIM** | **NOMINAL** | **NOMINAL** |
| **A** | 0.190 | 4.826 |
| **B** | 0.210 | 5.344 |
| **C** | 0.038 | 0.965 |
| **D** | 0.034 | 0.864 |
| **E** | 0.030 | 0.762 |
| **F** | 0.030 | 0.762 |

## SCHEMATIC







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