Low Skew Zero Delay Buffer

FEATURES

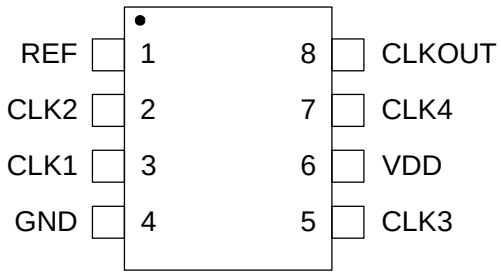
- Frequency Range 10MHz to 220MHz
- Zero input - output delay.
- Low output-to-output skew.
- Optional Drive Strength:
  Standard (8mA) *PL123E-05*
  High (12mA) *PL123E-05H*
- 2.5V or 3.3V, ±10% operation.
- Available in 8-pin SOP packaging.

DESCRIPTION

The PL123E-05 (-05H for High Drive) is a high performance, low skew, low jitter zero delay buffer designed to distribute high speed clocks. It has five low-skew outputs that are synchronized with the input. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than ±100ps, the device acts as a zero delay buffer. The input output propagation delay can be advanced or delayed by adjusting the load on the CLKOUT pin.

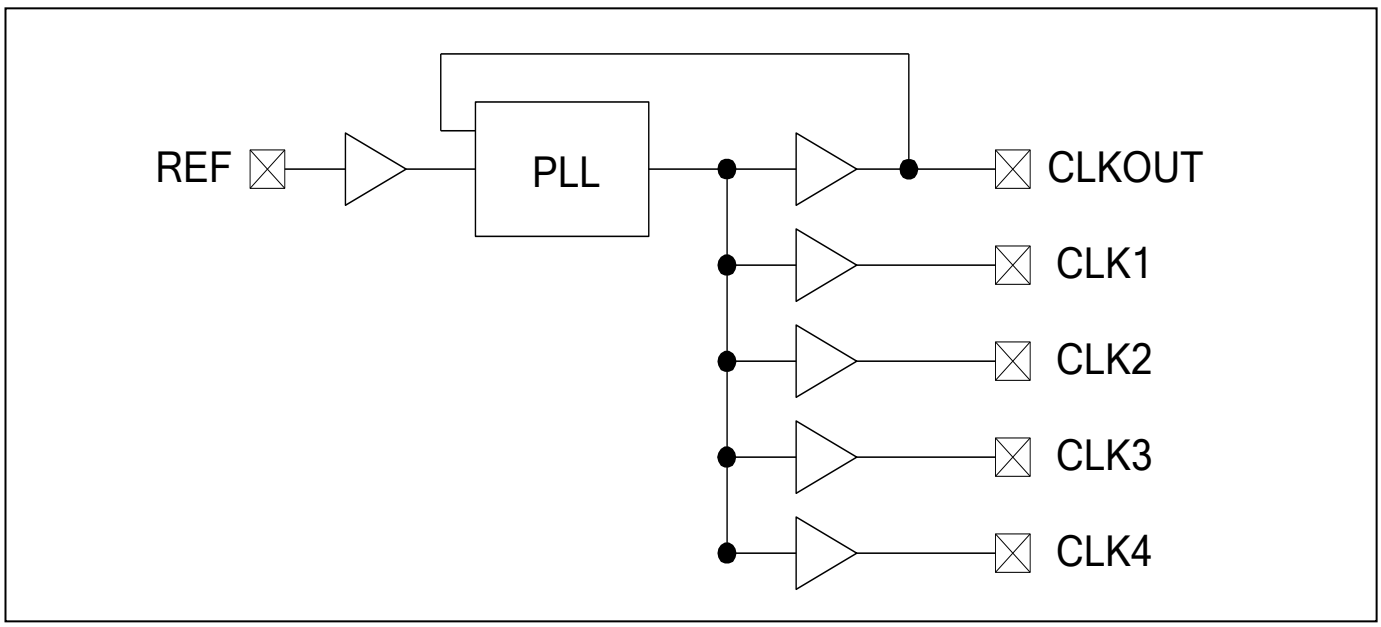
These parts are not intended for 5V input-tolerant applications.

PIN CONFIGURATION



SOP-8L

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Package Type	Type	Description
	SOP-8L		
REF[1]	1	I	Input reference frequency.
CLK2[2]	2	O	Buffered clock output.
CLK1[2]	3	O	Buffered clock output.
GND	4	P	Ground connection.
CLK3[2]	5	O	Buffered clock output.
VDD	6	P	VDD connection.
CLK4[2]	7	O	Buffered clock output.
CLKOUT[2,3]	8	O	Buffered clock output. Internal feed back on this pin.

Notes: 1: Weak pull-down. 2: Weak pull-down on all outputs.
3. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

INPUT / OUTPUT SKEW CONTROL

The PL123E-05 will achieve Zero Delay from input to output when all the outputs are loaded equally. Adjustments to the input/output delay can be made by adjusting the loading on the CLKOUT pin.

Please contact Micrel for more information.

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

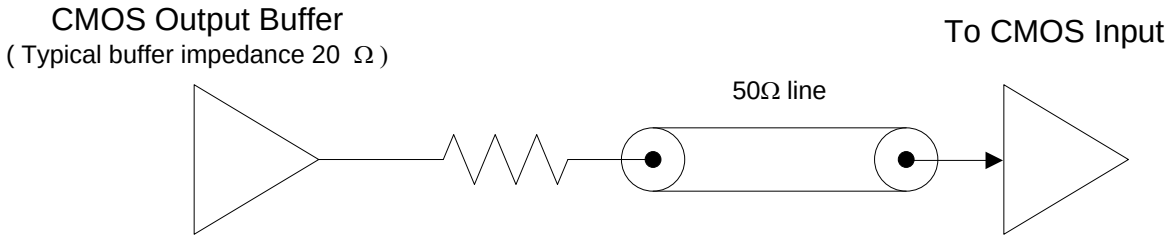
- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Connect a 33 Ω series resistor at each of the output clocks to enhance the stability of the output signal

Absolute Maximum Conditions

Supply Voltage to Ground Potential .....–0.5V to 4.6V
DC Input Voltage.....V_{SS} – 0.5V to 4.6V
Storage Temperature ..... –65°C to 150°C

Junction Temperature..... 150°C
Static Discharge Voltage
(per MIL-STD-883, Method 3015).....> 2000V

Operating Condition

Description	Parameter	Min	Max	Unit
Supply Voltage	V_{DD}	2.25	3.63	V
Load Capacitance, <100 MHz, 3.3V	C_L[4]	–	30	pF
Load Capacitance, <100 MHz, 2.5V with High Drive		–	30	pF
Load Capacitance, <133.3 MHz, 3.3V		–	22	pF
Load Capacitance, <133.3 MHz, 2.5V with High Drive		–	22	pF
Load Capacitance, <133.3 MHz, 2.5V with Standard Drive		–	15	pF
Load Capacitance, >133.3 MHz, 3.3V		–	15	pF
Load Capacitance, >133.3 MHz, 2.5V with High Drive		–	15	pF
Input Capacitance[5]	C_{IN}	–	5	pF
Closed-loop bandwidth (typical), 3.3V	BW	1		MHz
Closed-loop bandwidth (typical), 2.5V		0.5		MHz
Output Impedance (typical), 3.3V High Drive	R_{OUT}	23		Ω
Output Impedance (typical), 3.3V Standard Drive		33		Ω
Output Impedance (typical), 2.5V High Drive		26		Ω
Output Impedance (typical), 2.5V Standard Drive		39		Ω
Power-up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	t_{PU}	0.01	250	ms

Notes:
4. Applies to Test Circuit #1.
5. Applies to both REF Clock and internal feedback path on CLKOUT.
6. Theta Ja, EIA JEDEC 51 test board conditions, 2S2P; Theta Jc Mil-Spec 883E Method 1012.1.

3.3V DC Electrical Specifications

Description	Parameter	Test Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		2.97	3.63	V
Input LOW Voltage	V_{IL}		–	0.8	V
Input HIGH Voltage	V_{IH}		2.5	V_{DD} + 0.3	V
Input Leakage Current	I_{IL}	$0 < V_{IN} < V_{IL}$	–	±10	µA
Input HIGH Current	I_{IH}	$V_{IN} = V_{DD}$	–	100	µA
Output LOW Voltage	V_{OL}	I_{OL} = 8 mA (Standard Drive) I_{OL} = 12 mA (High Drive)	– –	0.4 0.4	V V
Output HIGH Voltage	V_{OH}	I_{OH} = –8 mA (Standard Drive) I_{OH} = –12 mA (High Drive)	2.4 2.4	– –	V V
Supply Current	I_{DD}	Unloaded outputs, 66-MHz REF	–	45	mA

2.5V DC Electrical Specifications

Description	Parameter	Test Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		2.25	2.75	V
Input LOW Voltage	V_{IL}		–	0.7	V
Input HIGH Voltage	V_{IH}		1.7	V_{DD} + 0.3	V
Input Leakage Current	I_{IL}	$0<V_{IN} < V_{DD}$	–	10	µA
Input HIGH Current	I_{IH}	$V_{IN} = V_{DD}$	–	100	µA
Output LOW Voltage	V_{OL}	I_{OL} = 8 mA (Standard Drive) I_{OL} = 12 mA (High Drive)	– –	0.5 0.5	V
Output HIGH Voltage	V_{OH}	I_{OH} = –8 mA (Standard Drive) I_{OH} = –12 mA (High Drive)	V_{DD} – 0.6 V_{DD} – 0.6	– –	V
Supply Current	I_{DD}	Unloaded outputs, 66-MHz REF	–	30	mA

3.3V and 2.5V AC Electrical Specifications

Description	Parameter	Test Conditions	Min	Typ	Max	Unit
Maximum Frequency[7] (Input/Output)	$1/t_1$	3.3V High Drive	10	–	220	MHz
		3.3V Standard Drive	10	–	167	MHz
		2.5V High Drive	10	–	200	MHz
		2.5V Standard Drive	10	–	134	MHz
Input Duty Cycle (PLL Mode only)	T_{IDC}	<133.3 MHz	25	–	75	%
		>133.3 MHz	40	–	60	%
Output Duty Cycle[8]	$t_2 \div t_1$	<133.3 MHz	47	–	53	%
		>133.3 MHz	45	–	55	%
Rise, Fall Time (3.3V)[8]	t_3,t_4	Standard Drive, CL = 30pF, <100 MHz	–	1.6	–	ns
		Standard Drive, CL = 22pF, <133.3 MHz	–	1.6	–	ns
		Standard Drive, CL = 15pF, <167 MHz	–	0.6	–	ns
		High Drive, CL = 30pF, <100 MHz	–	1.2	–	ns
		High Drive, CL = 22pF, <133.3 MHz	–	1.2	–	ns
		High Drive, CL = 15pF, >133.3 MHz	–	0.5	–	ns
Rise, Fall Time (2.5V)[8]	t_3, t_4	Standard Drive, CL = 15pF, <133.33 MHz	–	1.5	–	ns
		High Drive, CL = 30pF, <100 MHz	–	2.1	–	ns
		High Drive, CL = 22pF, <133.3 MHz	–	1.3	–	ns
		High Drive, CL = 15pF, >133.3 MHz	–	1.2	–	ns
Output to Output Skew [8]	t_5	All outputs equally loaded	–	–	100	ps
Delay, REF Rising Edge to CLKOUT Rising Edge[8]	t_6	PLL enabled @ 3.3V	–100	–	100	ps
		PLL enabled @2.5V	–200	–	200	ps
Part to Part Skew[8]	t_7	Measured at $V_{DD}/2$. Any output to any output, 3.3V supply	–	–	±150	ps
		Measured at $V_{DD}/2$. Any output to any output, 2.5V supply	–	–	±300	ps
PLL Lock Time[8]	t_{LOCK}	Stable power supply, valid clocks pre-sented on REF and CLKOUT pins	–	–	1.0	ms
Cycle-to-Cycle Jitter, Peak[8,9]	T_{JCC}	3.3V, >66 MHz, <15pF	–	–	55	ps
		3.3V, >66 MHz, <30pF, Standard. Drive	–	–	125	ps
		3.3V, >66 MHz, <30pF, High Drive	–	–	100	ps
		2.5V, >66 MHz, <15pF, Standard. Drive	–	–	100	ps
		2.5V, >66 MHz, <15pF, High Drive	–	–	80	ps
		2.5V, >66 MHz, <30pF, High Drive	–	–	125	ps

3.3V and 2.5V AC Electrical Specifications (continued)

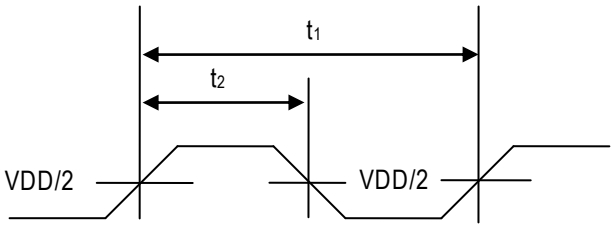
Description	Parameter	Test Conditions	Min	Typ	Max	Unit
Period Jitter, Peak[8,9]	T_{PER}	3.3V, 66–100 MHz, <15 pF	–	–	60	ps
		3.3V, >100 MHz, <15 pF	–	–	35	ps
		3.3V, >66 MHz, <30 pF, Standard Drive	–	–	75	ps
		3.3V, >66 MHz, <30 pF, High Drive	–	–	70	ps
		2.5V, >66 MHz, <15 pF, Standard. Drive	–	–	60	ps
		2.5V, 66–100 MHz, <15 pF, High Drive	–	–	60	ps
		2.5V, >100 MHz, <15 pF, High Drive	–	–	45	ps

Notes:

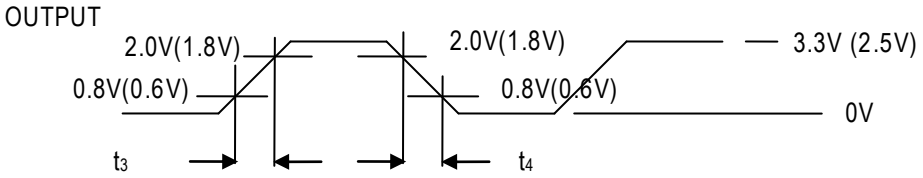
7. For the given maximum loading conditions. See C_L in Operating Conditions Table.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.
9. Typical jitter is measured at 3.3V or 2.5V, 29°C, with all outputs driven into the maximum specified load.

SWITCHING WAVEFORMS

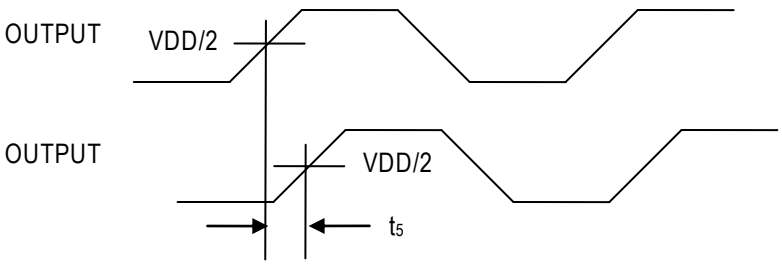
Duty Cycle Timing



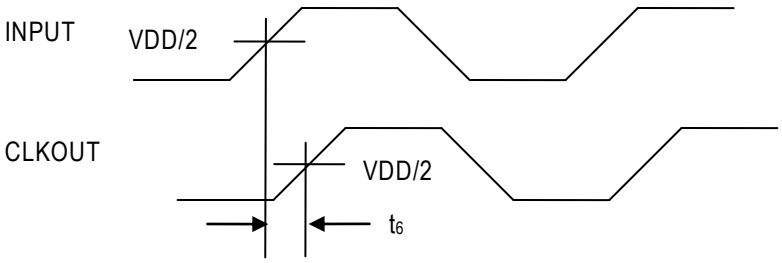
All Outputs Rise/Fall Time



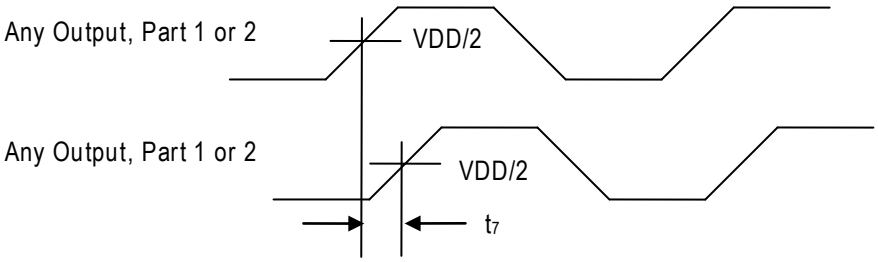
Output-Output Skew



Input-Output Propagation Delay

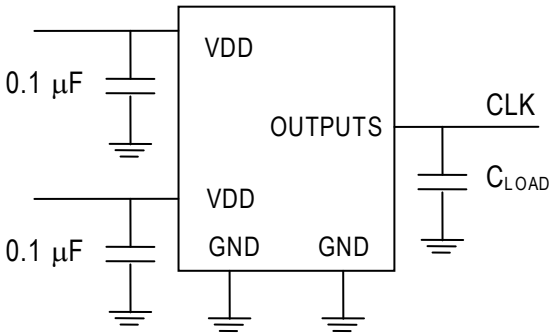


Device-Device Skew



TEST CIRCUITS

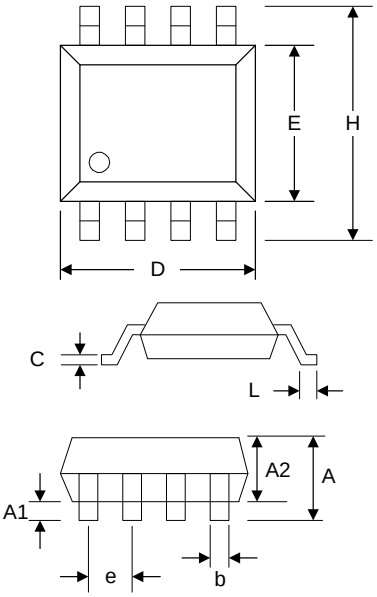
Test Circuit #1



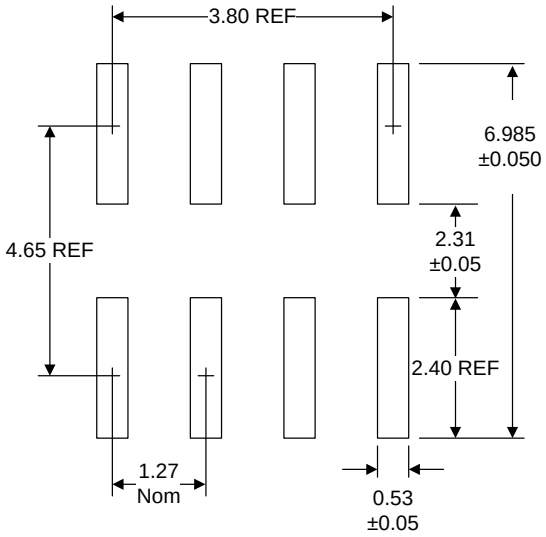
PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

SOP-8L

Symbol	Dimension (MM)	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



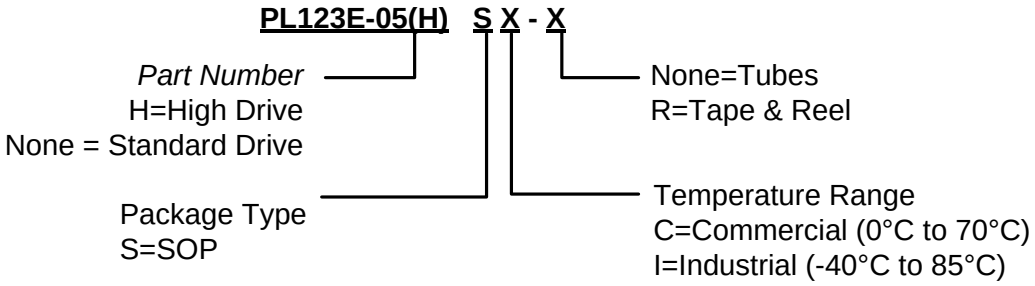
Recommended Land Pattern (MM)



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



Part/Order Number	Marking*	Package Option
PL123E-05SC	P123E05 SC LLLLL	8-Pin SOP Tube
PL123E-05SC-R		8-Pin SOP (Tape and Reel)
PL123E-05HSC	P123E05H SC LLLLL	8-Pin SOP Tube
PL123E-05HSC-R		8-Pin SOP (Tape and Reel)
PL123E-05SI	P123E05 SI LLLLL	8-Pin SOP Tube
PL123E-05SI-R		8-Pin SOP (Tape and Reel)
PL123E-05HSI	P123E05H SI LLLLL	8-Pin SOP Tube
PL123E-05HSI-R		8-Pin SOP (Tape and Reel)

***Note:** **LLLLL designates lot number**