UA5M20MC Datasheet

CENTELLAX

5 - 20GHz MMIC Amplifier with Integrated Bias

Application

The UA5M20MC MMIC Amplifier with Integrated Bias is designed for digital radio, spread spectrum, electronic warfare, and broadband communication systems. It can be used as a LO or mixer isolation amplifier, a transmit amplifier in a radio system, or as a general isolation and gain block amplifier.

Description

The UA5M20MC is a two-stage PHEMT high gain amplifier designed to be insensitive to process or temperature changes. Its high isolation make it ideal for applications requiring both gain and isolation. The device can be operated at 5V 135mA, or 3.3V 108mA for integration with mixed-signal circuitry.

Features

The UA5M20MC is typically self-biased for low-cost Class-A operation, requiring only a single 5V supply; both drain and both gate pads are available for higher-efficiency operation. The device is AC coupled with integrated blocking capacitors.

Device Highlights

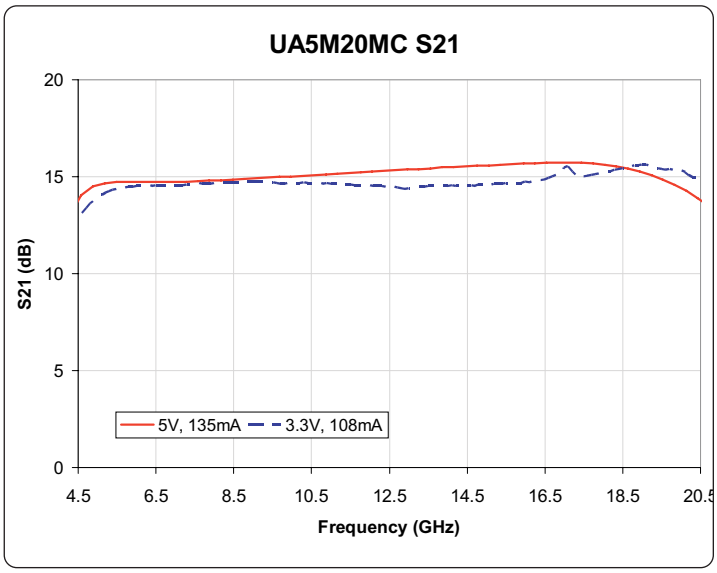
- Excellent performance 5-18GHz:
  - High, flat gain (15 ± 0.5dB)
  - Good return loss (15dB)
  - 17.5dBm P_{-1dB}, 20dBm P_{sat}
- Mixed-signal 3.3V operation:
  - Similar small-signal performance
  - Good power (16.5dBm P_{sat})
- Quick and easy to use:
  - Self-biasing (5V or 3.3V supply)
  - Integrated blocking capacitors
- Very high isolation (-36dB)
- 100% DC, RF, and visually tested
- Size: 920x920um (36.2x36.2mil)

Key Specifications

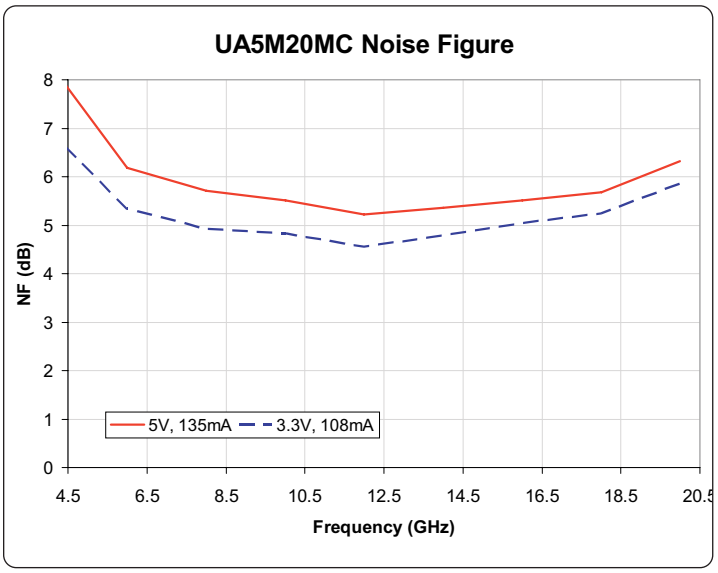
Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

Vdd1=Vdd2=5.0V, Vg1=Vg2=N/C, Idd1=65mA, Idd2=90mA, Zo=50Ω

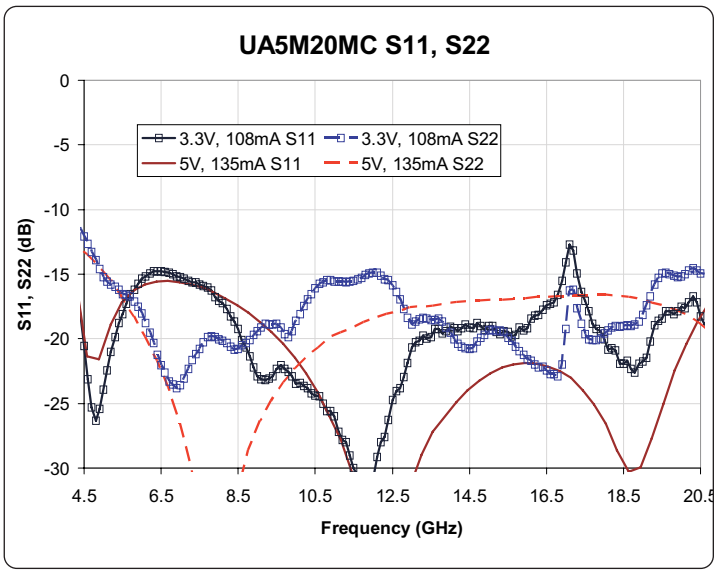
Parameter	Description	5 - 18GHz			4.5 - 20GHz		
		Min	Typ	Max	Min	Typ	Max
S21 (dB)	Small Signal Gain	14	15		12.5	14.5	
Flatness (±dB)	Gain Flatness		0.5	0.8		1.0	2.0
S11 (dB)	Input Match		-15	-13		-15	-13
S22 (dB)	Output Match		-17	-11.5		-17	-12
S12 (dB)	Reverse Isolation		-36	-32		-36	-32
P_{-1dB} (dBm)	1dB Compressed Output Power	16	17.5			17	
P_{sat} (dBm)	Saturated Output Power	19	20		18.5	20	
NF (dB)	Noise Figure		7			7.5	



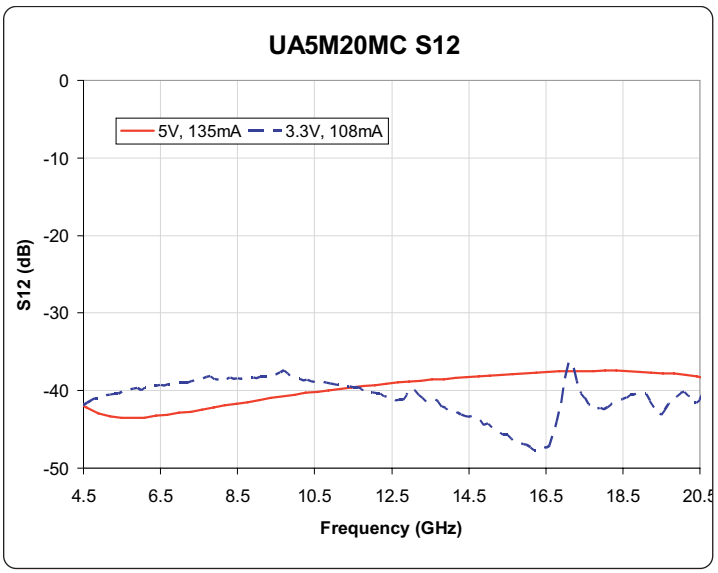
Typical IC performance measured on-wafer



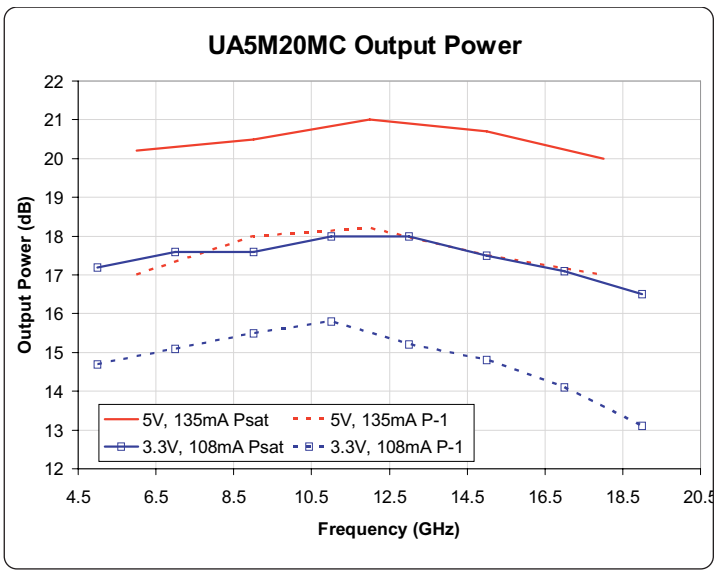
Typical IC performance with package de-embedded



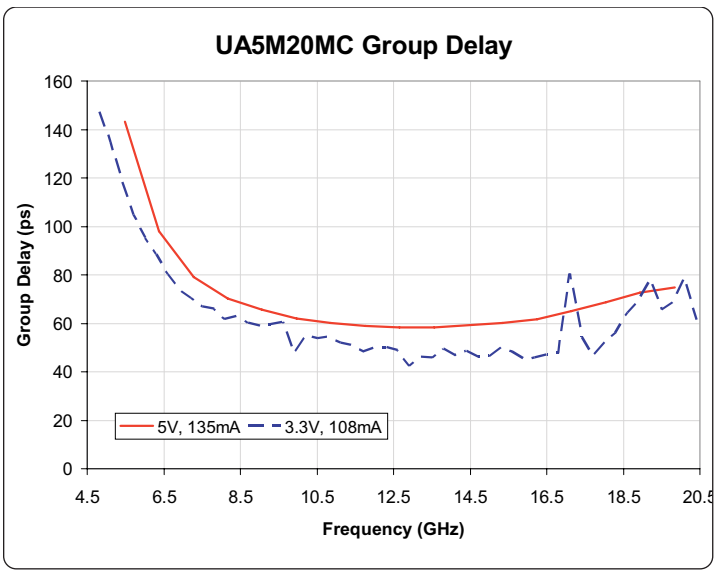
Typical IC performance measured on-wafer



Typical IC performance measured on-wafer



Typical IC performance measured on-wafer



Typical IC performance measured on-wafer

Typical measurement data is available upon request. Email support@centellax.com for more information.

Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vdd1	Drain Bias Voltage FET1	3V	5V	6V
Idd1	Drain Bias Current FET1	—	65mA	90mA
Vdd2	Drain Bias Voltage FET2	3V	5V	6V
Idd2	Drain Bias Current FET2	—	90mA	110mA
Vgg1	Gate Bias Voltage FET1	-4V	N/C	+1V
Vgg2	Gate Bias Voltage FET2	-4V	N/C	+1V
P_{in}	Input Power (CW)			12dBm
P_{dc}	Power Dissipation		0.675W	
T_{ch}	Channel Temperature			150°C
Θ_{ch}	Thermal Resistance (T_{case}=85°C)		60°C/W	

DC Bias

The UA5M20MC is typically biased by applying +5V to the two drain pads (Vdd1, Vdd2); the gates (Vgg1, Vgg2) will self-bias.

All four bias lines are available on-chip; both drains and both gates can be biased to different potentials. Grounded bond wires are not required, as the backside of the chip is both an RF and DC ground.

Negative potentials applied to the gates will reduce the drain current in that stage. This will increase the amplifier's efficiency by moving its operation closer to Class AB or B.

The UA5M20MC can also be biased with +3.3V drain voltage. This yields good performance with the same supply used for mixed-signal circuitry or microprocessors.

Gain Control

Some gain control is available when operating the amplifier in the linear gain region. Negative voltage applied to Vgg1 and Vgg2 will reduce the amplifier gain. Additionally, Vdd1 and Vdd2 can also be used for linear low-frequency amplitude modulation.

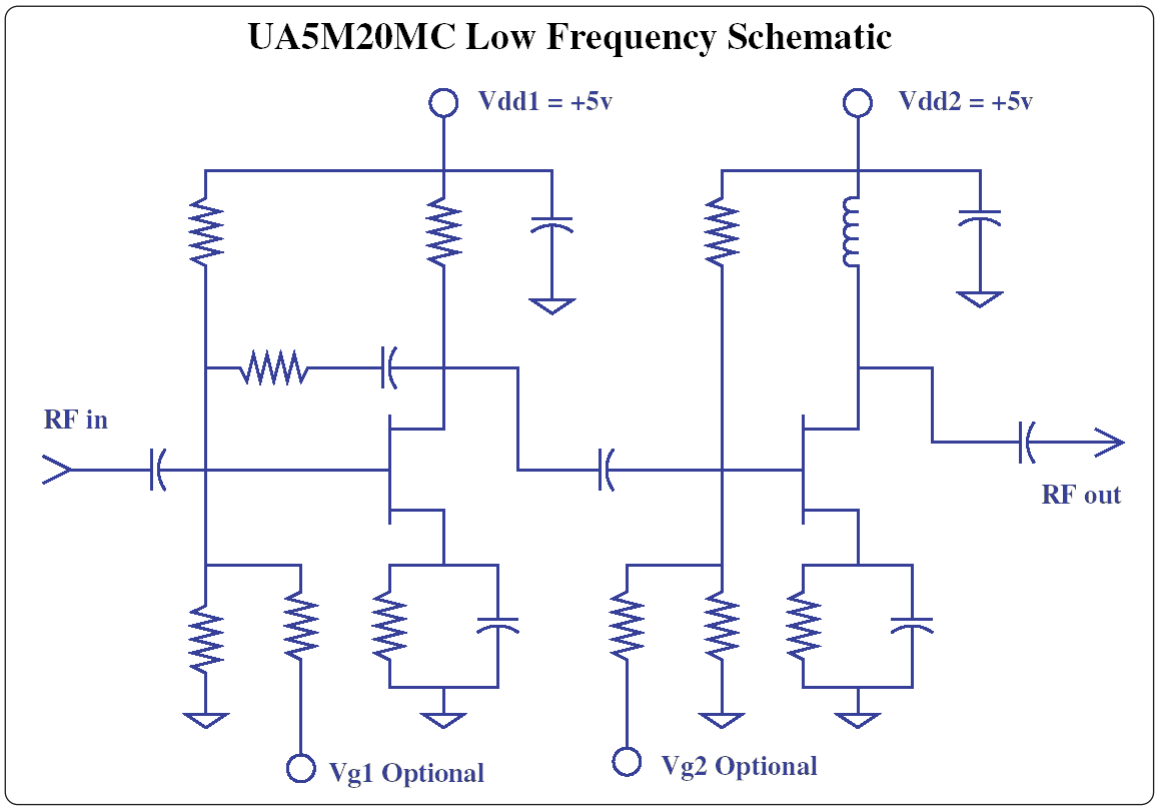
Matching

The UA5M20MC has been designed with input and output impedances that best match a 50ohm system, and require no external matching networks.

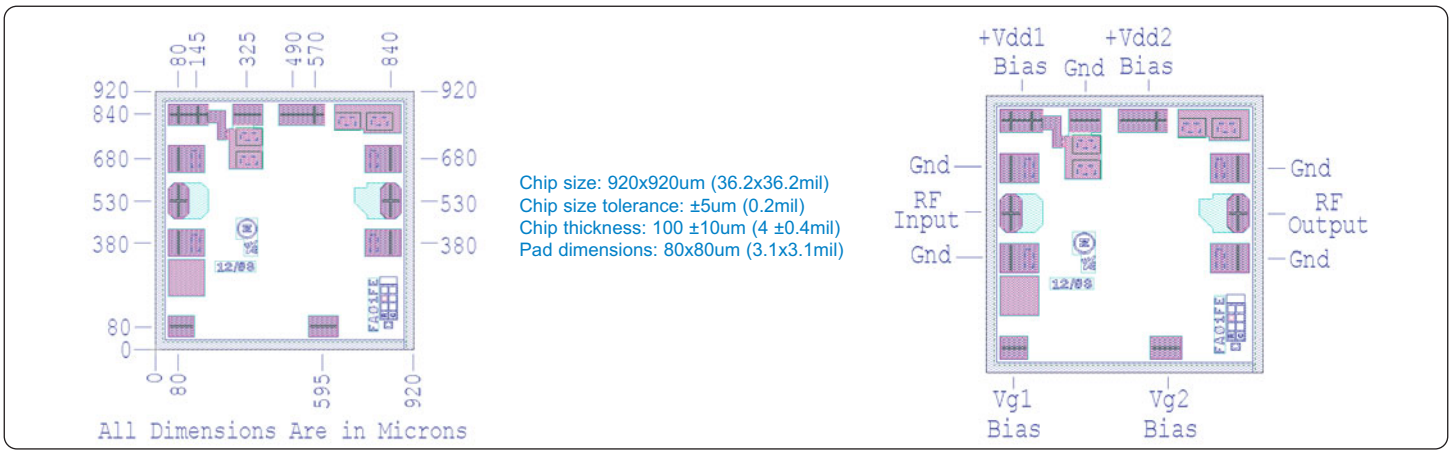
Best performance will be obtained by using multiple short bondwires, or by using ribbon or mesh bondwires.

DC Blocks

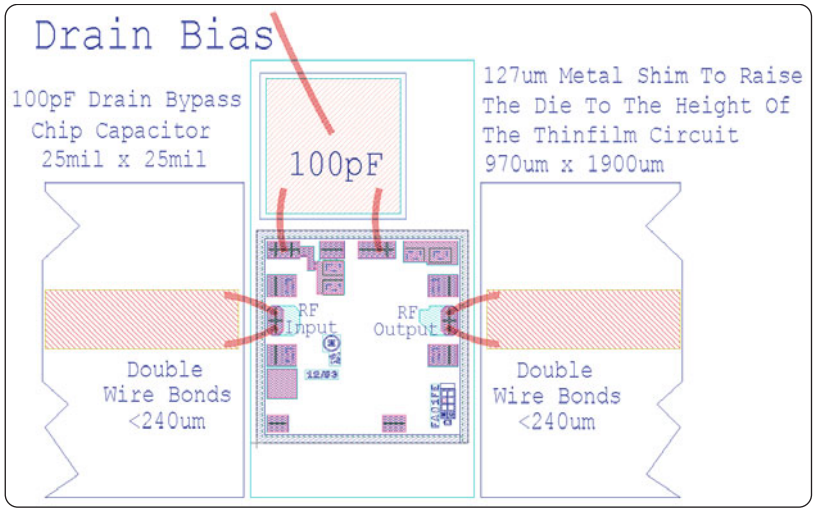
The amplifier is internally AC coupled to the RF input and output pads. DC blocking capacitors are not required for isolating bias voltages from external circuitry.



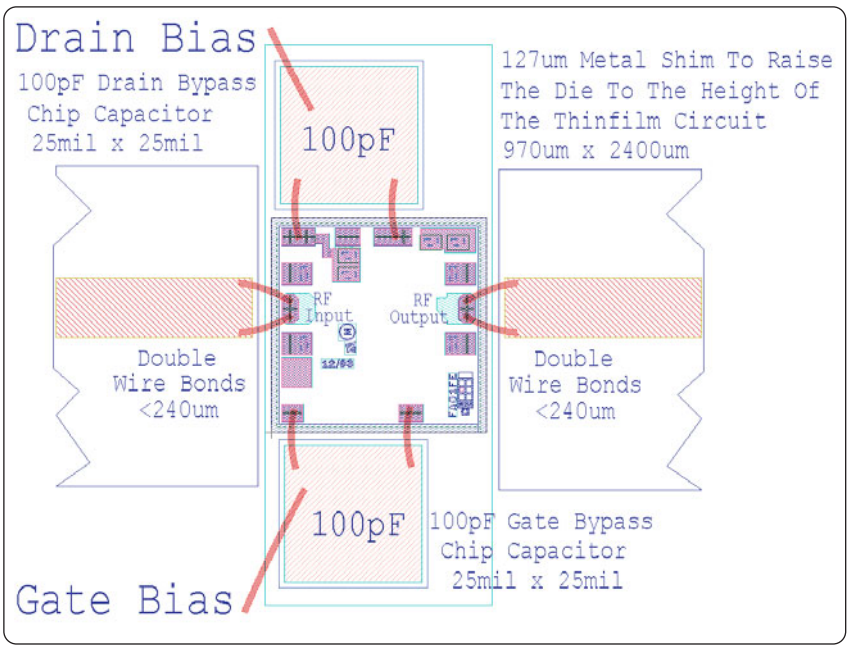
UA5M20MC Datasheet



Die size, pad locations, and pad descriptions



Single supply (self-biased) assembly diagram



Dual supply (externally-biased) assembly diagram

Applications Support

Alternate assembly diagrams and other additional application support are available upon request. Visit the Centellax website for large printable assembly diagrams and application notes: http://www.centellax.com/products/microwave/mmics/UA5M20MC.shtml.

Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center**; handle from edges or with a custom collet.

Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking.

ESD Handling and Bonding:

This MMIC is ESD sensitive; preventive measures should be taken during handling, die attach, and bonding.

Epoxy die attach is recommended. Please visit our website for more handling, die attach and bonding information: http://www.centellax.com/.

Recommended Components

>100pF 25x25mil Bypass Capacitor:
Presidio SL2525X7R101K16VH