

2 - 50GHz Power Amplifier

Features

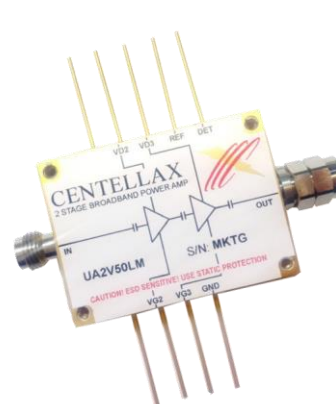
- 30dBm output power @ 10GHz
- 26dBm output power @ 40GHz
- 18dB gain to 26GHz
- 15dB gain to 40GHz
- Useful gain and power to 50GHz
- 10.6W power dissipation
- Small size
- ECCN 3A001.b.4.c

Description

The UA2V50LM Amplifier is a broadband, high power, moderate gain instrumentation grade amplifier. The amplifier was designed to provide exceptional gain flatness per octave over greater than 5 octaves of frequency coverage. The 2 GHz to 50 GHz amplifier provides up to 18dB of gain and 30 dBm output power with low harmonics and low residual phase noise.

Application

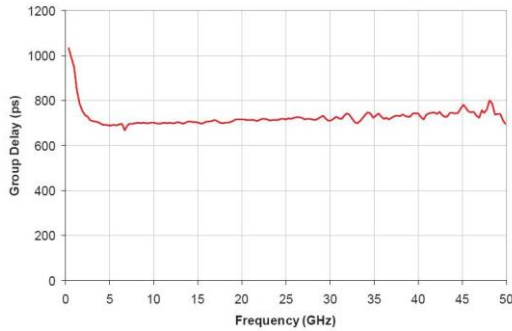
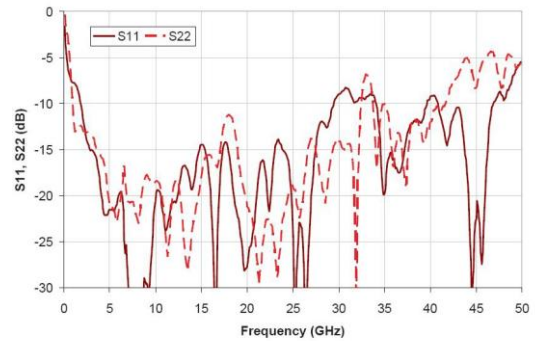
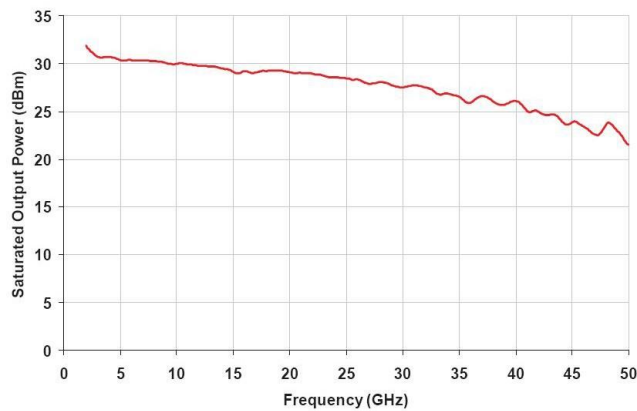
The UA2V50LM Amplifier is an ideal selection for laboratory and instrumentation systems where a high performance broadband RF power amplifier is required. Examples include use as a post amplifier for synthesizers, mixers, modulators, etc. where output powers are low and need to be increased to the 20dBm to 30dBm range. The amplifier was designed for use in communications systems, test equipment, military systems, etc.



Key Characteristics @ 25°C: VD1 = VD2 = 6V; VD3 = 7V; Vg1 = Vg2 = Vg3 = -0.1V; Zo = 50Ω

| Parameter | Description | Min | Typ | Max | Min | Typ | Max |
|-----------|-------------------|-----|-----|-----|-----|-----|-----|
| S21 (dB) | Small Signal Gain | 15 | 18 | - | 12 | 15 | - |
| S11 (dB) | Input Match | - | -10 | -8 | - | -8 | -5 |
| S22 (dB) | Output Match | - | -12 | -10 | - | -8 | -5 |
| S12 (dB) | Reverse Isolation | - | 28 | - | - | 25 | - |

Typical Performance

UA2V50LM Group Delay

UA2V50LM S11, S22

UA2V50LM Saturated Output Power


Supplemental Specifications¹

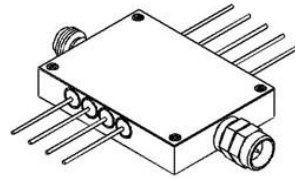
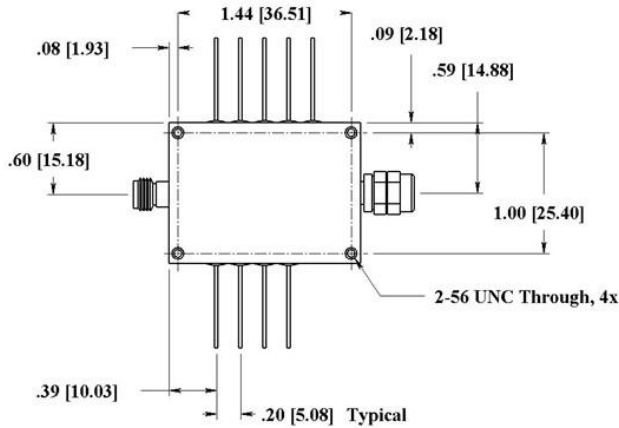
| Parameter | Description | Minimum | Typ | Maximum |
|-----------|---------------------------|---------|-----------|---------|
| Vd2 (V) | Drain Bias Voltage FET2 | - | 6 | 8 |
| Vg2 (V) | Gate Bias Voltage FET2 | -4 | -0.2 to 0 | 0.5 |
| Idd2 (mA) | Drain Bias Current FET2 | - | 600 | 1000 |
| Vd3 (V) | Dain Bias Voltage FET3 | - | 6 | 8 |
| Vg3 (V) | Gate Bias Voltage FET3 | -4 | -0.2 to 0 | 0.5 |
| Idd3 | Drain Bias Current FET3 | - | 1000 | 1200 |
| Pin | Input Power (CW) | - | - | 28 dBm |
| Pdc | Power Dissipation | - | 10.6 | - |
| Tbs | Backside Case Temperature | - | - | 75°C |

Note:

It is recommended to apply gate bias voltages before drain bias voltages, however, it is not necessary to absolutely guarantee this sequence. This device is robust and will survive drain voltages being applied before gate voltages.

¹Operation listed under the Supplemental Specifications may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Operating Specifications is not implied. Prolonged use at the absolute maximum rating conditions may affect device reliability.

Physical Dimensions and Pin Assignment

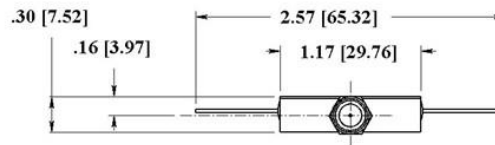
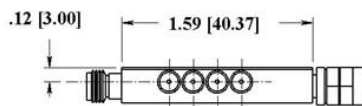


Physical Characteristics

(all measurements in inches[mm])

Tolerance typically
+/- 0.0025in
(+/- 0.0635mm)

DC pin diameter is
0.03in [0.76mm]



| Pin | Function | Operational Notes |
|-------|--------------------------------|--|
| RFin | RF input | V-connector (female) |
| RFout | RF output | V-connector (male) |
| Vg2 | 1st stage gate bias | Set at typical operating specification |
| Vg3 | 2nd stage gate bias | Set at typical operating specification |
| Vd2 | 1st stage drain bias | Set at typical operating specification |
| Vd3 | 2nd stage drain bias | Set at typical operating specification |
| Ref | DC reference offset (optional) | Remove this offset from the detector voltage (see appnote MM-AAP-004) |
| Det | RF power detector (optional) | Remove the DC offset from this signal and linearize (see appnote MM-AAP-004) |
| Gnd | Connected | Connected to Ground |

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