

## DC to 30GHz Broadband MMIC Medium-Power Amplifier

### Features

- Power and gain from 1.5-20GHz:
  - 24.5dBm Psat, 17.5dB gain
- Great 0.04-26.5GHz performance:
  - Flat gain (16.5 ± 1.25dB)
  - High Psat at 26.5GHz (23.5dBm)
  - High P1dB at 26.5GHz (19dBm)
- Good input / output return loss
- High isolation
- >30dB dynamic gain control
- Integrated temperature-referenced power detector output
- 100% DC, RF, and visually tested
- Size: 2390x920um (94.1x36.2mil)

### Description

The MMA023AA is an eight stage traveling wave amplifier. The amplifier has been designed for power, flat gain, and good return loss to 30GHz. The amplifier typically has 24.5dBm Psat and 17.5dB gain from 1.5-20GHz, and 22dBm Psat from 0.04-30GHz.

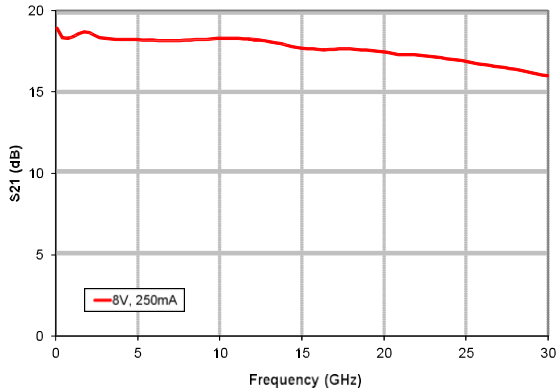
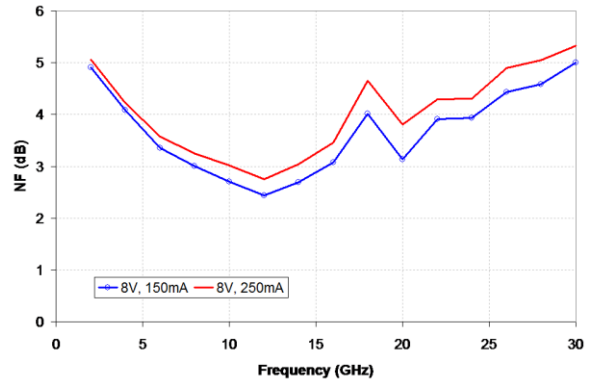
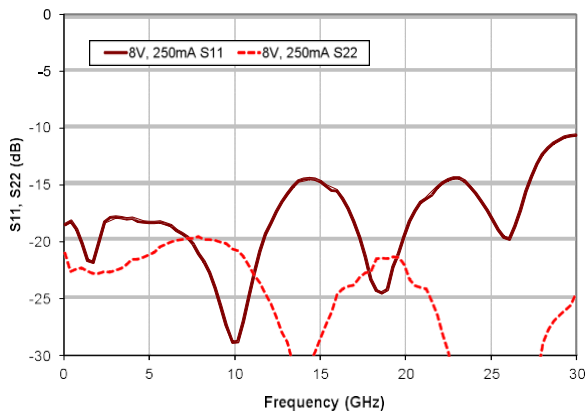
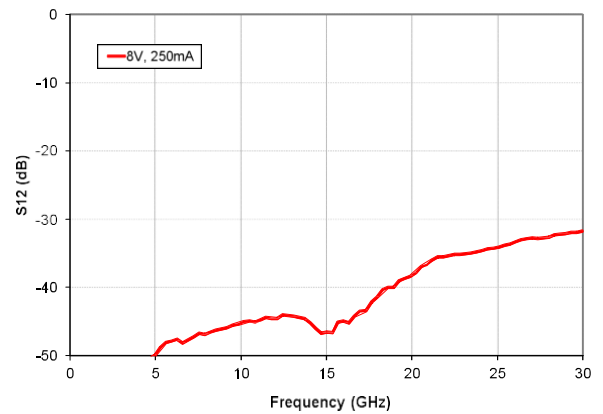
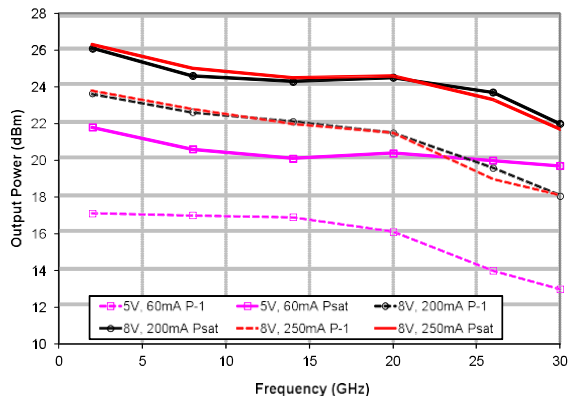
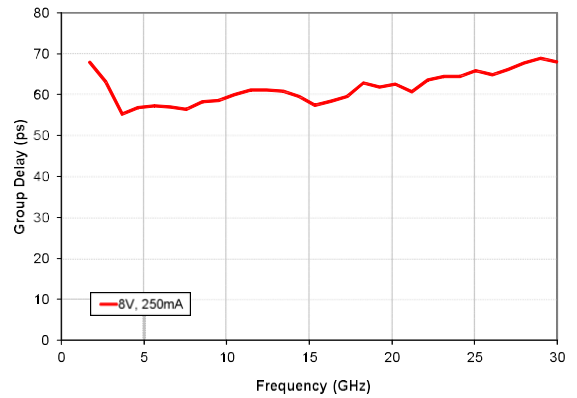
### Application

The MMA023AA Broadband MMIC Medium-Power Amplifier is designed for broadband power applications in RF and microwave communications, test equipment and military systems. By using specific external components, the bandwidth of operation can be extended below 40MHz.

**Key Characteristics:** Vdd=8.0V, Idd=250mA, Zo=50Ω

Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

| Parameter                 | Description                 | 1.5 - 20GHz |      |      | 0.04 - 26.5GHz |      |     | 0.04 - 30GHz |      |     |
|---------------------------|-----------------------------|-------------|------|------|----------------|------|-----|--------------|------|-----|
|                           |                             | Min         | Typ  | Max  | Min            | Typ  | Max | Min          | Typ  | Max |
| S21 (dB)                  | Small Signal Gain           | 16          | 17.5 | -    | 15             | 16.5 | -   | 14           | 15.5 | -   |
| Flatness (±dB)            | Gain Flatness               | -           | 0.75 | 1.25 | -              | 1.25 | 1.5 | -            | 1.5  | 2.0 |
| S11 (dB)                  | Input Match                 | -           | -15  | -12  | -              | -14  | -11 | -            | -10  | -8  |
| S22 (dB)                  | Output Match                | -           | -20  | -15  | -              | -20  | -15 | -            | -20  | -15 |
| S12 (dB)                  | Reverse Isolation           | -           | -37  | -30  | -              | -33  | -25 | -            | -31  | -25 |
| P1dB (dBm)                | 1dB Compressed Output Power | 20          | 21.5 | -    | 17.5           | 19   | -   | 16.5         | 18   | -   |
| Psat (dBm)                | Saturated Output Power      | 23          | 24.5 | -    | 22             | 23.5 | -   | 20.5         | 22   | -   |
| Pout @ 16dB (dBm)         | Output Power at 16dB Gain   | 21          | 23   | -    | -              | -    | -   | -            | -    | -   |
| NF (dB)                   | Noise Figure                | -           | 5.5  | -    | -              | 5.5  | -   | -            | 5.5  | -   |
| RF <sub>det</sub> (mV/mW) | RF Detector Sensitivity     | -           | 0.8  | -    | -              | 0.8  | -   | -            | 0.8  | -   |

**S21**

*Typical IC performance measured on-wafer*
**Noise Figure**

*Typical IC performance with package de-embedded*
**S11, S22**

*Typical IC performance measured on-wafer*
**S12**

*Typical IC performance measured on-wafer*
**Output Power**

*Typical IC performance measured on-wafer*
**Group Delay**

*Typical IC performance measured on-wafer*

**Table 1: Supplemental Specifications**

| Parameter       | Description                                  | Min                                    | Typ     | Max   |
|-----------------|--|--|---------|-------|
| V <sub>dd</sub> | Drain Bias Voltage                           | 3V                                     | 8V      | 8.2V  |
| I <sub>dd</sub> | Drain Bias Current                           | -                                      | 250mA   | 375mA |
| V <sub>g1</sub> | 1st Gate Bias Voltage                        | -4V                                    | -       | +0.5V |
| V <sub>g2</sub> | 2nd Gate Bias Voltage                        | V <sub>dd</sub> - V <sub>g2</sub> < 7V | N/C     | +4V   |
| P <sub>in</sub> | Input Power (CW)                             | -                                      | -       | 22dBm |
| P <sub>dc</sub> | Power Dissipation                            | -                                      | 2.0W    | -     |
| T <sub>ch</sub> | Channel Temperature                          | -                                      | -       | 150°C |
| Θ <sub>ch</sub> | Thermal Resistance (T <sub>case</sub> =85°C) | -                                      | 20° C/W | -     |



Caution, ESD  
Sensitive Device

**DC Bias:**

The MMA023AA is biased by applying a positive voltage to the drain ( $V_{dd}$ ), then setting the drain current ( $I_{dd}$ ) using a negative voltage on the gate ( $V_{g1}$ ).

When zero volts is applied to the gate, the drain to source channel is open; this results in high  $I_{dd}$ . When  $V_{g1}$  is biased negatively, the channel is pinched off and  $I_{dd}$  decreases.

The nominal bias is  $V_{dd}=8.0V$ ,  $I_{dd}=250mA$ . Improved noise or power performance can be achieved with application-specific biasing.

**Gain Control:**

Dynamic gain control is available when operating the amplifier in the linear gain region. Negative voltage applied to the second gate ( $V_{g2}$ ) reduces amplifier gain.

**RF Power Detection:**

RF output power can be calculated from the difference between the RF detector voltage and the DC detector voltage, minus a DC offset. Please consult the power detector application note available from the Microsemi webpage.

**Low-Frequency Use:**

The MMA023AA has been designed so that the bandwidth can be extended to low frequencies. The low end corner frequency of the device is primarily determined by the external biasing and AC coupling circuitry.

**Matching:**

The amplifier incorporates on-chip termination resistors on the RF input and output. These resistors are RF grounded through on-chip capacitors, which are small and become open circuits at frequencies below 1GHz.

A pair of gate and drain termination bypass pads are provided for connecting external capacitors required for the low frequency extension network. These capacitors should be 10x the value of the DC blocking capacitors.

**DC Blocks:**

The amplifier is DC coupled to the RF input and output pads; DC voltage on these pads must be isolated from external circuitry.

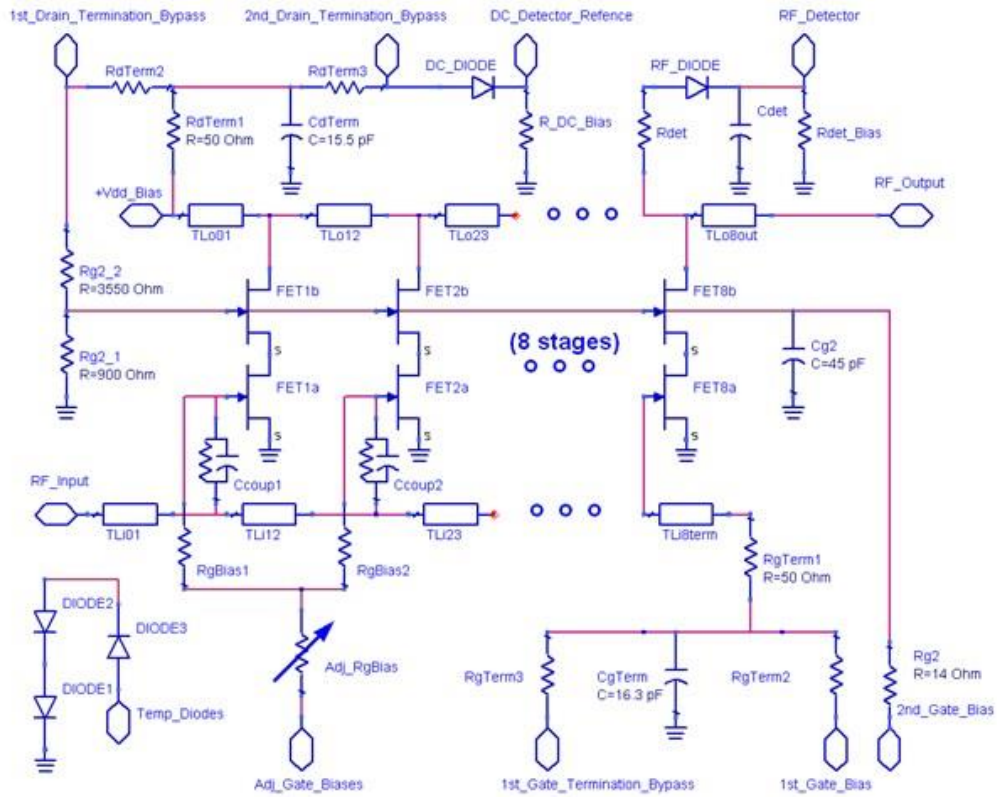
For operation above 2GHz, a series DC-blocking capacitor with minimum value of 20pF is recommended; operation above 40MHz requires a minimum of 120pF.

**Bias Inductor:**

DC bias applied to the drain ( $V_{dd}$ ) must be decoupled with an off-chip RF choke inductor. The amount of bias inductance will determine the low frequency operating point. Inductive biasing can also be applied to the chip through the RF output.

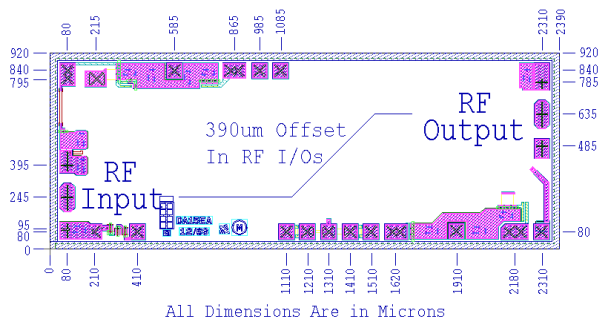
For many applications above 2GHz, a bondwire from the  $V_{dd}$  pad will suffice as the biasing inductor. Ensure the correct bond length as shown in the assembly diagrams.

## Simplified Circuit Schematic

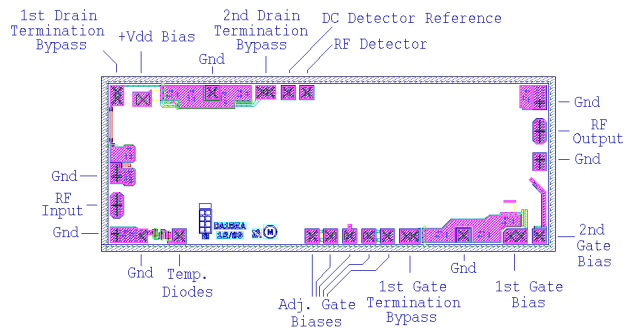


## Die size, pad locations, and pad descriptions

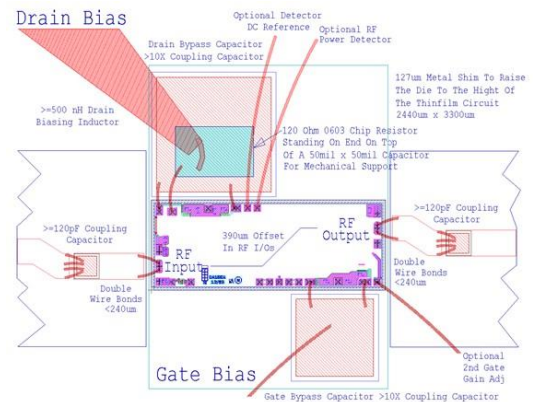
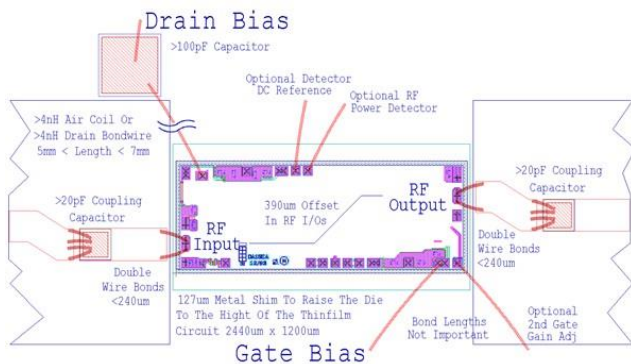
Chip size: 2390x920um (94.1x36.2mil)  
 Chip size tolerance: ±5um (0.2mil)  
 Chip thickness: 100 ±10um (4 ±0.4mil)  
 Pad dimensions: 80x80um (3.1x3.1mil)



**30GHz bonding diagram**



**40MHz - 30GHz bonding diagram**



### Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center**; handle from edges or with a custom collet.

### Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking.

### ESD Handling and Bonding:

**This MMIC is ESD sensitive**; preventive measures should be taken during handling, die attach, and bonding.

**Epoxy die attach is recommended.** Please review our application note MM-APP-0001 handling and die attach recommendations, on our website for more handling, die attach and bonding information.

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