SG1842/SG1843 Series

CURRENT MODE PWM CONTROLLER

PRODUCTION DATA SHEET

DESCRIPTION

The SG1842/43 family of control IC's provides all the necessary features to implement off-line fixed frequency, current-mode switching power supplies with a minimum number of external components. Current-mode architecture demonstrates improved line regulation, improved load regulation, pulse-by-pulse current limiting and inherent protection of the power supply output switch. The bandgap reference is trimmed to ±1% over temperature. Oscillator discharge current is trimmed to less than ±10%. The SG1842/43 has under-voltage lockout, current limiting circuitry and start-up current of less than 1mA. The totem-pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N channel device.

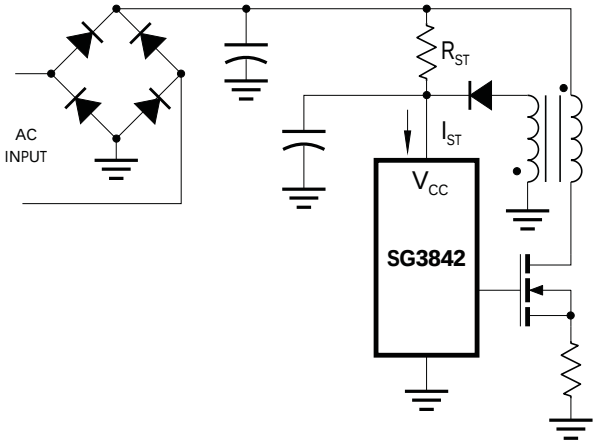
The SG1842/43 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2842/43 is specified for the industrial range of -25°C to 85°C, and the SG3842/43 is designed for the commercial range of 0°C to 70°C.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- OPTIMIZED FOR OFF-LINE CONTROL
- LOW START-UP CURRENT (<1mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- TRIMMED OSCILLATOR DISCHARGE CURRENT
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH 6V HYSTERESIS (SG1842 only)
- DOUBLE-PULSE SUPPRESSION
- HIGH-CURRENT TOTEM-POLE OUTPUT (1AMP PEAK)
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500KHZ OPERATION
- UNDERVOLTAGE LOCKOUT
  SG1842 - 16 volts
  SG1843 - 8.4 volts
- LOW SHOOT-THROUGH CURRENT <75mA OVER TEMPERATURE

PRODUCT HIGHLIGHT



HIGH RELIABILITY FEATURES

- AVAILABLE TO MIL-STD-883B AND DSCC
- SCHEDULED FOR MIL-M38510 QPL LISTING
- RADIATION DATA AVAILABLE
- Microsemi LEVEL "S" PROCESSING AVAILABLE

PACKAGE ORDER INFO

T_A (°C)	M Plastic DIP 8-Pin	N Plastic DIP 14-Pin	DM Plastic SOIC 8-Pin	D Plastic SOIC 14-Pin	Y Ceramic Dip 8-Pin	J Ceramic DIP 14-Pin	F Cer Flatpack 10-Pin	L Ceramic LCC 20-Pin
	RoHS / Pb-free Transition DC: 0503		RoHS / Pb-free Transition DC:0440					
0 to 70	SG3842M SG3843M	SG3842N SG3843N	SG3842DM SG3843DM	SG3842D SG3843D	SG3842Y SG3843Y	SG3842J SG3842J		
-25 to 85	SG2842M SG2843M	SG2842N SG2843N	SG2842DM SG2843DM	SG2842D SG2843D	SG2842Y SG2843Y	SG2842J SG2843J		
-55 to 125					SG1842Y SG1843Y	SG1842J SG1843J	SG1842F SG1843F	SG1842L SG1842L
MIL-STD/883					SG1842Y/883B SG1843Y/883B	SG1842J/883B SG1843J/883B	SG1842F/883B SG1843F/883B	SG1842L/883B SG1843L/883B
DESC					SG1842Y/DESC SG1843Y/DESC	SG1842J/DESC SG1843J/DESC	SG1842F/DESC SG1843F/DESC	SG1842L/DESC SG1843L/DESC

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. SG2843DM-TR)
Plastic packages are RoHS compliant

Rev. 1.6b 2010-03-15

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

Supply Voltage (I_{CC} < 30mA) ..... Self Limiting
Supply Voltage (Low Impedance Source) 30V
Output Current (Peak) ..... ±1A
Output Current (Continuous) 350mA
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) ..... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at T_A = 25°C (DIL-8) 1W
Operating Junction Temperature
  Hermetic (J, Y, F, L Packages) ..... 150°C
  Plastic (N, M, D, DM Packages) ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C
Pb-free / RoHS Peak Package Solder Reflow Temp. (40 second max. exposure)..... 260°C (+0, -5)

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. All voltages are with respect to Pin 5. All currents are positive into the specified terminal.

THERMAL DATA

M PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	95°C/W

N PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	65°C/W

DM PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	165°C/W

D PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	120°C/W

Y PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	130°C/W

J PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	80°C/W

F PACKAGE:

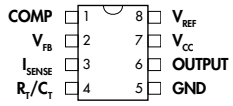
THERMAL RESISTANCE-JUNCTION TO CASE, θ_{JC}	80°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	145°C/W

L PACKAGE:

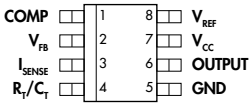
THERMAL RESISTANCE-JUNCTION TO CASE, θ_{JC}	35°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	120°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

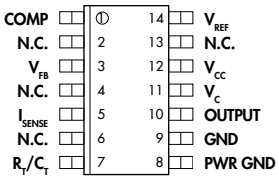
PACKAGE PIN OUTS



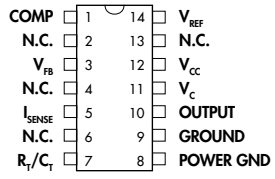
M & Y PACKAGE
(Top View)
M Package: Pb-free / RoHS 100% Matte Tin Lead Finish



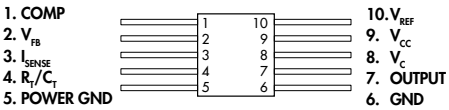
DM PACKAGE
(Top View)
Pb-free / RoHS 100% Matte Tin Lead Finish



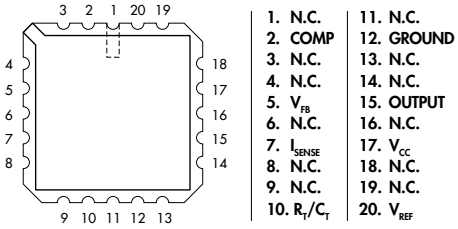
D PACKAGE
(Top View)
Pb-free / RoHS 100% Matte Tin Lead Finish



J & N PACKAGE
(Top View)
N Package: Pb-free / RoHS 100% Matte Tin Lead Finish



F PACKAGE
(Top View)



L PACKAGE
(Top View)

RECOMMENDED OPERATING CONDITIONS (Note 3)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Supply Voltage Range			30		V
Output Current (Peak)			±1		A
Output Current (Continuous)			200		mA
Analog Inputs (Pin 2, Pin 3)		0		2.6	V
Error Amp Output Sink Current			5		mA
Oscillator Frequency Range		0.1		500	kHz
Oscillator Timing Resistor	R_T	0.52		150	KΩ
Oscillator Timing Capacitor	C_T	0.001		1.0	µF
Operating Ambient Temperature Range:					
SG1842/43		-55		125	°C
SG2842/43		-25		85	°C
SG3842/43		0		70	°C

Note 3. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1842/SG1843 with -55°C ≤ T_A ≤ 125°C, SG2842/SG2843 with -25°C ≤ T_A ≤ 85°C, SG3842/SG3843 with 0°C ≤ T_A ≤ 70°C, V_{CC} = 15V (Note 7), R_T = 10kΩ, and C_T = 3.3nF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Symbol	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section												
Output Voltage		T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation		12 ≤ V_{IN} ≤ 25V		6	20		6	20		6	20	mV
Load Regulation		1 ≤ I_O ≤ 20mA		6	25		6	25		6	25	mV
Temperature Stability (Note 4)				0.2	0.4		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation (Note 4)		Line, Load, Temp.	4.90		5.10	4.90		5.10	4.82		5.18	V
Output Noise Voltage (Note 4)	V_N	10Hz ≤ f ≤ 10kHz, T_J = 25°C		50			50			50		µV
Long Term Stability (Note 4)		T_A = 125°C, 1000hrs		5	25		5	25		5	25	mV
Output Short Circuit			-30	-100	-180	-30	-100	-180	-30	-100	-180	mA
Oscillator Section												
Initial Accuracy		T_J = 25°C	47	52	57	47	52	57	47	52	57	kHz
Voltage Stability		12 ≤ V_{CC} ≤ 25V		0.2	1		0.2	1		0.2	1	%
Temperature Stability (Note 4)		T_{MIN} ≤ T_A ≤ T_{MAX}		5			5			5		%
Amplitude		$V_{RT/CT}$ (Peak to Peak)		1.7			1.7			1.7		V
Discharge Current		T_J = 25°C	7.8	8.3	8.8	7.5	8.4	9.3	7.5	8.4	9.3	mA
		T_{MIN} ≤ T_A ≤ T_{MAX}	7.0		9.0	7.2		9.5	7.2		9.5	mA
Error Amp Section												
Input Voltage		V_{COMP} = 2.5V	2.45	2.50	2.55	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current				-0.3	-1		-0.3	1		-0.3	-2	µA
Open Loop Gain	A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		65	90		dB
Unity Gain Bandwidth (Note 4)		T_J = 25°C	0.7	1		0.7	1		0.7	1		MHz
Power Supply Rejection Ratio	PSRR	12 ≤ V_{CC} ≤ 25V	60	70		60	70		60	70		dB
Output Sink Current		V_{VFB} = 2.7V, V_{COMP} = 1.1V	2	6		2	6		2	6		mA
Output Source Current		V_{VFB} = 2.3V, V_{COMP} = 5V	-0.5	-0.8		-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High		V_{VFB} = 2.3V, R_L = 15K to gnd	5	6		5	6		5	6		V
V_{OUT} Low		V_{VFB} = 2.7V, R_L = 15K to V_{REF}		0.7	1.1		0.7	1.1		0.7	1.1	V

(Electrical Characteristics continue next page.)

ELECTRICAL CHARACTERISTICS (Cont'd.)

Parameter	Symbol	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current Sense Section												
Gain (Notes 5 & 6)			2.85	3	3.15	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal (Note 5)		V_{COMP} = 5V	0.9	1	1.1	0.9	1	1.1	0.9	1	1.1	V
Power Supply Rejection Ratio (Note 5)	PSRR	12 ≤ V_{CC} ≤ 25V		70			70			70		dB
Input Bias Current				-2	-10		-2	-10		-2	-10	µA
Delay to Output (Note 4)				150	300		150	300		150	300	ns
Output Section												
Output Low Level		I_{SINK} = 20mA		0.1	0.4		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200mA		1.5	2.2		1.5	2.2		1.5	2.2	V
Output High Level		I_{SOURCE} = 20mA	13	13.5		13	13.5		13	13.5		V
		I_{SOURCE} = 200mA	12	13.5		12	13.5		12	13.5		V
Rise Time		T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Fall Time		T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Under-Voltage Lockout Section												
Start Threshold		1842	15	16	17	15	16	17	14.5	16	17.5	V
		1843	7.8	8.4	9.0	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After Turn-On		1842	9	10	11	9	10	11	8.5	10	11.5	V
		1843	7.0	7.6	8.3	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section												
Maximum Duty Cycle			93	95	100	90	95	100	90	95	100	%
Minimum Duty Cycle					0			0			0	%
Power Consumption Section												
Start-Up Current				0.5	1		0.5	1		0.5	1	mA
Operating Supply Current		V_{FB} = V_{ISENSE} = 0V		11	17		11	17		11	17	mA
V_{CC} Zener Voltage		I_{CC} = 25mA		34			34			34		V

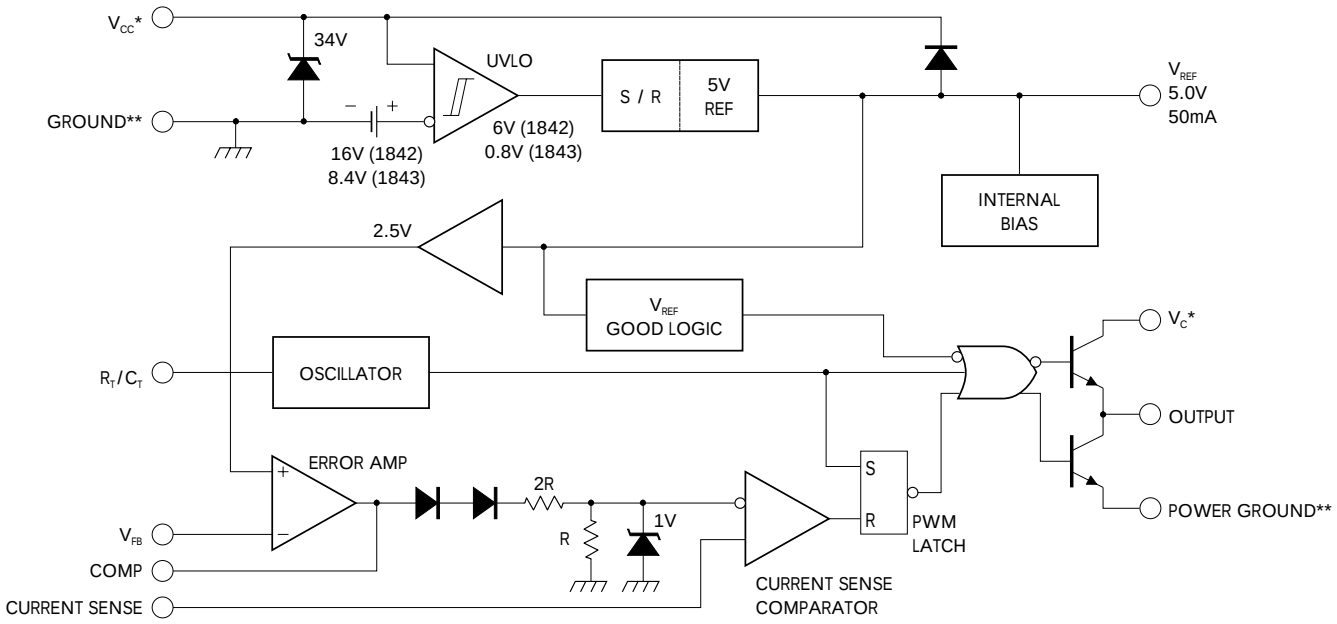
Notes: 4. These parameters, although guaranteed, are not 100% tested in production.

5. Parameter measured at trip point of latch with V_{VFB} = 0.

6. Gain defined as: $A = \frac{\Delta V_{COMP}}{\Delta V_{ISENSE}}$; $0 \le V_{ISENSE} \le 0.8V$.

7. Adjust V_{CC} above the start threshold before setting at 15V.

BLOCK DIAGRAM



* - V_{CC} and V_C are internally connected for 8 pin packages.
** - POWER GROUND and GROUND are internally connected for 8 pin packages.

GRAPH / CURVE INDEX

Characteristic Curves

FIGURE #

FIGURE INDEX

Application Information

FIGURE #

Typical Applications Section

FIGURE #

CHARACTERISTIC CURVES

FIGURE 1. — DROPOUT VOLTAGE vs. TEMPERATURE

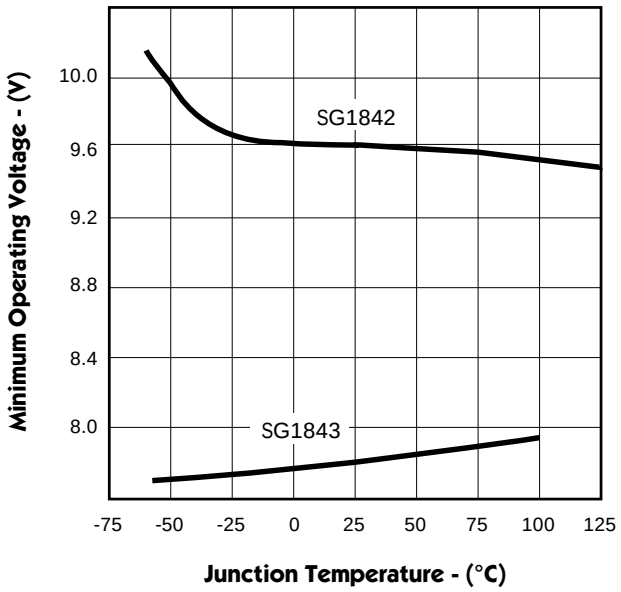


FIGURE 2. — OSCILLATOR TEMPERATURE STABILITY

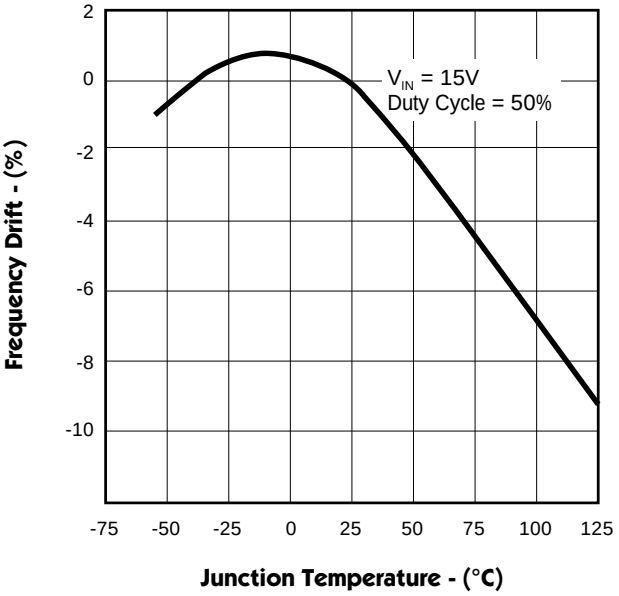


FIGURE 3. — CURRENT SENSE TO OUTPUT DELAY vs. TEMPERATURE

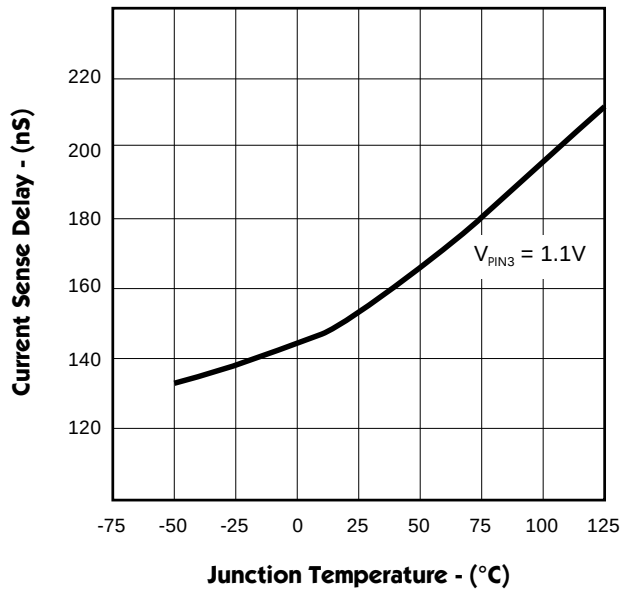
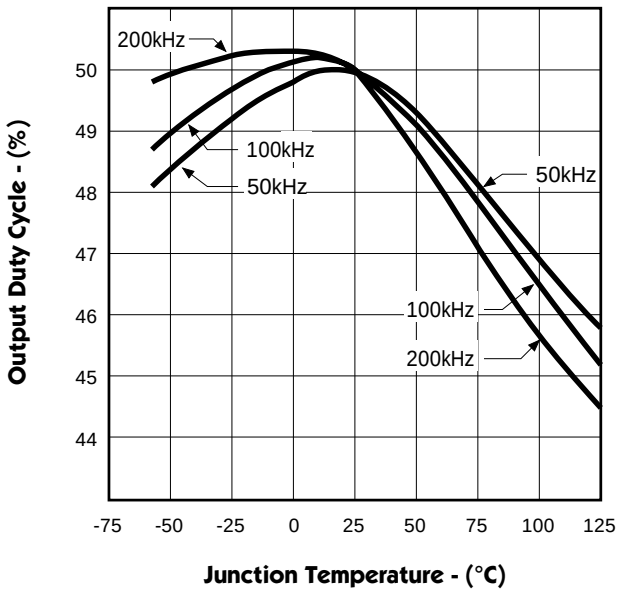


FIGURE 4. — OUTPUT DUTY CYCLE vs. TEMPERATURE



CHARACTERISTIC CURVES

FIGURE 5. — START-UP CURRENT vs. TEMPERATURE

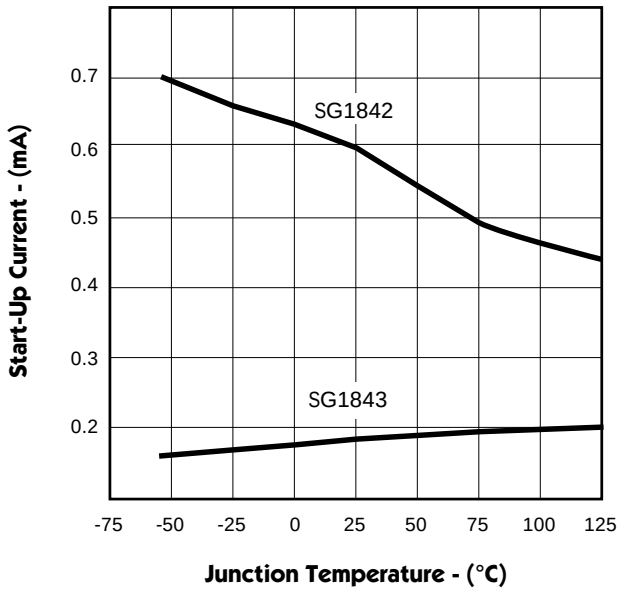


FIGURE 6. — REFERENCE VOLTAGE vs. TEMPERATURE

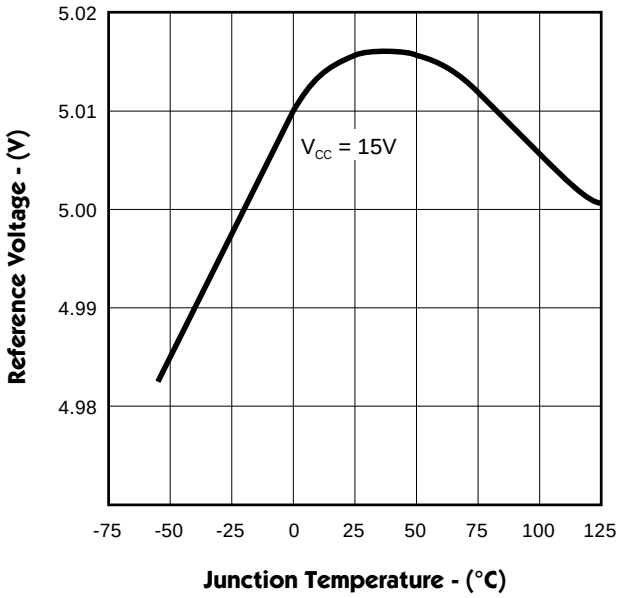


FIGURE 7. — START-UP VOLTAGE THRESHOLD vs. TEMPERATURE

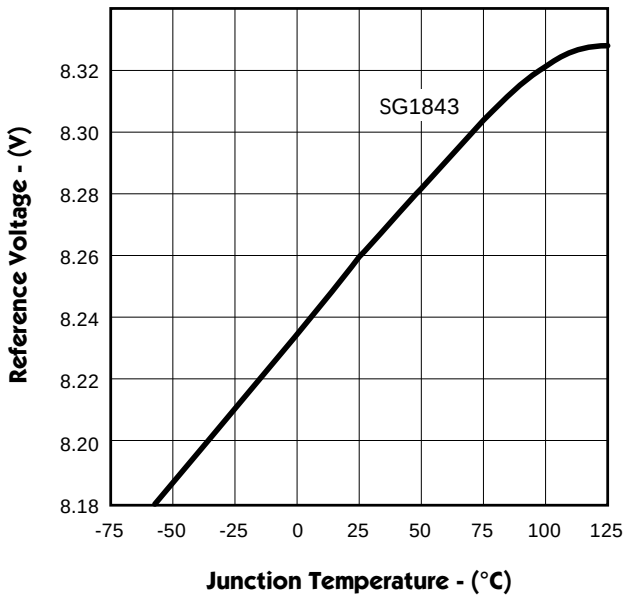
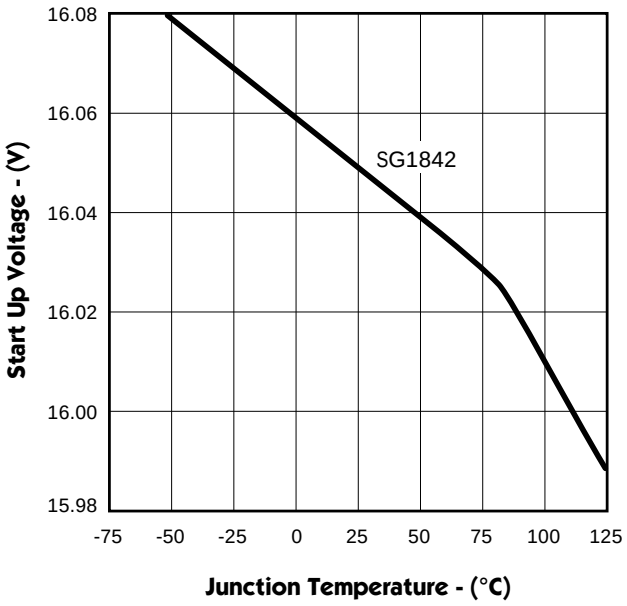


FIGURE 8. — START-UP VOLTAGE THRESHOLD vs. TEMPERATURE



CHARACTERISTIC CURVES

FIGURE 9. — OSCILLATOR DISCHARGE CURRENT vs. TEMPERATURE

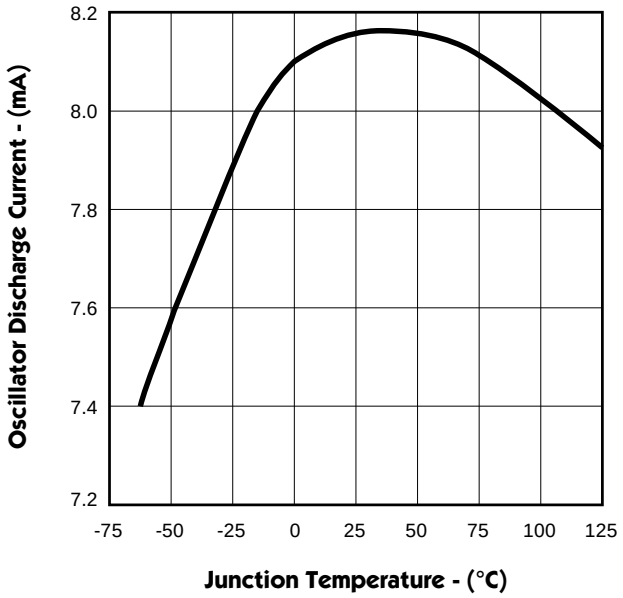


FIGURE 10. — OUTPUT SATURATION VOLTAGE vs. OUTPUT CURRENT & TEMPERATURE

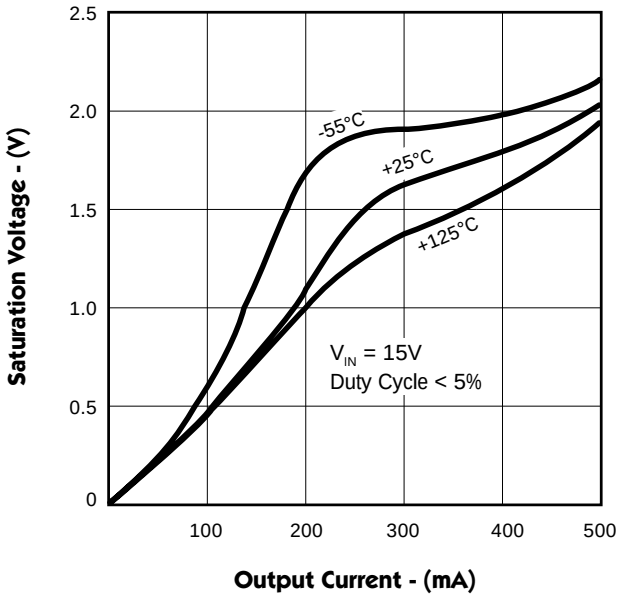


FIGURE 11. — CURRENT SENSE THRESHOLD vs. ERROR AMPLIFIER OUTPUT

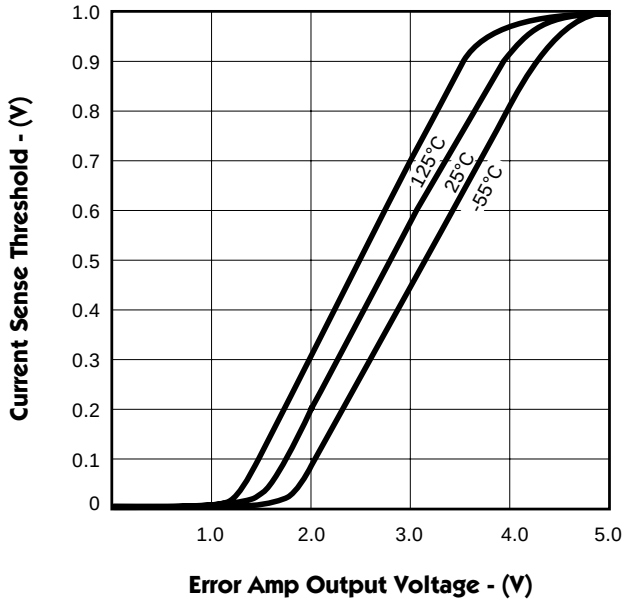
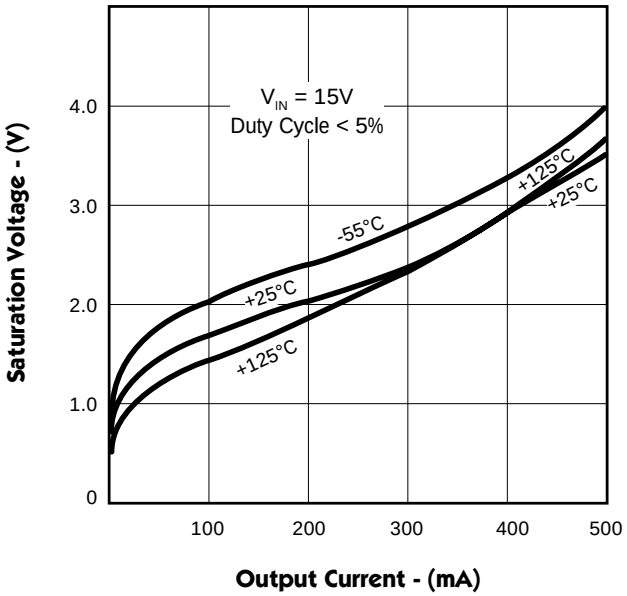


FIGURE 12. — OUTPUT SATURATION VOLTAGE vs. OUTPUT CURRENT & TEMPERATURE



APPLICATION INFORMATION

OSCILLATOR

The oscillator of the 1842/43 family of PWM's is designed such that many values of R_T and C_T will give the same oscillator frequency, but only one combination will yield a specific duty cycle at a given frequency.

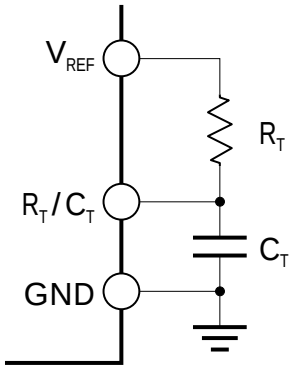
Given: Frequency ≡ f
Maximum Duty Cycle ≡ D_m

Calculate: $$R_T = 267\left[\frac{(1.76)^{1/D_m} - 1}{(1.76)^{(1-D_m)/D_m} - 1}\right] \ (\Omega)$$

where $.3 < D_m < .95$

$$C_T = \frac{1.86 * D_m}{f * R_T} \ (\mu F)$$

For Duty-Cycles above 95% use:



$$F \approx \frac{1.86}{R_T C_T} \quad \text{where } R_T \geq 5k\Omega$$

FIGURE 13 — OSCILLATOR TIMING CIRCUIT

A set of formulas are given to determine the values of R_T and C_T for a given frequency and maximum duty cycle. (Note: These formulas are less accurate for smaller duty cycles or higher frequencies. This will require trimming of R_T or C_T to correct for this error.)

Example:

A Flyback power supply requires a maximum of 45% duty cycle at a switching frequency of 50kHz. What are the values of R_T and C_T?

Given: f = 50kHz
$D_m = 0.45$

Calculate: $$R_T = 267\left[\frac{(1.76)^{1/.045} - 1}{(1.76)^{.55/.45} - 1}\right] = 674\Omega$$

$$C_T = \frac{1.86 * 0.45}{50000 * 674} = .025\mu F$$

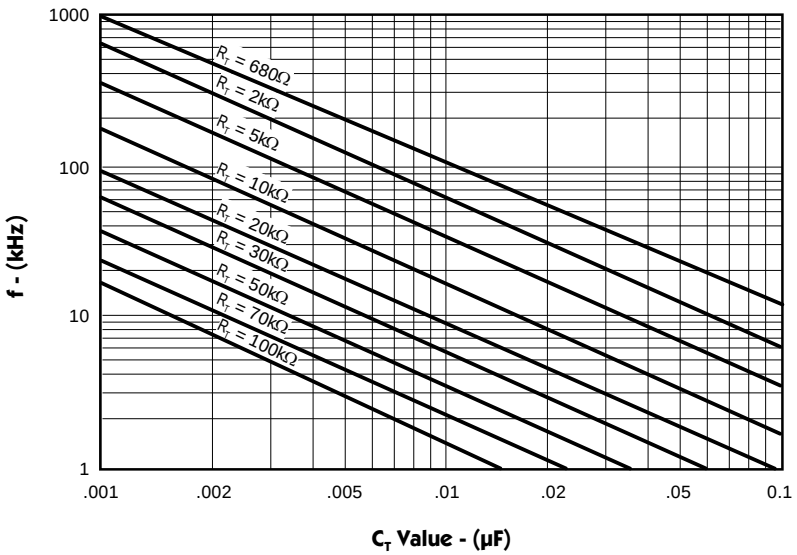


FIGURE 14 — OSCILLATOR FREQUENCY vs. R_T FOR VARIOUS C_T

TYPICAL APPLICATION CIRCUITS

Pin numbers referenced are for 8-pin package and pin numbers in parenthesis are for 14-pin package.

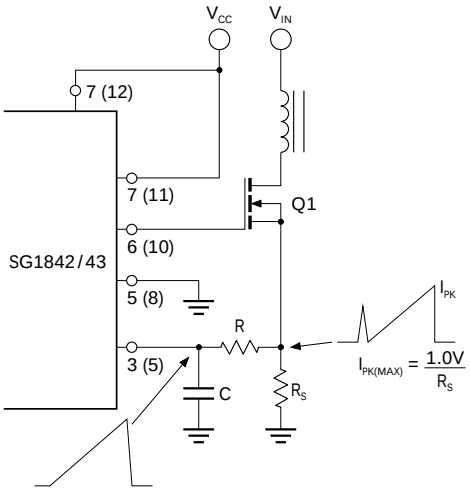


FIGURE 15. — CURRENT-SENSE SPIKE SUPPRESSION

The RC low pass filter will eliminate the leading edge current spike caused by parasitics of Power MOSFET.

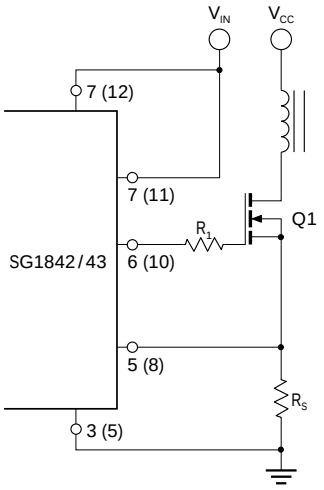


FIGURE 16. — MOSFET PARASITIC OSCILLATIONS

A resistor (R_1) in series with the MOSFET gate reduce overshoot and ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

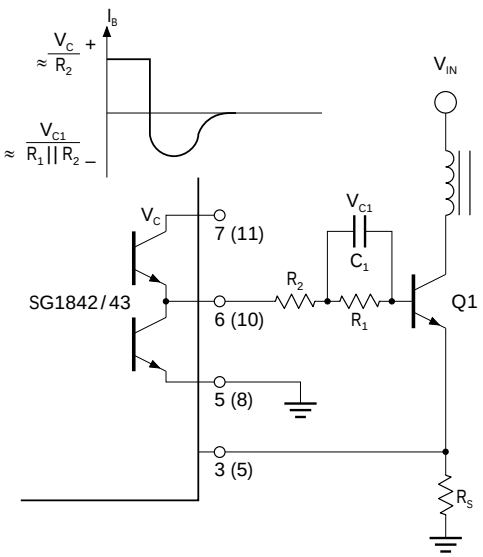


FIGURE 17. — BIPOLAR TRANSISTOR DRIVE

The 1842/43 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

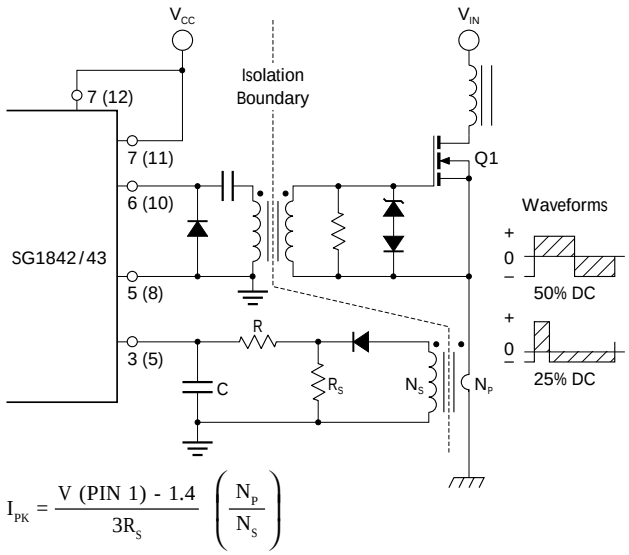
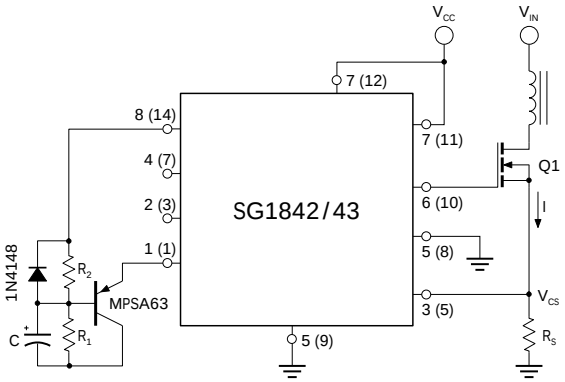


FIGURE 18. — ISOLATED MOSFET DRIVE

Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.

TYPICAL APPLICATION CIRCUITS (continued)



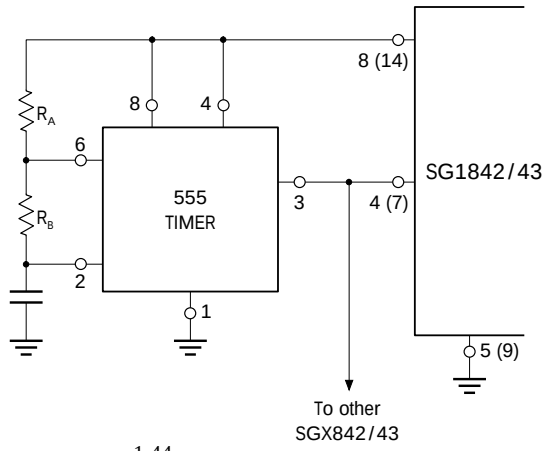
$$I_{PK} = \frac{V_{CS}}{R_S} \quad \text{Where: } V_{CS} = 1.67\left(\frac{R_1}{R_1+R_2}\right) \text{ and } V_{C.S.MAX} = 1V \text{ (Typ.)}$$

$$t_{SOFTSTART} = -\ln\left[1 - \frac{V_{EAO} - 1.3}{5\left(\frac{R_1}{R_1+R_2}\right)}\right]\left(\frac{R_1 R_2}{R_1+R_2}\right)C$$

where; $V_{EAO} \equiv$ voltage at the Error Amp Output under minimum line and maximum load conditions.

FIGURE 19. — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFTSTART

Softstart and adjustable peak current can be done with the external circuitry shown above.



$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$f = \frac{R_B}{R_A + 2R_B}$$

FIGURE 20. — EXTERNAL DUTY CYCLE CLAMP AND MULTI-UNIT SYNCHRONIZATION

Precision duty cycle limiting as well as synchronizing several 1842/1843's is possible with the above circuitry.

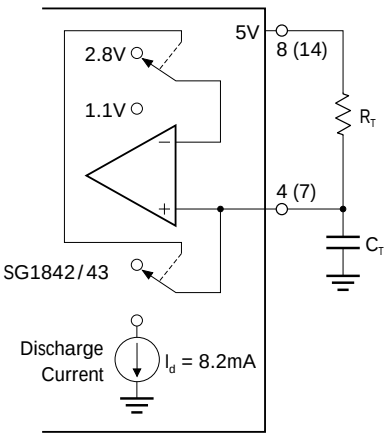


FIGURE 21. — OSCILLATOR CONNECTION

The oscillator is programmed by the values selected for the timing components R_T and C_T. Refer to application information for calculation of the component values.

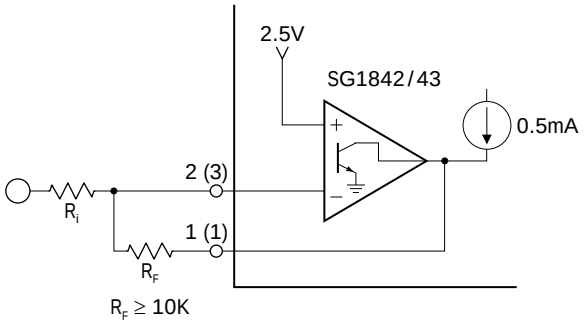


FIGURE 22. — ERROR AMPLIFIER CONNECTION

Error amplifier is capable of sourcing and sinking current up to 0.5mA.

TYPICAL APPLICATION CIRCUITS (continued)

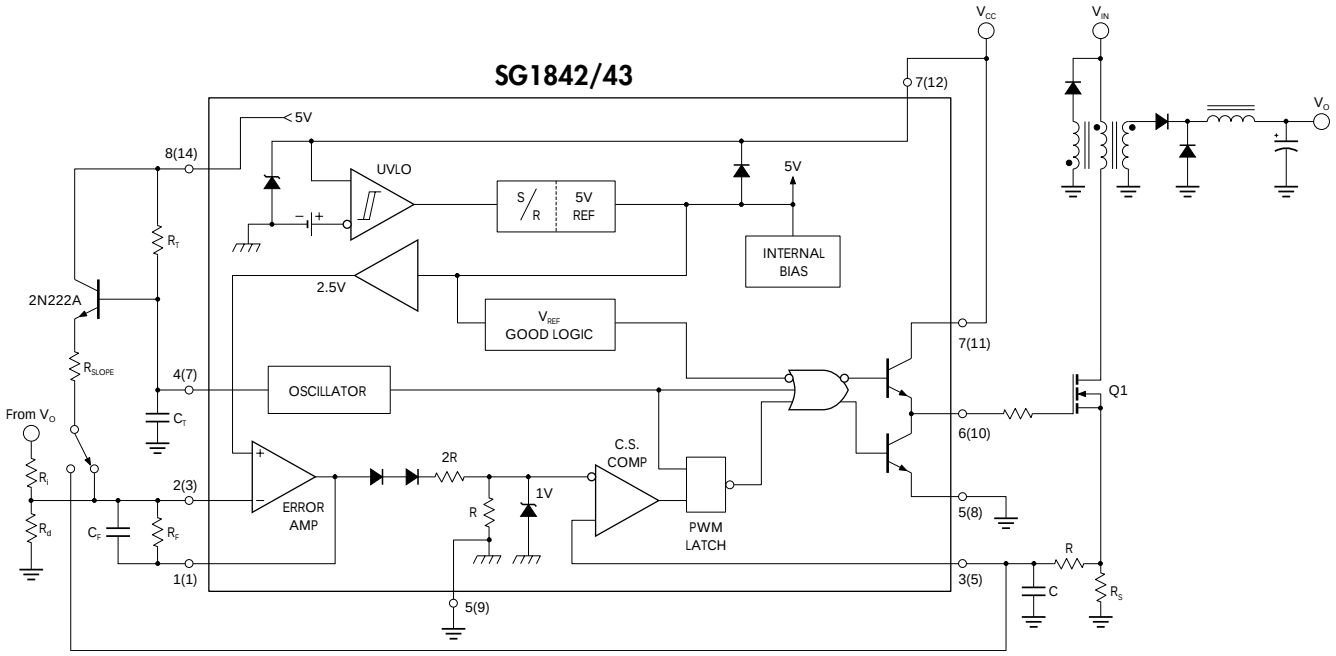


FIGURE 23. — SLOPE COMPENSATION

Due to inherent instability of current mode converters running above 50% duty cycle, a slope compensation should be added to either current sense pin or the error amplifier. Figure 23 shows a typical slope compensation technique.

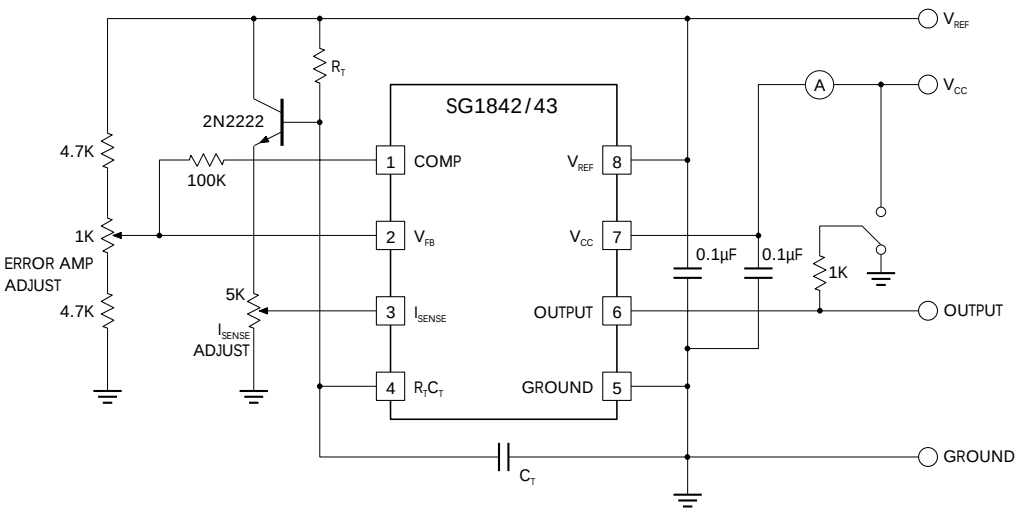


FIGURE 24. — OPEN LOOP LABORATORY FIXTURE

High-peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

TYPICAL APPLICATION CIRCUITS (continued)

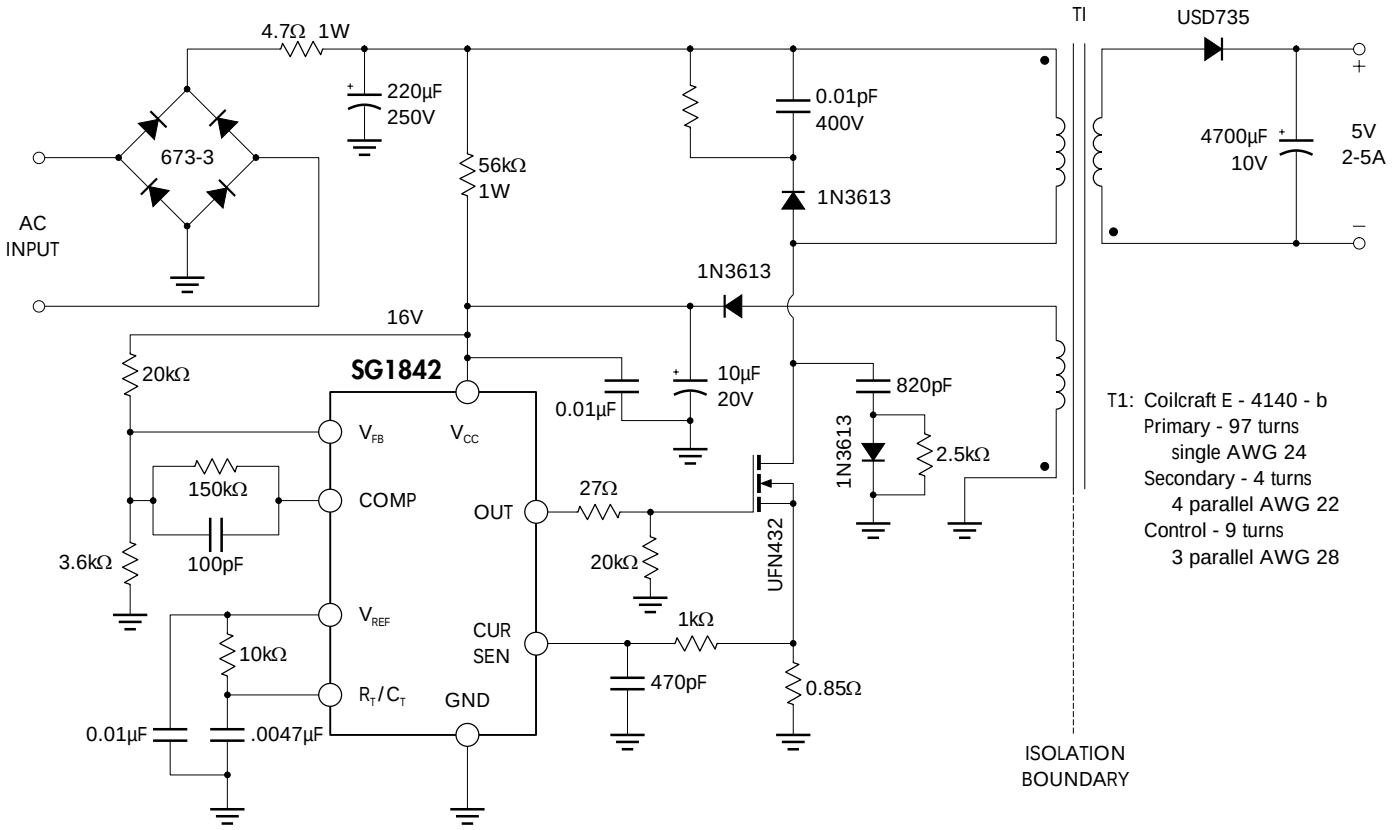


FIGURE 25. — OFF-LINE FLYBACK REGULATOR

SPECIFICATIONS

Input line voltage:	90VAC to 130VAC
Input frequency:	50 or 60Hz
Switching frequency:	40KHz ±10%
Output power:	25W maximum
Output voltage:	5V +5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 Watts,	
V_{IN} = 90VAC:	70%
V_{IN} = 130VAC:	65%
Output short-circuit current:	2.5Amp average

* This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the SG1842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance.